Sublayer Delay for Interleaved 100G FEC

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Introduction

- **Interleaved 100G FEC (CL161) latency is larger than CL91 latency**
- **Current P802.3ck/D1.0 draft specifies a CL161 sublayer delay constraint that is the same as CL91**
- **The sublayer delay value for RS-FEC-Int should be increased in proportion to the increased sublayer latency**

Previous Work

- gustlin_3ck_01a_1119.pdf, slide 6, contains the adopted P802.3ck baseline for Dual FEC for 100GBASE-CR1 and 100GBASE-KR1
  - nicholl_3ck_01b_0519.pdf, contains the details of the Interleaved 100G FEC
- gustlin_3ck_01_1118.pdf, slide 8, contains discussion about latency in Interleaved 100G FEC

Overview

- **This presentation reviews the 100G Sublayer Delay constraints and proposes updated values for the CL161 RS-FEC-Int Sublayer**

100G Sublayer Delays

- **Table 80-5 summarizes the Sublayer delay constraints for 100G**
- **These delay constraints are used to provide predictable operation of the MAC Control PAUSE operation**
- **The current 100GBASE-R RS-FEC Sublayer delay is 40960 bit times**
  - 40960 BT = 80 pause_quanta = 409.60 ns
- **This delay constraint information is also found in Clause 91.4**

Table 80–5—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
100GBASE-R PCS	35 328	69	353.28	See 82.5.
100GBASE-R FEC	122 880	240	1228.8	See 74.6.
100GBASE-R RS-FEC	40 960	80	409.60	See 91.4.
100GBASE-R PMA	9 216	18	92.16	See 83.5.4.
100GBASE-KR4 PMD	2 048	4	20.48	Includes delay of one direction through backplane medium. See 93.4.
100GBASE-KP4 PMA/PMD	8 192	16	81.92	Includes delay of one direction through backplane medium. See 94.2.5

Source: IEEE 802.3-2018 Clause 80

91.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 40960 bit times (80 pause_quanta or 409.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

Source: IEEE 802.3-2018 Clause 91

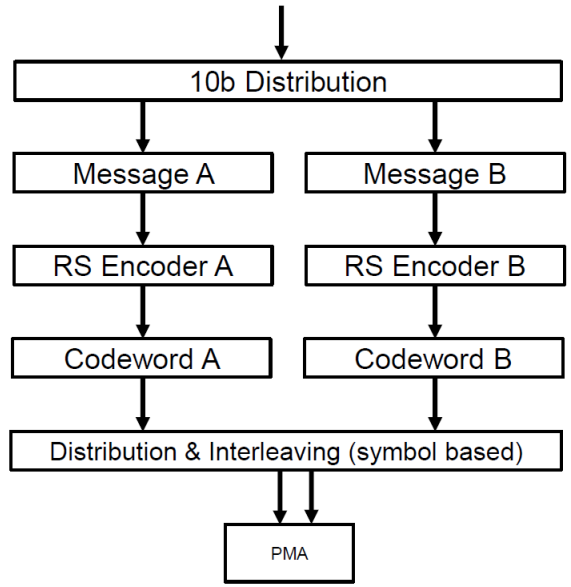
Interleaved 100G FEC Latency

- **Currently Table 80-5 contains no entry for RS-FEC-Int sublayer**
- **Clause 161.4 refers to 91.4, which implies that the delay constraint for RS-FEC-Int is the same as the delay constraint for RS-FEC sublayer**
- **However, CL161 Interleaved 100G FEC consumes an additional 51-102 ns of latency beyond CL91 latency**
  - The exact latency increase depends on implementation

Latency for the 100G Interleaved FEC Sublayer

Current Clause 91 RS544	
Latency	**Contributor**
51ns	Block time
50-100ns	Processing*
101-151ns	Total

Potential RS544 Interleaved	
Latency	**Contributor**
102ns	Block time
50-150ns	Processing*
152-252ns	Total



*depends on parallelism/latency tradeoffs

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Source: gustlin_3ck_01_1118.pdf

Proposed delay constraints for RS-FEC-Int

- Assuming the worst case additional latency of ~102 ns for RS-FEC-Int
- At 100G, one pause_quanta is 5.12ns, thus 102 ns is 20 pause_quanta
- The current Clause 91 RS-FEC sublayer delay is 80 pause_quanta
- Propose to use 100 pause_quanta for the Clause 161 RS-FEC-Int sublayer delay

- Propose to update Clause 161.4 with the following text:
  - The maximum delay contributed by the RS-FEC-Int sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 51200 bit times (100 pause_quanta or 512 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

Proposed Sublayer delay table entry for RS-FEC-Int

- **Propose to update Table 80-5 with values for the 100GBASE-R RS-FEC-Int sublayer**

Proposed Table 80-5 Sublayer delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)	Notes
…	…	…	…	…
100GBASE-R PCS	35 328	69	353.28	See 82.5
100GBASE-R FEC	122 880	240	1228.8	See 74.6
100GBASE-R RS-FEC	40 960	80	409.60	See 91.4
100GBASE-R RS-FEC-Int	51 200	100	512	See 161.4
…	…	…	…	…

Summary

- **This presentation reviews the sublayer delay constraint for Interleaved 100G FEC and proposes a new value for CL161**
- **Recommend to update P802.3ck draft with the new value**

Thank You!

Backups

200G Sublayer Delays

- **Table 116-5 summarizes the Sublayer delay constraints for 200G**
- **The current 200GBASE-R PCS Sublayer delay is 160 256 bit times**
  - 160 256 BT = 313 pause_quanta = 801.28 ns
- **This delay constraint information is also found in Clause 119.5**

Table 116–5—Sublayer delay constraints (200GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
200G MAC, RS, and MAC Control	49 152	96	245.76	See 117.1.4.
200GBASE-R PCS or 200GXS[d]	160 256	313	801.28	See 119.5.

Source: IEEE 802.3-2018 Clause 116

119.5 Delay constraints

The maximum delay contributed by the 200GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 160 256 BT (313 pause_quanta or 801.28 ns). The maximum delay contributed by the 400GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 320 000 BT (625 pause_quanta or 800 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

Source: IEEE 802.3-2018 Clause 119

400G Sublayer Delays

- **Table 116-6 summarizes the Sublayer delay constraints for 400G**
- **The current 400GBASE-R PCS Sublayer delay is 320 000 bit times**
  - 320 000 BT = 625 pause_quanta = 800 ns
- **This delay constraint information is also found in Clause 119.5**

Table 116–6—Sublayer delay constraints (400GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
400G MAC, RS, and MAC Control	98 304	192	245.76	See 117.1.4.
400GBASE-R PCS or 400GXS[d]	320 000	625	800	See 119.5.

Source: IEEE 802.3-2018 Clause 116

119.5 Delay constraints

The maximum delay contributed by the 200GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 160 256 BT (313 pause_quanta or 801.28 ns). The maximum delay contributed by the 400GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 320 000 BT (625 pause_quanta or 800 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

Source: IEEE 802.3-2018 Clause 119