C2M Methodology, CTLE Gain, and DFE Taps

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Overview

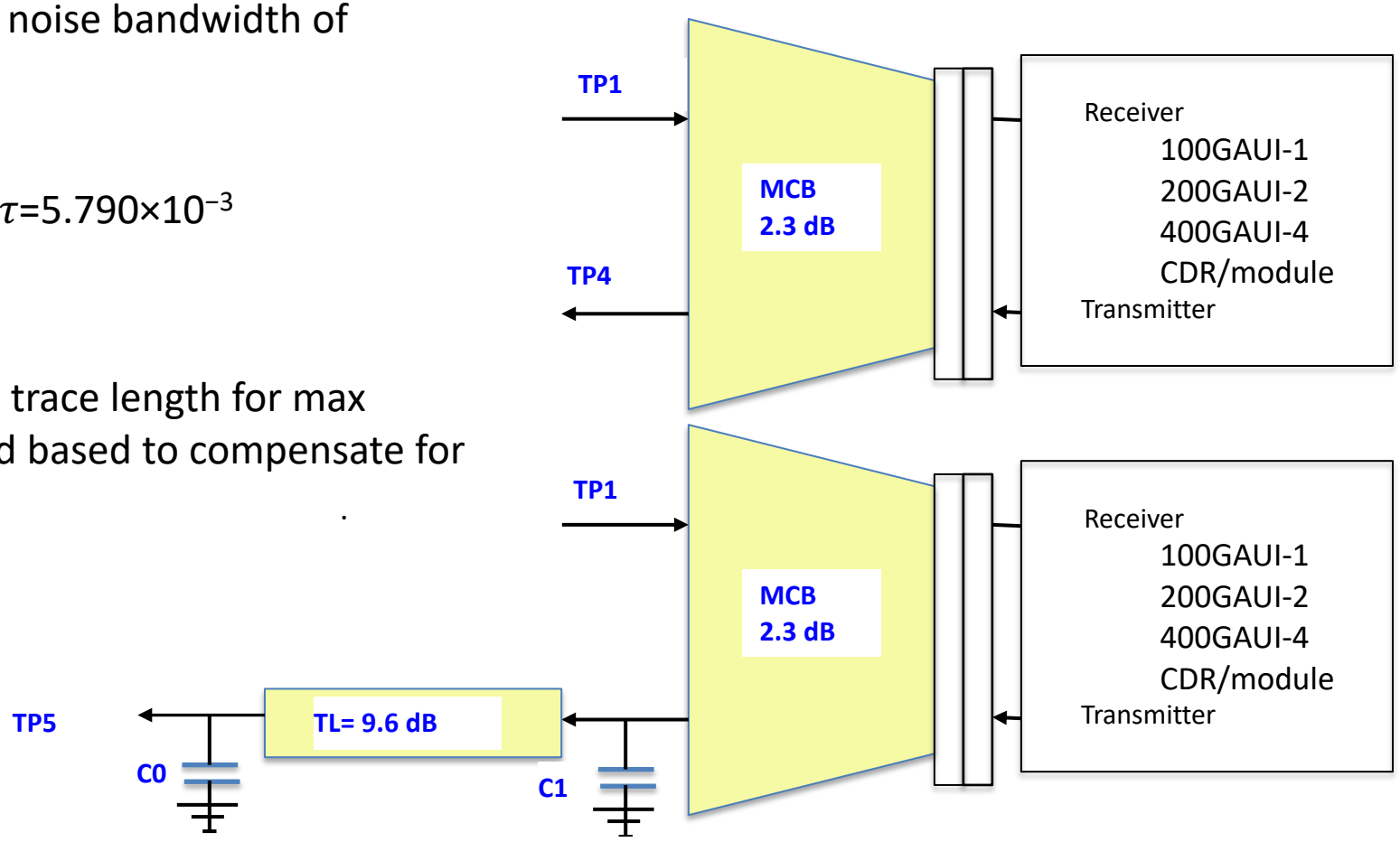
- **Module to ASIC test methodology**
  - Purpose to use CR (C0, C1) to add some impairment to the MCB accounting for long barrel vias
- **Module output measurement test points**
  - Is TP4 and TP5 sufficient
- **COM analysis at TP4, TP5**
  - Penalty associated from fixed module TX FIR
- **Addressing comments 191, 193, 196, and 199.**

Module to ASIC Test Methodology

- **Unlike ASIC-Module the Module-ASIC output at TP4 and TP5 measured with compliance board and reference trace typically has COM >6 dB dB with 4T DFE receiver**
  - If one replaces module compliance board with realistic host with long barrel via and a short stub then COM can drop by ~ 2 dB
  - COM can drop to 2-3 dB for realistic channel if one include the ASIC package
- **Instead of just measuring TP5 with bare reference trace and getting a very optimistic COM, it is recommended to use benartsi_3ck_01a_0719 method initially purposed for CR end to end links with (C0, C1)= (29, 19 fF) for C2M TP5 measurements**
- **Given that there is no way to add (C0, C1) to TP4 unless one create single lumped**
  - Adding C0/C1 to short PCB (68 mm) can produce unpredictable result as function of trace delay
  - But adding C0/C1 to 244 mm trace with 9.6 dB loss for TP5 is not sensitive to trace delay
- **Proposed test methodology at module output is as following:**
  - Measure TP4 without C0/C1 at this point
  - Measure TP5 with addition of C0/C1.

TP1, TP4 and TP5 Test Points

- **TP4/TP5 measurements are with addition of 0.577 nV^2/GHz (TBD) noise to account for BGA crosstalk**
  - The equivalent 0.577 mV RMS noise is for noise bandwidth of 53.125*0.75 = 39.84 GHz
- **Transmission line parameters**
  - $\gamma 0=0$, $a1 =3.8206\times10^{-4}$, $a2 =9.5909\times10^{-5}$, $\tau=5.790\times10^{-3}$
  - TP4 is MCB output measurement
  - TP4 is measured at MCB output
  - TP5 is measured with addition of 244 mm trace length for max channel loss (trace length may be adjusted based to compensate for MCB loss deviation from 2.3 dB)



COM 2.76 Module to Host (CDR PKG 2-8 mm) with addition of C0/C1

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.1	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1e-4 1.2e-4]	nF	[TX RX]
L_s	[0.1 0.12]	nF	[TX RX]
C_b	[0 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[2 8; 0.01 0.01]	mm	[test cases]
z_p (NEXT)	[2 8; 0.01 0.01]	mm	[test cases]
z_p (FEXT)	[2 8; 0.01 0.01]	mm	[test cases]
z_p (RX)	[13 29; 1.8 1.8]	mm	[test cases]
C_p	[0.65e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.72		min
c(-1)	-0.18		[min:step:max]
c(-2)	0.04		[min:step:max]
c(1)	-0.04		[min:step:max]
N_b	4	UI	
b_max(1)	0.3		
b_max(2..N_b)	0.1		
g_DC	[-14:1:-4]	dB	[min:step:max]
f_z	12.5	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:-1]		[min:step:max]
f_HP_PZ	1.3275	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.2		
ffe_backoff	1		

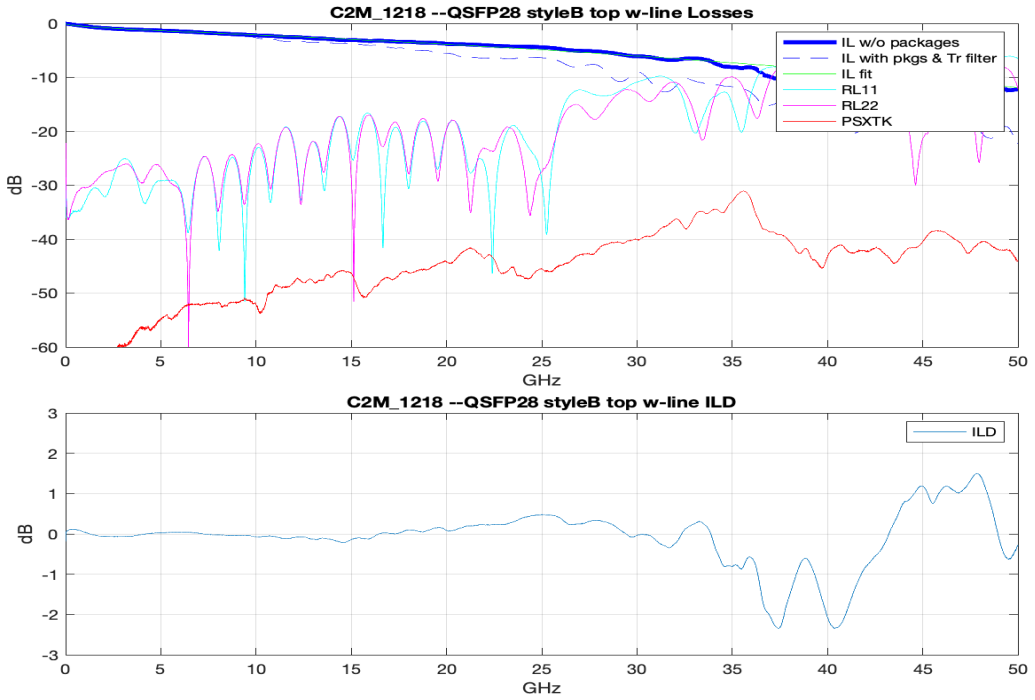
0.8

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[2 4 1 3]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	2.3407E+09	
rho_x	0.19	
fixture delay time	[0 0]	port1 port2]
TDR_W_TXPKG	1	
N_bx	4	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.37E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

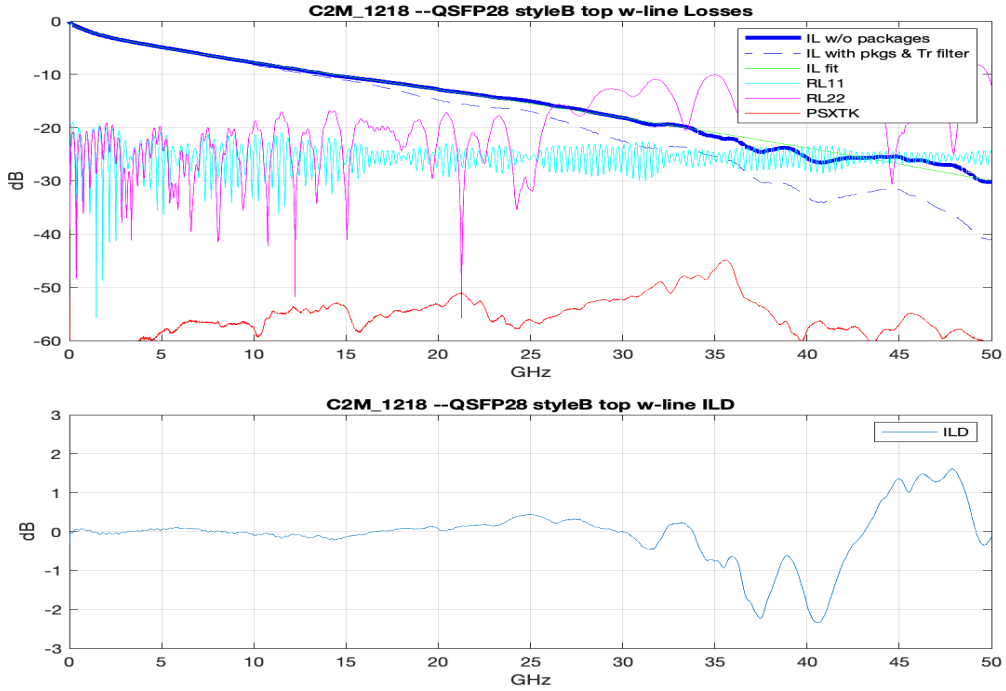
Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*244*	mm
z_bp (NEXT)	*244*	mm
z_bp (FEXT)	*244*	mm
z_bp (RX)	*0*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	2	taps per group
N_f	12	UI span for floating taps
bmaxg	0.1	DFE value for floating
B_float_RSS_MAX	**0.03**	rss tail tap limit
N_tail_start	**25**	UI) start of tail taps limi
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.825	GHz
A_ft	0.410	V
A_nt	**0.600**	V
heck_3ck_03b_0319	**Adopted Mar 2019**	**kasapi_3ck_02_1119**
walker_3ck_01d_0719	**Adopted July 2019**	**Adopted Nov 2019**
result of R_d=50		under consideration
benartsi_3ck_01a_0719	**no used for KR**	
mellitz_3ck_03_0919		

TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

Mated board IL = 5.2 dB
Total IL with 8 mm PKG=8.0 dB



Mated board + 220 mm trace IL = 16.1 dB
Total IL with 8 mm PKG=18.6 dB



Yamaichi QSFP56 Mated Board Near End TP4

❑ Mated board COM with addition of PCB trace and C0/C1*

- With addition of C0/C1 COM improves by ~1.0
  - The 68 mm trace with new Tau no longer creates worst case COM
- Having a fixed single TX FIR setting result in only ~0.2 dB of penalty
- DFE B1-B4<|0.05|.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=15.1 dB ERL22=11.2 dB Optimum TX FIR	4 DFE COM	5.2	8.0	56.6/54.2	0.156/0.187	6.9/6.8	5.2/5.3
	4DFE + 68 mm	8.6	11.6	47.8/45.2	0.187/0.219	5.8/5.9	6.3/6.2
	4T DFE+68 mm +C0/C1	8.6	12.6	41.4/31.7	0.187/0.187	5.9/6.7	6.1/5.4
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=15.1 dB ERL22=11.2 dB TX FIR [0.04 -0.18 0.72 -0.04]	4 DFE COM	5.2	8.0	47.8/46.1	0.187/0.187	7.4/7.2	4.8/4.9
	4DFE + 68 mm	8.6	11.6	43.9/42.1	0.187/0.187	6.0/5.9	6.1/6.1
	4T DFE+68 mm +C0/C1	8.6	12.6	42.6/36.7	0.187/0.187	6.0/6.9	6.0/5.2

* Using CR COM reduced TX SNR and increased eta_0.

Yamaichi QSFP56 Mated Far End TP5 Results

- **Mated board COM with addition of PCB trace and C0/C1***
  - With addition of C0/C1 COM decreases by about 0.4 dB of penalty
  - Having a fixed single TX FIR setting result in only ~0.2 dB of penalty
  - DFE B1max<0.28, B2-B4<0.03.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	4T DFE +215mm	15.8	18.7	27.1/25.1	0.156/0.187	5.7/5.8	6.4/6.2
	4T DFE +215mm +C0/C1	15.8	19.6	23.2/19.4	0.156/0.187	6.3/7.9	6.3/5.7
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB TX FIR [0.04 -0.18 0.72 -0.04]	4T DFE +215mm	15.8	18.7	27.1/25.1	0.156/0.187	5.7/5.8	6.4/6.2
	4T DFE +215mm +C0/C1	15.8	19.6	25.4/21.1	0.187/0.156	5.8/6.6	6.2/5.5

* Using CR COM reduced TX SNR and increased eta_0.

Yamaichi QSFP56 Mated Board at Slicer

- **Mated board COM with addition of PCB trace and C0/C1***
  - With addition of C0/C1 COM decreases by about 0.6 dB of penalty
  - Having a fixed single TX FIR setting result in only ~0.3 dB of penalty
  - TDFE B1max<0.22, B2-B4<|0.06|.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	4 DFE COM	5.2	12.8	36.3/36.9	0.125/0.156	8.8/6.9	3.9/5.2
	4DFE + 68 mm	8.6	16.1	30.6/30.2	0.125/0.187	8.1/6.4	4.3/5.6
	4T DFE+68 mm +C0/C1	8.6	17.1	24.0/24.2	0.125/0.156	9.7/7.7	3.5/4.6
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB TX FIR [0.04 -0.18 0.72 -0.04]	4 DFE COM	5.2	12.8	30.6/33.8	0.156/0.156	9.5/7.2	3.5/5.0
	4DFE + 68 mm	8.6	16.1	28.6/28.4	0.156/0.187	8.5/6.6	4.1/5.5
	4T DFE+68 mm +C0/C1	8.6	17.1	20.8/22.7	0.125/0.156	10.2/8.0	3.2/4.4

* Using CR COM reduced TX SNR and increased eta_0.

Yamaichi QSFP56 Mated Board at Slicer

- **Mated board COM with addition of PCB trace and C0/C1***
  - With addition of C0/C1 COM decreases by about 0.8 dB of penalty
  - Having a fixed single TX FIR setting result in only ~0.5 dB of penalty
  - DFE B1max<0.3, B2-B4<0.04.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	4T DFE +215mm	15.8	23.2	17.1/14.3	0.125/0.156	7.4/6.7	4.8/5.4
	4T DFE +215mm +C0/C1	15.8	24.3	12.5/11.7	0.094/0.156	9.2/7.8	3.7/4.6
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB TX FIR [0.04 -0.18 0.72 -0.04]	4T DFE +215mm	15.8	23.2	16.0/13.1	0.156/0.156	7.6/7.1	4.7/5.1
	4T DFE +215mm +C0/C1	15.8	24.3	11.3/10.3	0.125/0.125	9.6/8.8	3.5/3.9

* Using CR COM reduced TX SNR and increased eta_0.

COM Analysis on Lim Channel 1 and 4 – Module to ASIC at TP5

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Fixed TX FIR setting is the optimum setting for Yamaichi mated board + 68 mm with C0/C1
  - Sub-optimum TX FIR may have as much as 0.6 dB COM penalty
  - Even with addition of C0/C1 to the MCB the Lim COM’s are about 0.5 dB worse
  - DFE B1max<0.2, B2-B4<0.05 for both 2” and 9” Lim Channels.

Channel	TX Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Lim Channel 2” at TP5 FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB, ERL22=9.3 dB	Optimum	5.9	8.6	52.5/50.8	0.187/0.187	7.1/7.0	5.1/5.1
	Fixed*	5.9	8.6	42.3/39.8	0.187/0.187	7.8/7.9	4.5/4.6
Lim Channel 9” at TP5 FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB	Optimum	14.8	16.8	26.6/25.0	0.156/0.187	6.0/6.5	6.1/5.6
	Fixed*	14.8	16.8	24.6/23.8	0.187/0.187	6.4/6.6	5.7/5.5

*** TX FIR [0.04 -0.18 0.72 -0.04]**

COM Analysis on Lim Channel 1 and 4 – Module to ASIC at Slicer

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Fixed TX FIR setting is the optimum setting for Yamaichi mated board + 68 mm with C0/C1
  - Sub-optimum TX FIR has no more than 0.4 dB penalty
  - COM is similar between Lim 9” and HCB/MCB+215 mm+C0/C1 but 2” Lim channel with short package has over 2 dB higher penalty
  - DFE B1max<0.3, B2-B4<0.05 for both 2” and 9” Lim Channels.

Channel	TX FIR	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=11.3 dB, ERL22=10.5 dB	Optimum	5.9	14.3	19.6/31.7	0.0625/0.187	13.6/7.6	2.0/4.7
	Fixed*	5.9	14.3	13.9/28.8	0.094/0.187	15.6/7.9	1.6/4.5
Lim Channel 9” at Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB	Optimum	14.8	23.0	15.0/14.8	0.125/0.156	9.1/6.8	3.8/5.3
	Fixed*	14.8	23.0	14.2/15.2	0.125/0.156	9.4/6.9	3.6/5.3

* TX FIR [0.04 -0.18 0.72 -0.04]

Response to Comment 191 and 193

- **The 68 mm trace with C0/C1 has delay dependencies results, recommendation**
  - Measure TP4 directly without short trace and C0/C1
    - A better method is need to improve correlation between module output and Lim 2” channel
  - Measure TP5 with addition of C0/C1
- **Recommended Module to chip limits:**
  - TP4
    - VEC ≤ 7.0 dB
    - VEO ≥ 50 mV
    - EW ≥ 0.175 UI
  - TP5
    - VEC ≤ 7.0 dB
    - VEO ≥ 20 mV
    - EW ≥ 0.175 UI.

Response to Comment 196

- **DFE tap weight limit**
  - TP1a
    - B1(max) ≤ 0.3 and B[2-4] ≤ 0.08
  - TP4
    - B1(max) ≤ 0.15 and B[2-4] ≤ 0.05
  - TP5
    - B1(max) ≤ 0.3 and B[2-4] ≤ 0.08.

Response to Comment 199

- **CTLE tap weights allowed at TP1a, TP4, TP5.**

CTLE HF (dB)	CTLE LF (dB)	TP1a	TP4	TP5
1	0, 1	✓	✓	✓
2	0, 1	✓	✓	✓
3	0, 1	✓	✓	✓
4	0, 1	✓	✓	✓
4	1, 2	✓	✓	✓
5	1, 2	✓	✓	✓
6	1, 2	✓	✓	-
7	1, 2	✓	✓	-
8	2, 3	✓	✓	-
9	2, 3	✓	✓	-
10	2, 3	✓	✓	-
11	2, 3	✓	-	-
12	2, 3	✓	-	-
13	2, 3	✓	-	-

Summary

- **Propose module output measurement**
  - TP4 measured directly
  - TP5 measured with addition of addition of CR (C0, C1) caps + ~244 mm trace
- **Module TX FIR is set based for a nominal setting such that TP4 and TP5 are met**
  - The data here indicate with single TX FIR setting can satisfy eye opening from min-max channel loss
  - The penalty associated with fix TX FIR is low enough (<0.5 dB) that we can greatly simplify the module-ASIC bring up and operation
- **For Lim and Yamaichi MCB/HCB if one constructs module-ASIC link the COM at slicer can be as low as 1.7 dB with 4T DFE due to short package reflection, which is similar to what has been observed on the ASIC-Module direction**
  - ASIC SerDes either would have to operate with as high as 15.6 dB VEC or may additional capability to deal with short package/channel reflections penalty.