100GBASE-KR1/CR1 AN Direction

IEEE P802.3ck

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Introduction

- A dual FEC strategy was adopted for 100GBASE-CR1/KR1 at the November Plenary:

  Move to adopt clause 82 as the PCS, a dual FEC strategy based on gustlin_3ck_01_0719 (but with CL91 as the default FEC and the remaining AN TBD), and clause 135 as the PMA for the 100GBASE-CR1 and 100GBASE-KR1 PHYs.

  Y:48 N:0 A: 13

- We now need to close on the AN strategy

AN High Level Operation

- Technology Ability bit A22 is made into FEC request (F4) bit for 100G-CR1/KR1
  - Leaves A19,A20,A21 unused in BasePage
- F4 is then used negotiate between two operating modes
  - FEC mode default is currently non interleaved (Clause 91)
  - F4 is a request to use the non-default operating mode

FEC AN Resolution Options

- Default FEC is Clause 91 (non Interleaved)
- Options for negotiation (assuming no ability bit):

A. If either side requests Interleaved (clause 161), use interleaved FEC
   - It is mandatory to implement Interleaved in both TX and RX directions
   - Larger burden but most robust option

B. If both sides requests Interleaved (clause 161), use interleaved FEC
   - Interleaved could be considered as optional to implement
   - Least burden but less robust

C. FEC is decided by the RX per direction, request what you want for your RX
   - We can have different FEC schemes per direction
   - Each side must implement interleaved in the TX direction, RX is optional to implement interleaved
   - Compromise on burden, asymmetric operational mode

FEC AN Resolution Options

Option	A	B	C
Mode – who determines Interleaved usage	Either	Both	Each Receiver
FEC Robustness	Higher	Lower	Higher
What must be implemented for Interleaved?	TX + RX	Optional	TX
Symmetric operation	Yes	Yes	No
Implementation burden	Highest	Lowest	In between

Preferred Option

- We believe that we should choose option A.

Option	A	B	C
Mode – who determines Interleaved usage	Either	Both	Each Receiver
FEC Robustness	Higher	Lower	Higher
What must be implemented for Interleaved?	TX + RX	Optional	TX
Symmetric operation	Yes	Yes	No
Implementation burden	Highest	Lowest	In between

Proposed Changes (non Clause 73)

- Changes assume Option A

30.5.1.1.16 aFECmode -- add RS-FEC Interleave

30.6.1.1.5 aAutoNegLocalTechnologyAbility -- add RS-FEC interleave

Table 45-88 Add RS-FEC Interleave Enable bit

45.2.1.110.a 100G RS-FEC Interleave Enable
This bit enables RS-FEC interleave mode for PHYs that support 100G-RS-FEC Interleave Operation....

Table 45–318a set bit 6 as RS-FEC-Int negotiated

Proposed Changes (Clause 73)

Figure 73-4 Update diagram to change A22 to F4

73.6.4 Technology Ability Field
Technology Ability Field (A[21:0]) is a 22-bit wide field containing

Table 73-4 (change A22 to A21)

73.6.5 FEC capability
FEC (F4, F2, F3, F0, F1) is encoded in bits D43:D47 of the base link codeword. The five FEC bits are used as follows:
a) F0 is 10 Gb/s per lane FEC ability
b) F1 is 10 Gb/s per lane FEC requested
c) F2 is 25G RS-FEC requested
d) F3 is 25G BASE-R FEC requested
e) F4 is 100G RS-FEC-Int requested

~~Bits F2 and F3 are used for resolving FEC operation for 25G PHYs, while bits F0 and F1 are used for 10 Gb/s per lane operation. Bits F0 and F1 are not used for 25G PHYs.~~

73.6.5.a FEC Resolution for 100G PHYs

For 100GBASE-P PHYs which support RS-FEC-Int the F4 field is used to negotiate which FEC operating mode is used. If one or both sides request RS-FEC-Int operation then RS-FEC-Int operation is enabled.

73.6.5.3 FEC control variables
after the 2nd paragraph insert the following new paragraph
"The variable an_rsfec_int_negotiated control indicates that RS-FEC-Int operations has been negotiated. If the value is false, then RS-FEC-Int has not been negotiated. If the value is true, then RS-FEC-Int has been negotiated.

Table 73-6 add an_rsfec_int_negotiated entry mapped to 7.49.6

PICS LE10 delete the words "based on F0 and F1 bits" from the description.

Thanks!