

C2M Methodology and Limits at TP1a, TP4, and TP5

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IEEE 802.3ck Task Force

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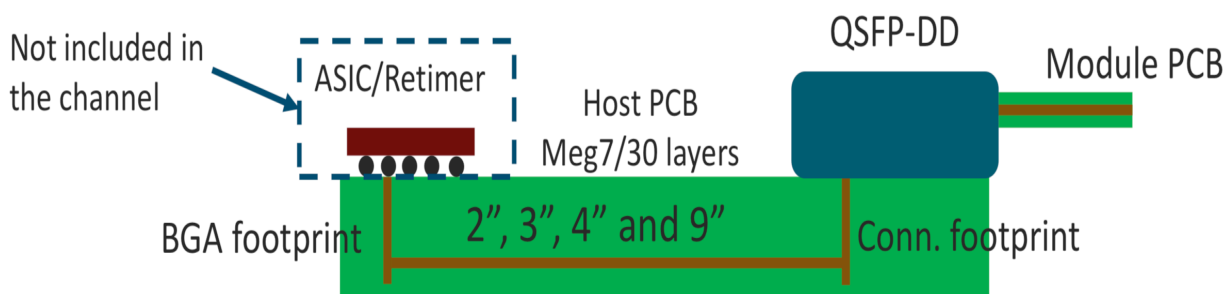
Overview

- ❑ **Updated analysis is with COM 2.7.6**
 - This analysis uses updated [lim_3ck_adhoc_02_073119](#) channels
 - COM analysis at TP1a/Slicer Lim channels
- ❑ **DFE tap weight and its impact on burst error**
- ❑ **4T DFE fails on some of the agreed channel that must pass**
 - Adding Noise only makes COM worse
- ❑ **Proposed test methodology at module output:**
 - Measure TP4 without C0/C1
 - Measure TP5 with addition of C0/C1
- ❑ **Addressing comments 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 112, 113, 114.**

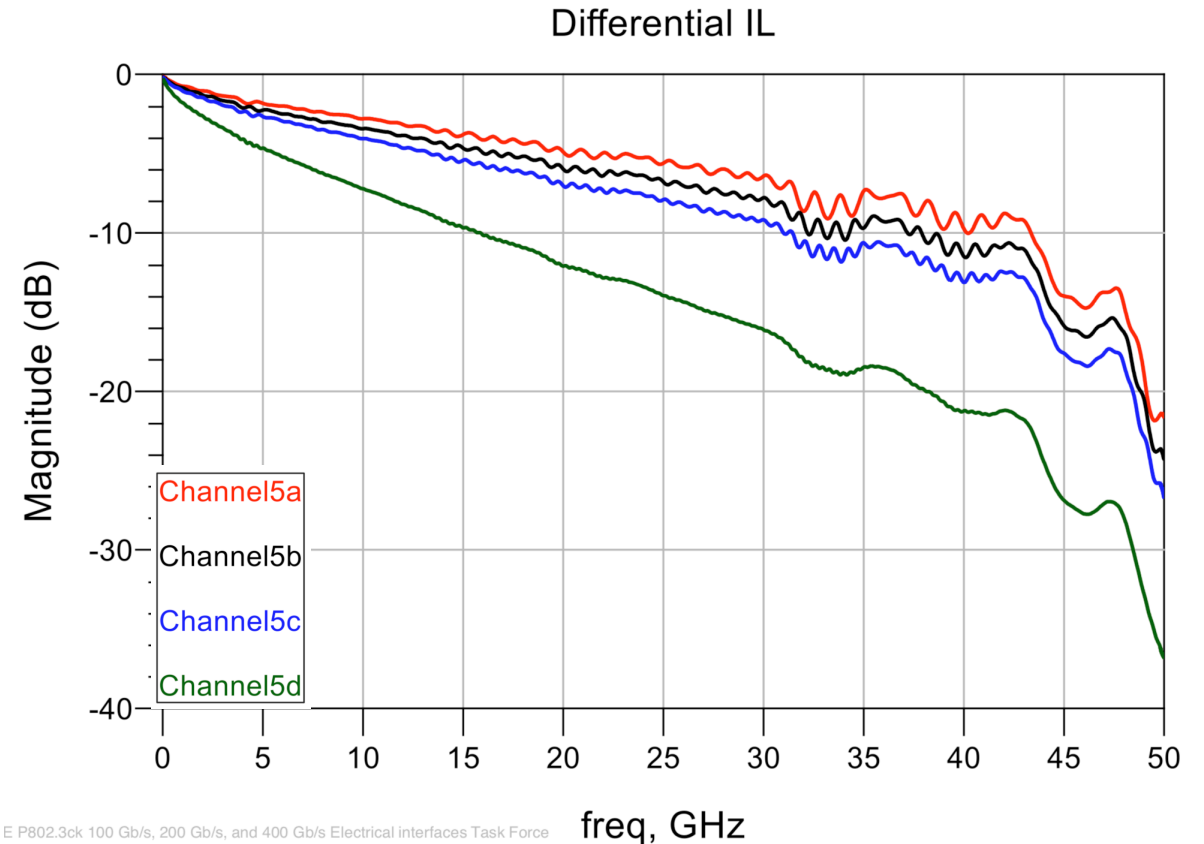
C2M Channels for Updated Analysis

Channel based on [lim_3ck_adhoc_02_073119](#) as shown

- 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
- PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
- PCB via stub length is modeled as 10 mils
- Diff pair trace width/spacing is 4.5 mils /8.5 mils
- ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.



This analysis uses min loss channel 5a and max loss channel 5d.



E P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical interfaces Task Force

COM Code 2.76 Host-Module TP1a

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.1	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nF	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.65		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0.3		
b_max(2..N_b)	0.1		
g_DC	[-14:1:-4]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:-1]		[min:step:max]
f_HP_PZ	1.3275	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	4	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.15		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	2.3407E+09	
rho_x	0.19	
fixture delay time	[0 0]	port1 port2]
TDR_W_TXPKG	1	
N_bx	4	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.2E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

18.5534591
 CTLE Config
 For FFE

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	Units
board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	68	mm
z_bp (NEXT)	68	mm
z_bp (FEXT)	68	mm
z_bp (RX)	0	mm
Include PCB	0	logical
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	2	taps per group
N_f	12	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.825	GHz
A_ft	0.410	V
A_nt	0.600	V
heck_3ck_03b_0319	Adopted Mar 2019	kasapi_3ck_02_1119
walker_3ck_01d_0719	Adopted July 2019	Adopted Nov 2019
result of R_d=50		under consideration
benartsi_3ck_01a_0719	no used for KR	
mellitz_3ck_03_0919		

COM Code 2.76 Host-Module Slicer Input

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.1	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1e-4]	nF	[TX RX]
L_s	[0.12 0.12]	nF	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[6 6; 0 0]	mm	[test cases]
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.65		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	2	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-4]	dB	[min:step:max]
f_z	12.5	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:-1]		[min:step:max]
f_HP_PZ	1.3275	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.35		
ffe_post_tap1_max	0.35		
ffe_tapn_max	0.2		
ffe_backoff	1		

I/O control		
DIAGNOSTICS	1	logical
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RESULT_DIR	.\results\100GEL_WG_(date)\	
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ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	2.3407E+09	
rho_x	0.19	
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TDR_W_TXPKG	1	
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RX_CALIBRATION	0	logical
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Noise, jitter		
sigma RJ	0.01	UI
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board_tl_tau	5.790E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	215	mm
z_bp (NEXT)	215	mm
z_bp (FEXT)	215	mm
z_bp (RX)	0	mm
Include PCB	0	logical
Floating Tap Control		
N_bg	1	0 1 2 or 3 groups
N_bf	2	taps per group
N_f	12	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps
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COM Analysis on Lim Channel 1 and 4 – ASIC to Module

□ Include BGA foot print+(mid length via)+ 2” or 9” host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB

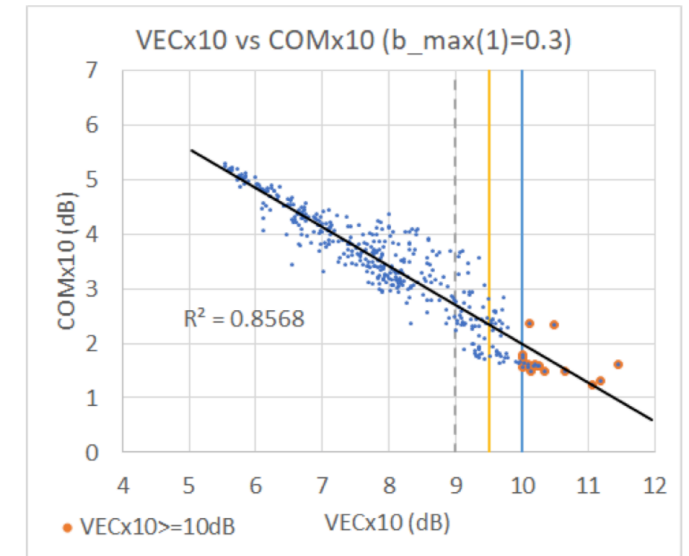
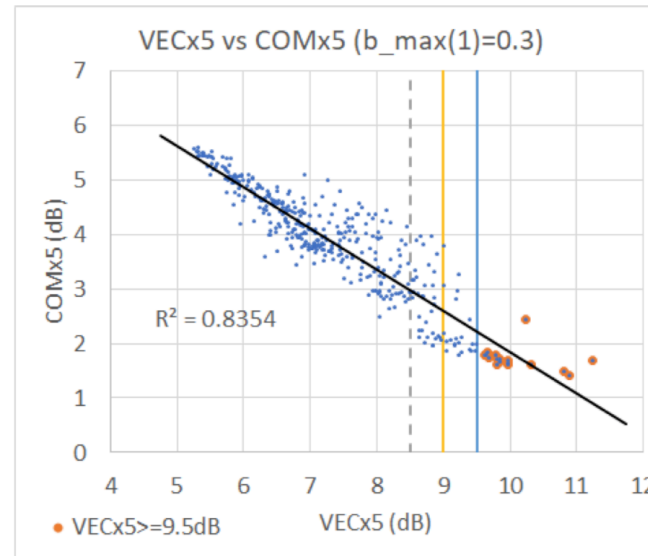
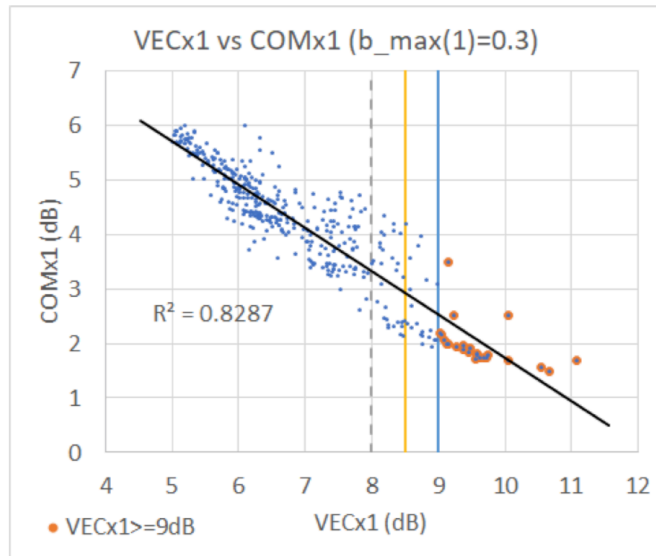
- DFE B1max<0.3, B2-B4<0.08 at TP1a
- DFE B1max at slicer 0.46.

Channel	Equalizer	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II	VEC Case I/II	EW Case I/II	COM Case I/II
Lim Channel 2” at TP1a FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	12.5 dB	21.4/31.3	11.5/6.0	0.156/0.219	2.7/6.0
	4T DFE	5.9 dB	12.5 dB	27.4/38.8	11.4/6.5	0.063/0.187	2.7/5.5
	2T+2T 12UI DFE	5.9 dB	12.5 dB	43.7/39.9	7.5/6.5	0.125/0./187	4.8/5.6
	12T FFE	5.9 dB	12.5 dB	48.4/32.3	5.4/5.8	0.219/0.219	6.6/6.3
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	14.5 dB	11.0/28.8	15.7/8.1	0.125/0.188	1.6/4.3
	4T DFE	5.9 dB	14.5 dB	18.7/27.5	14.2/8.9	0.062/0.156	1.9/3.9
	2T+2T 12UI DFE	5.9 dB	14.5 dB	30.3/29.3	10.0/8.4	0.094/0.156	3.3/4.2
	12T FFE	5.9 dB	14.5 dB	28.4/23.7	7.7/7.8	0.188/0.188	4.6/4.5
Lim Channel 9” at TP1a FOM ILD = 0.13 ICN = 1.44 mV ERL11=16 dB ERL22=11.3 dB	5T FFE	14.8	21.4	11.3/13.9	10.8/6.5	0.125/0.187	3.0/5.5
	4T DFE	14.8	21.4	18.2/18.9	8.2/6.4	0.125/0.187	4.3/5.7
	2T+2T 12UI DFE	14.8	21.4	23.7/18.9	6.1/6.4	0.156/0.187	6.0/5.7
	12T FFE	14.8	21.4	19.1/13.2	5.3/6.2	0.219/0.187	6.8/5.8
Lim Channel 9” At Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=16.0 dB ERL22=11.3 dB	5T FFE	14.8	23.2	7.2/10.9	12.3/7.3	0.094/0.188	2.4/4.9
	4T DFE	14.8	23.2	16.9/15.6	8.6/7.2	0.125/0.156	4.0/5.0
	2T+2T 12UI DFE	14.8	23.2	21.5/17.0	6.9/6.9	0.125/0.156	5.3/5.2
	12T FFE	14.8	23.2	14.9/12.7	6.3/6.8	0.188/0.188	5.8/5.3

How to Deal with Short Channel with High VEC

□ Lim 073119 2" channels has a VEC of 12.3 dB with 4T DFE

- Lim channel are representative of actual implementation and has been agreed the standard must support
- Hidaka [hidaka_3ck_adhoc_01_021920](#) investigated VEC at TP1a with 1x ($\eta_0=0.82e-8$), 5x, and 10x noise
 - Increasing η_0 also increases VEC limit even higher (+ 1dB) and only marginally improves the correlation



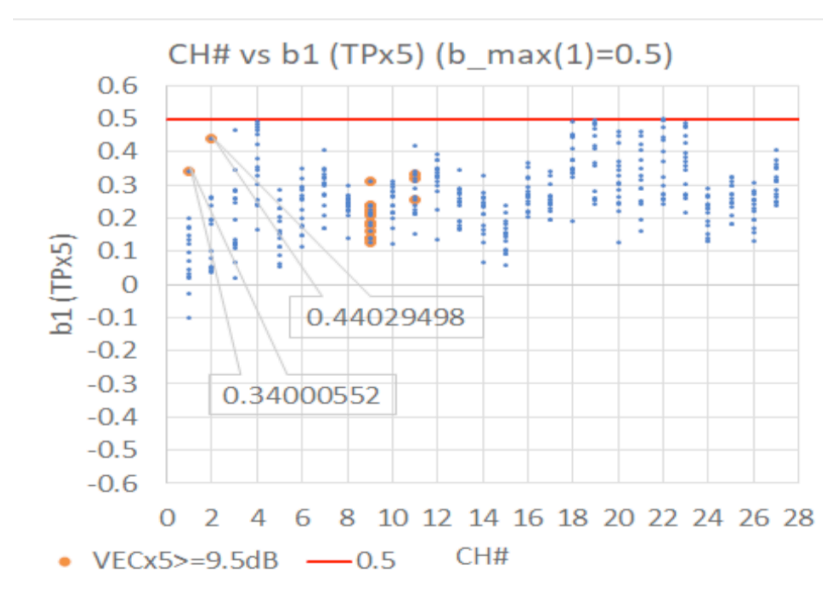
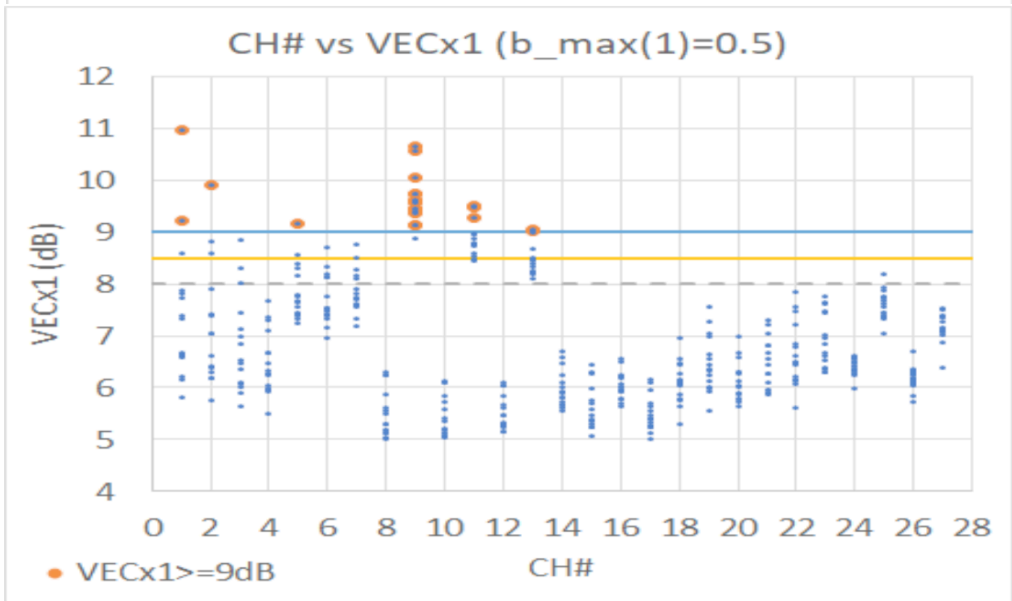
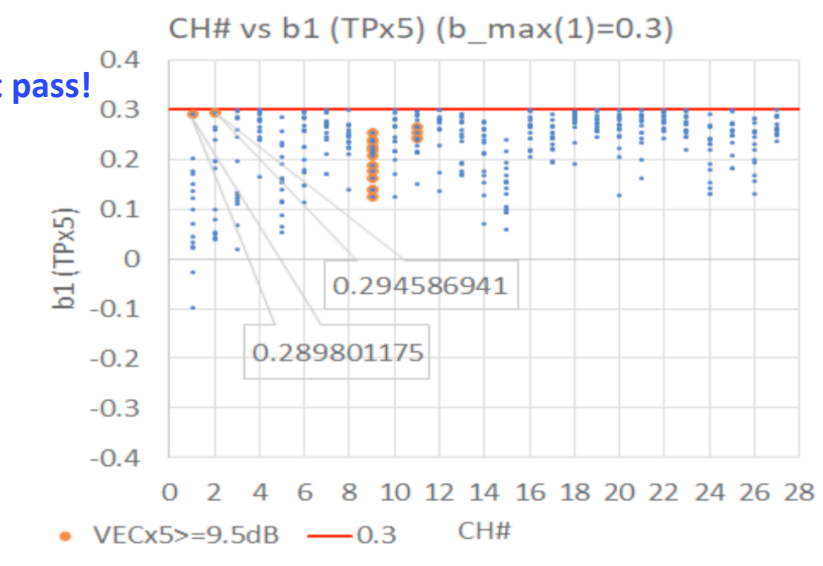
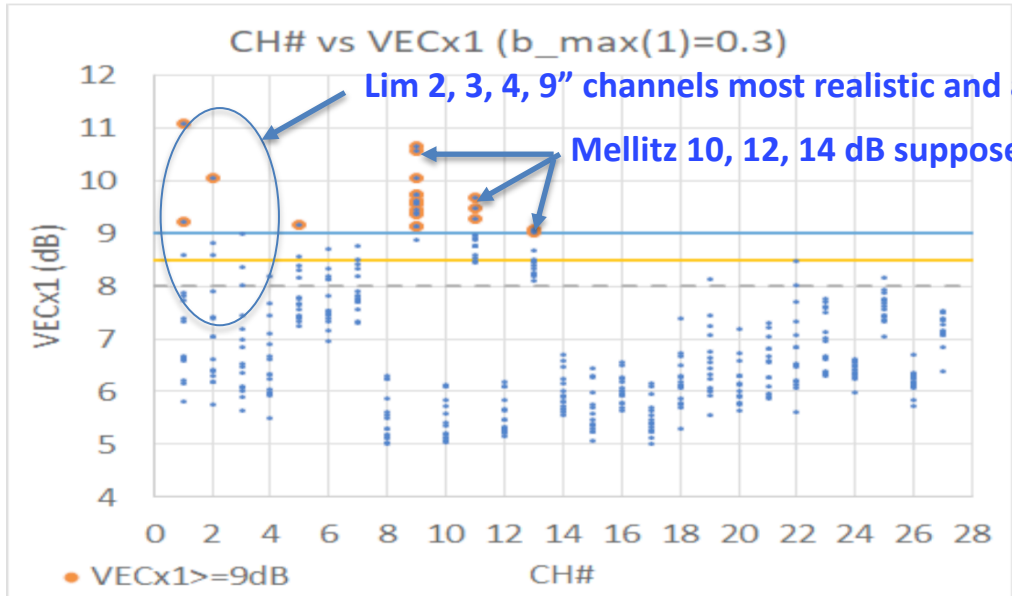
- Adding some noise to simplify scope measurement is reasonable but doesn't address how the receiver will operate with 14+ dB VEC and COM < 1.9 dB!

How to Deal with Short Channel with High VEC, cont.

- **Assuming we are not throwing out Lim 073119 2” channels we have the following options:**
 - Build a super duper 4T DFE receiver that will deliver the target BER when COM is only 1.8 dB
 - Alternatively leverage 2T DFE + 2T floating DFE with 12 UI span
 - This test will qualify and make sure post-cursors are contained to 12 UI but actual implementation doesn't have to be a 12T floating DFE
- **How would it work:**
 - Test TP1a with 4T DFE if the $VEC \leq 10$ dB – channel passes
 - Test TP1a with 4T DFE if the $VEC > 12.5$ dB – channel fails
 - Test TP1a with 4T DFE if the $10.0 < VEC \leq 12.5$ dB – channel is tested with 2T DFE + 2T floating DFE with span of 12 UI
 - If $VEC \leq 10$ dB with floating DFE then – channel passes
 - The floating DFE test is only to quantify the post cursors but actual implementation may one of:
 - Chip scale /improved packaging
 - A receiver with lower noise/better slicer and timing that can operate with 1.8 dB COM
 - A more capable 4T equalizer but short of KR equalizer.

Hidaka Results Show no real difference in VEC Increasing b1_max to 0.5 at TP1a

See http://www.ieee802.org/3/ck/public/adhoc/feb19_20/hidaka_3ck_adhoc_01_021920.pdf

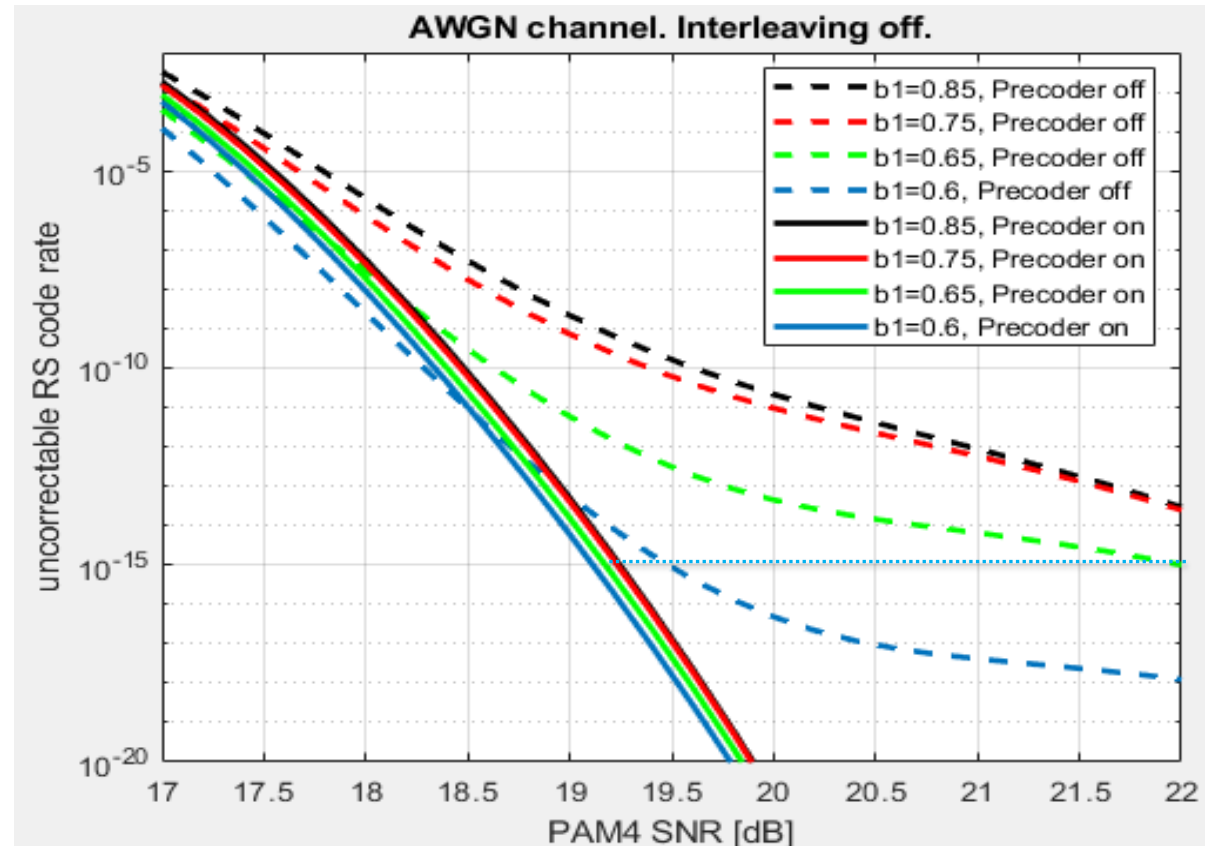
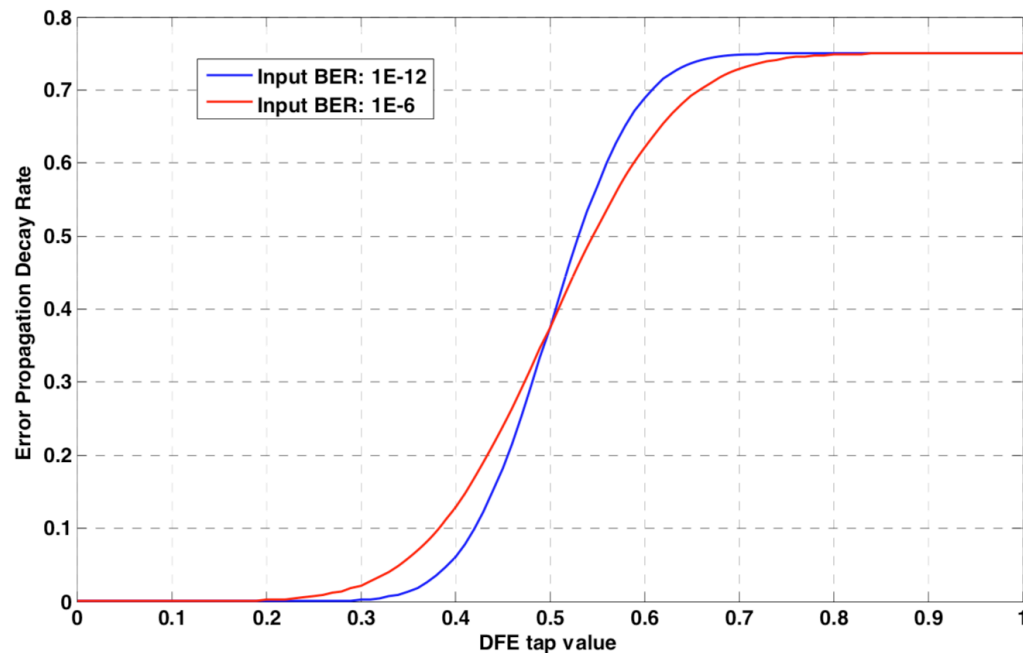


SNR Penalty Due to DFE Burst Errors

□ Pre-coder off and assumes $B(2,3,4)=0$

- With DFE error decay nearly constant for $B_{1max} > 0.6$, increasing B_{1max} will only reduce overall link SNR
- Given that B_{1max} slicer is about 1.5x larger than B_{1max} at TP1a, B_{1max} at TP1a needs to be < 0.4
- Pushing $B_{1max}=0.5$ at TP1a may result in B_{1max} at slicer of ~ 0.75 with ~ 2.5 dB of burst SNR penalty.

http://www.ieee802.org/3/bj/public/sep11/parthasarathy_01_0911.pdf



Multi-Segment Link Penalty

□ [anslow_01_0815_logic](#)
analysis for one CWD
with $a=0.75$ the electrical
link segment Pre-FEC
 $BER \leq 2.9E-7$

- With $a=0.5$ the pre-FEC BER= $1.6E-5$ inline with current C2M BER of $1E-5$
- $a=0.75$ can't be supported by C2M unless pre-BER is reduced to $2.9E-7$!

The BER of the electrical sub-links for a penalty of ~ 0.1 dB optical in the optical sub-link are shown in the table below.

	At slicer output for FLR = $6.2E-11$			
	Total electrical		Optical	
Same cwd (1), $a = 0.75$	Burst	$2.9E-7^*$	Random	$2.4E-4$
Same cwd, symbol interleave (2), $a = 0.75$	Burst	$7.5E-7^*$	Random	$2.4E-4$
Same cwd (1), $a = 0.5$	Burst	$1.6E-5^*$	Random	$2.4E-4$
1:4 Pre-interleaved (4), $a=0.75$	Burst	$2.2E-5^*$	Random	$2.4E-4$
1:2 Pre-interleaved (8), $a=0.75$	Burst	$3.5E-5^*$	Random	$2.4E-4$
Diff cwd (FOM) (7), $a = 0.75$	Burst	$4E-5^*$	Random	$2.4E-4$
Same cwd elec only precoded, $a=0.75$	Burst	$5.1E-5^*$	Random	$2.4E-4$
Same cwd end-to-end precoded, $a=0.75$	Burst	$6.9E-5^*$	Random	$4.9E-5$
1:4 Pre-interleaved (6), $a=0.75$	Burst	$5.7E-5^*$	Random	$2.4E-4$
1:2 Pre-int, sym mux (10), $a=0.75$	Burst	$7.6E-5^*$	Random	$2.4E-4$
1:4 Pre-int, sym mux (9), $a=0.75$	Burst	$1E-4^*$	Random	$2.4E-4$
Random errors	Random	$8.2E-5$	Random	$2.4E-4$

Note – these values are the BER **including** the additional errors due to the bursts. To account for burst errors, the values marked with “*” have been multiplied by 4 when $a = 0.75$ and 2 when $a = 0.5$.

TP4 and TP5 Test Methodology

TP4/TP5 measurements are with addition of 0.577 nV²/GHz (TBD) noise to account for BGA crosstalk

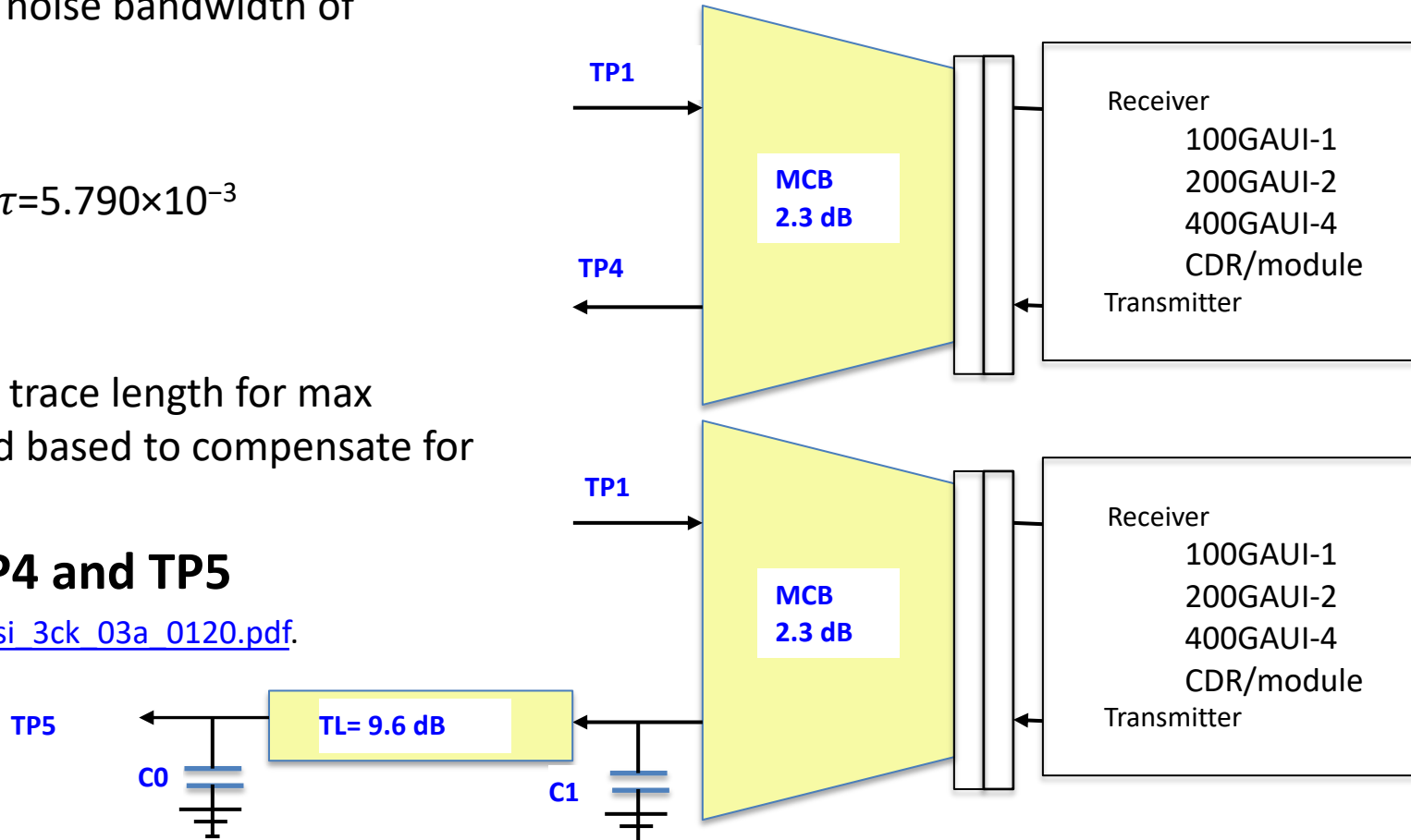
- The equivalent 0.577 mV RMS noise is for noise bandwidth of $53.125 \times 0.75 = 39.84$ GHz

Transmission line parameters

- $\gamma_0=0$, $a_1 = 3.8206 \times 10^{-4}$, $a_2 = 9.5909 \times 10^{-5}$, $\tau = 5.790 \times 10^{-3}$
- TP4 is MCB output measurement
- TP4 is measured at MCB output
- TP5 is measured with addition of 244 mm trace length for max channel loss (trace length may be adjusted based to compensate for MCB loss deviation from 2.3 dB)

Single module TX setting can meet TP4 and TP5

- See http://www.ieee802.org/3/ck/public/20_01/ghiasi_3ck_03a_0120.pdf.



TP1a, TP4, and TP5 Specifications

□ Recommended host TP1a limits:

— TP1a

- $VEC \leq 9.5$ dB (VEO/VEC doesn't support 2" Lim channels unless VEO/VEC mask reconsidered or post-cursor span quantified)
- $VEO \geq 15$ mV (VEO/VEC doesn't support 2" Lim channels unless VEO/VEC mask reconsidered or post-cursor span quantified)
- $EW \geq 0.15$ UI
- Initial proposed $B1(\max) \leq 0.3$ and $B[2-4] \leq 0.08$ (expected $B1\max$ at slicer ~ 0.5)
- New proposed limits after consultation with P. Sun and Y. Hadaka $B1(\max) \leq 0.4$ and $B[2-4] \leq 0.15$ ($B1\max$ at slicer ~ 0.6)
- Recommend to go with $\eta_0 = 4.1e-8$ as suggested by [hidaka_3ck_adhoc_01_021920](#).

□ Recommended Module TP4/TP5 limits:

— TP4

- $VEC \leq 7.0$ dB
- $VEO \geq 50$ mV
- $EW \geq 0.175$ UI
- $B1(\max) \leq 0.15$ and $B[2-4] \leq 0.05$

— TP5

- $VEC \leq 7.0$ dB
- $VEO \geq 20$ mV
- $EW \geq 0.175$ UI
- $B1(\max) \leq 0.3$ and $B[2-4] \leq 0.1$ (the expected $B1\max$ at slicer would be ~ 0.6).

CTLE Gains

□ CTLE tap weights allowed at TP1a, TP4, TP5

- Reduces # of CTLE setting to 24 for TP1a and less at TP4/TP5.

CTLE HF (dB)	CTLE LF (dB)	TP1a	TP5	TP4
2	0, 1	✓	✓	✓
3	0, 1	✓	✓	✓
4	0, 1	✓	✓	✓
4	1, 2	✓	✓	✓
5	1, 2	✓	✓	✓
6	1, 2	✓	✓	-
7	1, 2	✓	✓	-
8	2, 3	✓	✓	-
9	2, 3	✓	✓	-
10	2, 3	✓	✓	-
11	2, 3	✓	-	-
12	3	✓	-	-
13	3	✓	-	-

Summary

- ❑ **For Lim and Yamaichi MCB/HCB end-end link with COM as low as 1.7 dB and VEC >14.5 dB a conventional 4T DFE receiver may not be sufficient – adding noise is not the answer**
 - One would need a 4T DFE with much better PKG/noise/timing such that it can work with 1.7 dB COM
 - Such equalizer may/or may not be realizable or at least mass producible
 - [dudek_3ck_adhoc_01_030420](#) has suggested one would a receiver not needing 3 dB COM, use stronger equalizer, use better package, lower frontend noise
 - Use of better package and lower noise is one option where the receiver may operate with 1.7 dB COM
 - Unless the post-cursor span is quantified no one knows how powerful/long an equalizer is needed
 - The 4T DFE with floating (2T DFE+2T floating DFE with 12T) is a method to quantify the post cursor but actual CDR implementation may use more powerful equalizer, improve package, and/or improve noise/timing.
- ❑ **Module output measurements**
 - TP4 measured directly
 - TP5 measured with addition of addition of CR (C0, C1) caps + ~244 mm trace
- ❑ **Module TX FIR is set for a nominal setting such that both TP4 and TP5 limits are met**
 - The data here indicate with single TX FIR setting can satisfy eye opening from min-max channel loss
 - The penalty associated with fix TX FIR is low enough (<0.5 dB) that we can greatly simplify the module-ASIC bring up and operation.