# Comment #42 Resolution

**IEEE P802.3ck**

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# Introduction

- In an effort to close comment #42, we are providing a more detailed possible resolution
  - This only applies to Clause 161, not proposing to add it to other FEC clauses

- Comr

*Cl* **161** *SC* **161.6** *P* **123** *L* **3** # 42

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*Comment Type* **T** *Comment Status* **D**

FEC histogram counter are very useful for understanding the performance of an interface. Add in optional histogram counters for the RS-FEC decoder.

*SuggestedRemedy*

Add into the RS-FEC-Int MDIO function mapping the following registers: RS-FEC symbol error per codeword 1 through RS-FEC symbol error per codeword 15 (a total of 15 registers). 32b each. Each counter counts the number of codewords that contain that specific number of errors. Also add an RS-FEC codeword counter that counts all of the codewords that are received (errored or not), also 32 bits. Note that each of these counters counts all codewords or symbol errors from both interleaved codewords, we do no break these out by interleaved instance.

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

# Clause 161 Possible Resolution

**Table 161–2—MDIO/RS-FEC-Int status variable mapping§**

| MDIO control variable§ | PMA/PMD register name§ | Register/bit number§ | FEC variable§ |
|---|---|---|---|
| FEC AM lock *x*, *x*=0 to 3§ | RS-FEC status register§ | 1.201.8:11§ | amps_lock<*x*>§ |
| RS-FEC align status§ | RS-FEC status register§ | 1.201.14§ | fec_align_status§ |
| FEC corrected codewords§ | RS-FEC corrected codewords counter register§ | 1.202, 1.203§ | FEC_corrected_cw_counter§ |
| FEC uncorrected codewords§ | RS-FEC uncorrected codewords counter register§ | 1.204, 1.205§ | FEC_uncorrected_cw_counter§ |
| FEC lane *x* mapping§ | RS-FEC lane mapping register§ | 1.206§ | FEC_lane_mapping<*x*>§ |
| FEC symbol errors, FEC lanes 0 to 3§ | RS-FEC symbol error counter register, FEC lanes 0 to 3§ | 1.210 to 1.217§ | FEC_symbol_error_counter_*i*§ |
| FEC degraded SER ability § | RS-FEC status register§ | 1.201.3 § | FEC_degraded_SER_ability§ |
| FEC degraded SER § | RS-FEC status register§ | 1.201.4§ | FEC_degraded_SER§ |
| FEC codeword counter§ | RS-FEC codeword counter register§ | 1.284§ | FEC_cw_counter§ |
| FEC codeword error bin counter, 1 to 15§ | RS-FEC codeword error bin counter register§ | 1.285 to 1.299§ | FEC_codeword_error_bin_*i*§ |

# Clause 161 Possible Resolution cont

**161.6.22 FEC_cw_counter¶**

FEC_cw_counter is a 32-bit counter that counts once for each FEC codeword received when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.124a (1.284).¶

**161.6.23 FEC_codeword_error_bin_*i*¶**

FEC_codeword_error_bin_*i*, where i=1 to 15, are 32-bit counters. While fec_align_status is true, for each codeword received with exactly i correctable 10-bit symbol errors FEC_codeword_error_bin_*i* is incremented. For example, if a codeword has exactly 5 errored 10-bit symbols, then fec_codeword_error_bin_5 is incremented. These variables are mapped to the registers defined in 45.2.1.124b (1.285 to 1.299).¶

# Clause 45 Resolution

## 45. Management Data Input/Output (MDIO) Interface

### 45.2 MDIO Interface Registers

#### 45.2.1 PMA/PMD registers

*Change Table 45-3 as follows (unchanged rows not shown):*

**Table 45–3—PMA/PMD registers**

| Register address | Register name | Subclause |
|---|---|---|
| ... | | |
| ~~1.284 through 1.299~~ | ~~Reserved~~ | |
| 1.284 | RS-FEC codeword counter | 45.2.1.124a |
| 1.285 through 1.299 | RS-FEC codeword error bin 1 through 15 | 45.2.1.124b |
| ... | | |

# Thanks!