ERL and Parameter Recommendations (updated from mellitz_3ck_adhoc_01a_030420) for Clause 162, 163 and Annex 120F, and 120G

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Putting ERL, Return Loss, and Reflections into Perspective

Much of this is like finding faces in the clouds when all we care about is it raining or not.

Agenda

- ERL comments
  - i.e. the purpose is to resolve comments
- COM Tracking ERL
- ERL parameters recommendations
- Clause 162 COM only shows correlation to Il and not ISI
  - Recommendation: The best tact here it to set the ERL limit close to the lowest ERL for channels near 3 dB COM
- Annex 120F an 120G
  - Recommendation based on Clause 163

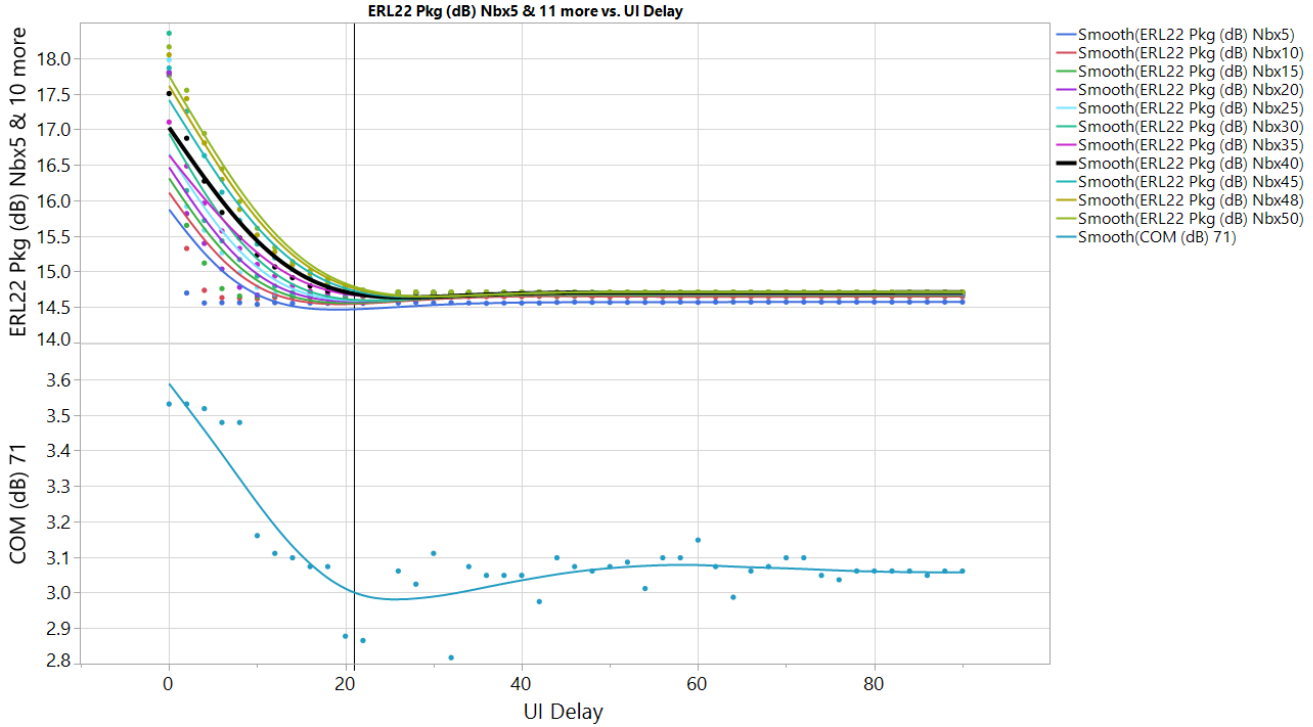
Comments and References

Clause	comment	type
162.9.3	10003	Tx Host
162.9.3.4	10009	Tx Host
162.9.4	10009	Rx Host
162.9.4.5	10011	Rx Host
162.11.3	10013	CA
162.11.3	10012	CA
163.9.1.1	10020	Tx Chip
163.9.1.1	10021	Tx Chip
163.9.2.1	10022	Rx Chip
163.10.2	10024	Channel

How Well Does COM Track ERL?

- COM tracks ERL when channel reflections are near the device transmitter or receiver.
  - ERL and COM vs. added delay track fit shapes
  - The N_{bx} parameter is related of the equalizer (DFE) reach
  - See back up for details

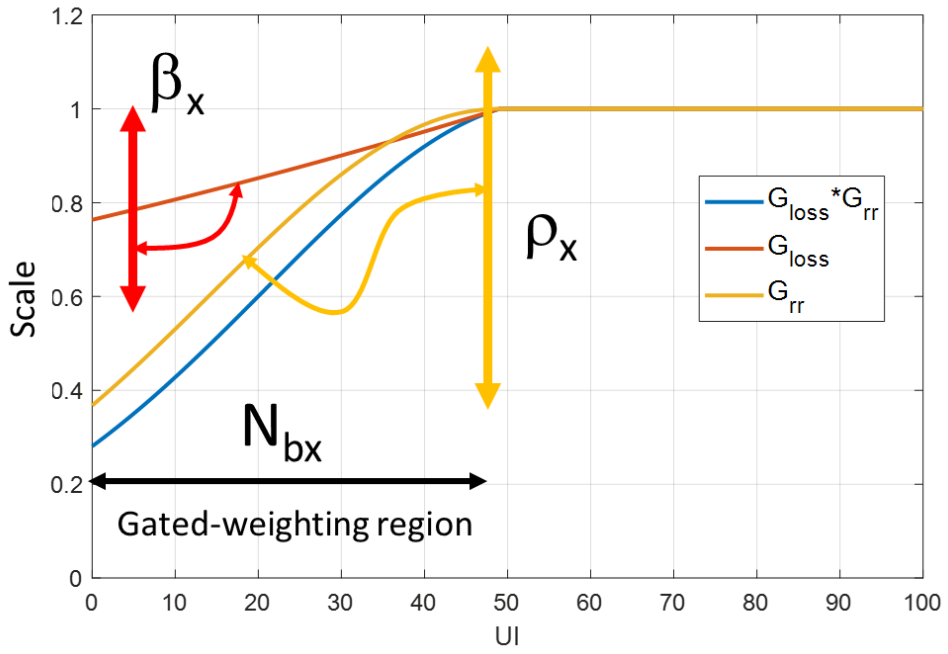
- N_{bx} is not tied to DFE reach for computed ERL when the test point in not near TP0 or TP5
  - See back up for details



Parameter Proposal

- 0 value for β_x
- 0.618 value for ρ_x

See mellitz_3ck_adhoc_01a_030420 for more details



$$G_{rr}(t) = \begin{cases} 0 & t < T_{fx} \\ \rho_x(1+\rho_x)\exp\left(-\dfrac{[(t-T_{fx})f_b-(N_{bx}+1)]^2}{(N_{bx}+1)^2}\right) & T_{fx} \le t < T_{fx}+\dfrac{N_{bx}+1}{f_b} \\ 1 & t \ge T_{fx}+\dfrac{N_b+1}{f_b} \end{cases}$$

$$G_{loss}(t) = \begin{cases} 0 & t < T_{fx} \\ 10^{\frac{\frac{\beta_x}{f_b}[(t-T_{fx})f_b-(N_{bx}+1)]}{20}} & T_{fx} \le t < T_{fx}+\dfrac{N_{bx}+1}{f_b} \\ 1 & t \ge T_{fx}+\dfrac{N_{bx}+1}{f_b} \end{cases}$$

Adopt N is based on electrical length from Mike Li

Clause/Annex	type	N
162.9.3.4	Tx Host	800
162.9.4.5	Rx Host	800
162.11.3	CA	7000
163.9.1.1	Tx Chip	200
163.9.2.1	Rx Chip	200
163.10.2	Channel	3500
120F.3.1.1	Tx Chip	200
120F.3.2.1	Rx Chip	200
120F.4.3	Channel	2000
120G.3.1.3	Host/Module	800

N_{bx} recommendations

Clause/Annex	type	N_{bx}
162.9.3.4	Tx Host	0
162.9.4.5	Rx Host	0
162.11.3	CA	0
163.9.1.1	Tx Chip	TBD
163.9.2.1	Rx Chip	TBD
163.10.2	Channel	TBD
120F.3.1.1	Tx Chip	TBD
120F.3.2.1	Rx Chip	TBD
120F.4.3	Channel	TBD
120G.3.1.3	Host/Module	0

N_{bx} suggestions to use for consistency when reporting ERL when TBD's have not been resolved

Clause/Annex	type	N_{bx}
162.9.3.4	Tx Host	0
162.9.4.5	Rx Host	0
162.11.3	CA	0
163.9.1.1	Tx Chip	35
163.9.2.1	Rx Chip	35
163.10.2	Channel	35
120F.3.1.1	Tx Chip	12
120F.3.2.1	Rx Chip	12
120F.4.3	Channel	12
120G.3.1.3	Host/Module	0

ERL/N_{bx} ~= 0.066 to 0.1 dB/N_{bx}

ERL minimum recommendations

Clause/Annex	type	ERL min (dB) at TP0a	ERL min (dB)at TP0
162.9.3.4	Tx Host	TBD	TBD
162.9.4.5	Rx Host	TBD	TBD
162.11.3	CA	NA	TBD
163.9.1.1	Tx Chip	TBD	TBD
163.9.2.1	Rx Chip	TBD	TBD
163.10.2	Channel	NA	TBD
120F.3.1.1	Tx Chip	TBD	TBD
120F.3.2.1	Rx Chip	TBD	TBD
120F.4.3	Channel	TBD	TBD
120G.3.1.3	Host/Module	TBD	TBD

Summary

- Lock down β_x an ρ_x for all clauses and annexes
- Adopt N for all clauses and annexes because electrical channel lengths are known
- Use N_{bx}= 0 for Clause 162, Annex 120G
- Keep N_{bx} = TBD in the next draft for Clause 163 and Annexes 120F and 120G
- Adopt ERL_{min} as TBD for all clause and channels
  - Confirmation and proposals from vested parties required

THANK YOU !

Backup Data

Background

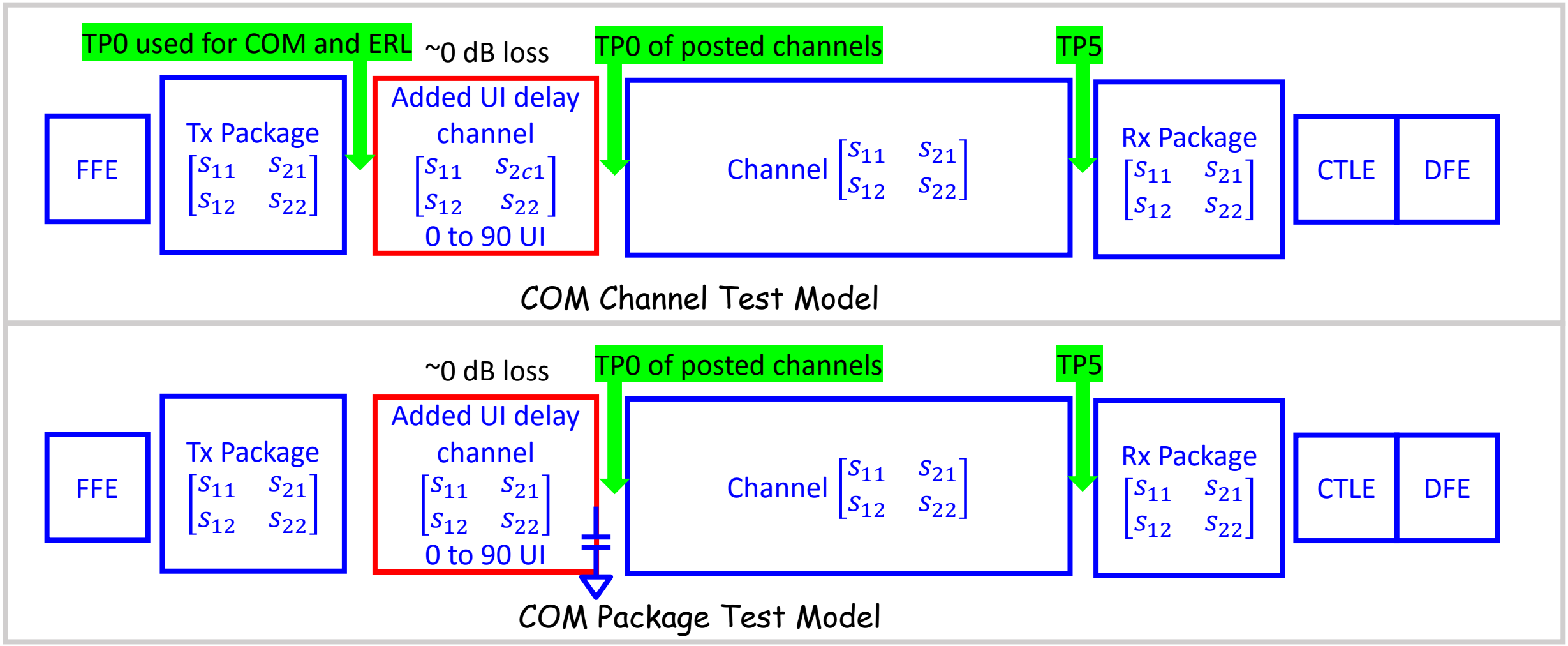
- Reviewing all the ERL presentations over the past year suggest determining simultaneously optimizing ERL parameters (β_x , ρ_x,N_{bx}) and ERL limits in the context of performance(COM or ΔCOM) for all possible channels and packages is a daunting problem
- Data also suggest single settings for ERL parameters are useful *(mellitz_3ck_adhoc_01a_030420)*
  - ERL depends on independent parameters, β_x and ρ_x
    - ERL strongly tracks ρ_x which is only weakly scaled by β_x
  - Treat ρ_x and β_x as just computational parameters and lock down for all ports
    - This simplification moves the project along
  - Then set the ERL limit accordingly
- For Clause 163 and Annex 120G DFE reach tracks COM and ERL through N_{bx}

Does ERL track ΔCOM and COM

- The answer is “It depends” ☹
- For Tx/Rx KR and C2C packages answer is yes
- For channels where reflections are near the end of the channel the answer is yes
- For all others the tracking is looser and dominated by end terminations
- The best tact here it to set the ERL limit close to the lowest ERL for channels near 3 dB COM

ERL and COM tracking for bga(tp0) to bga(tp5)

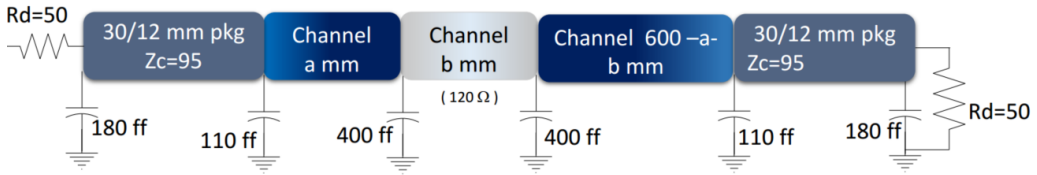
Package and Channel COM added delay experiments



Similar to ERL experiment done in mellitz_3cd_01b_1117

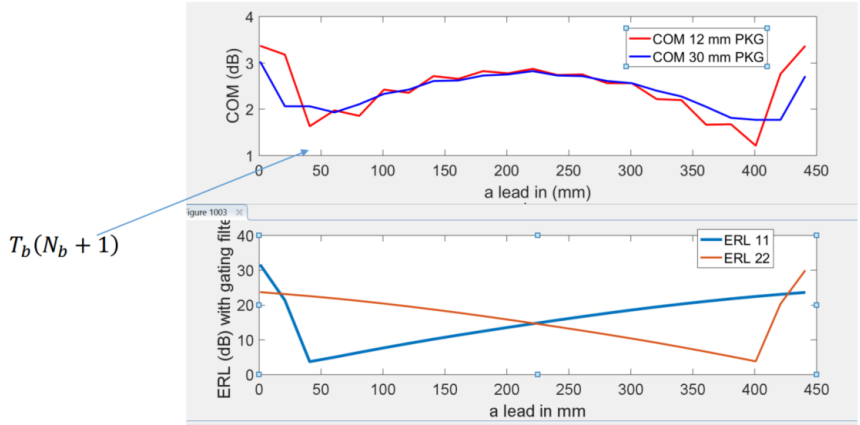
Would changing the amount of reflection alter the trends of the results?

- ❑ Change the capacitor to 400 ff from 200 ff
- ❑ Shorten the total length to 450 mm from 600 mm to keep around 3 dB of COM



mm	ff	Ω	mm	ff	mm	ff	mm	ff	mm	ff	mm	Ω	ff	Ω
30	180	95	12	110	a	400	b	400	450 -a-b	110	30	95	180	50

Similar trends regardless of reflection magnitude

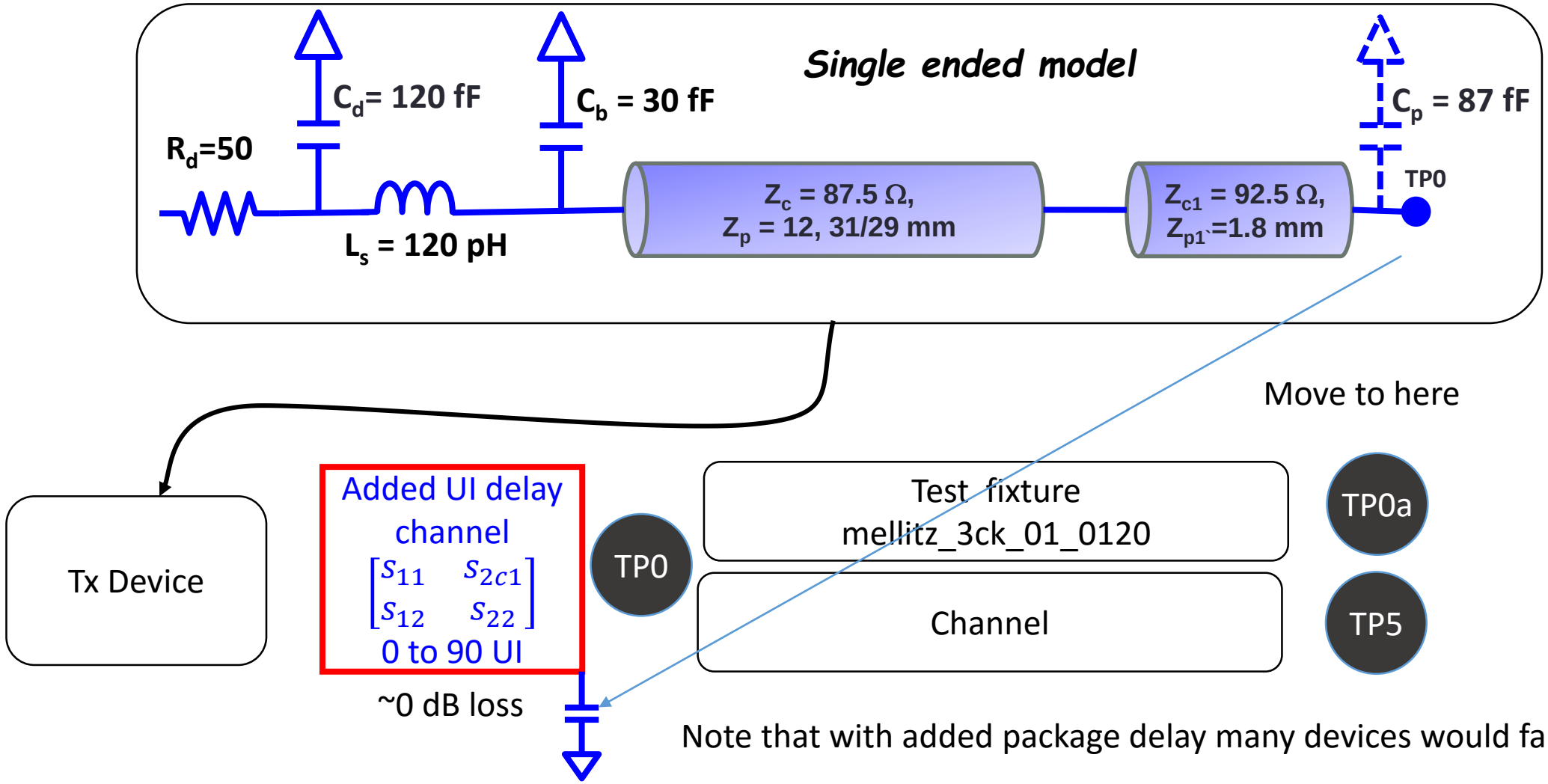


Takeaway:

- Similar effects on either end of the channel
- A key factor is the distance a channel reflection is from either Tx or Rx package

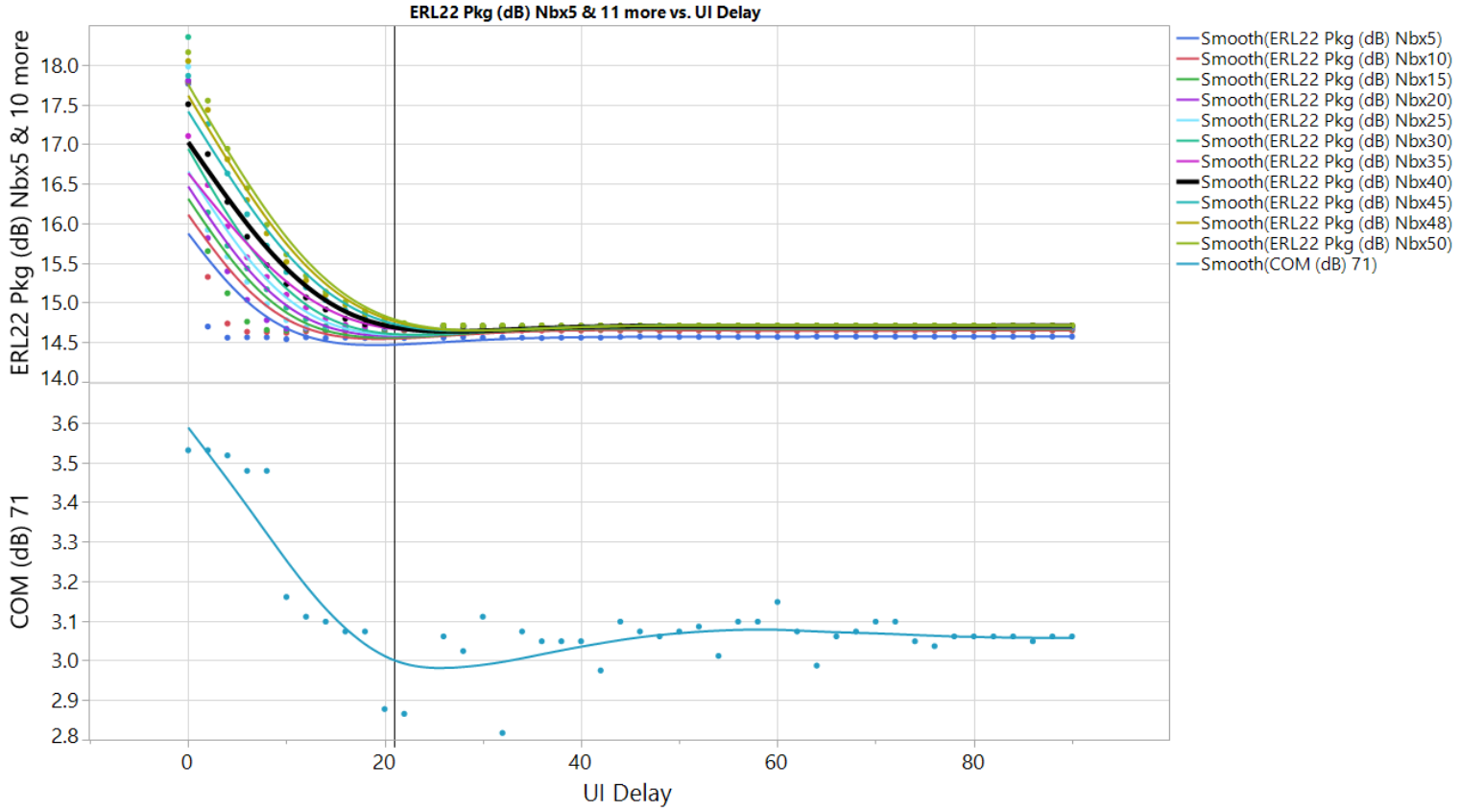
Package added delay experiment.

Use this to test the N_{bx} Hypothesis for packages



Added Package delay vs COM and ERL of package for selections of N_{bx}

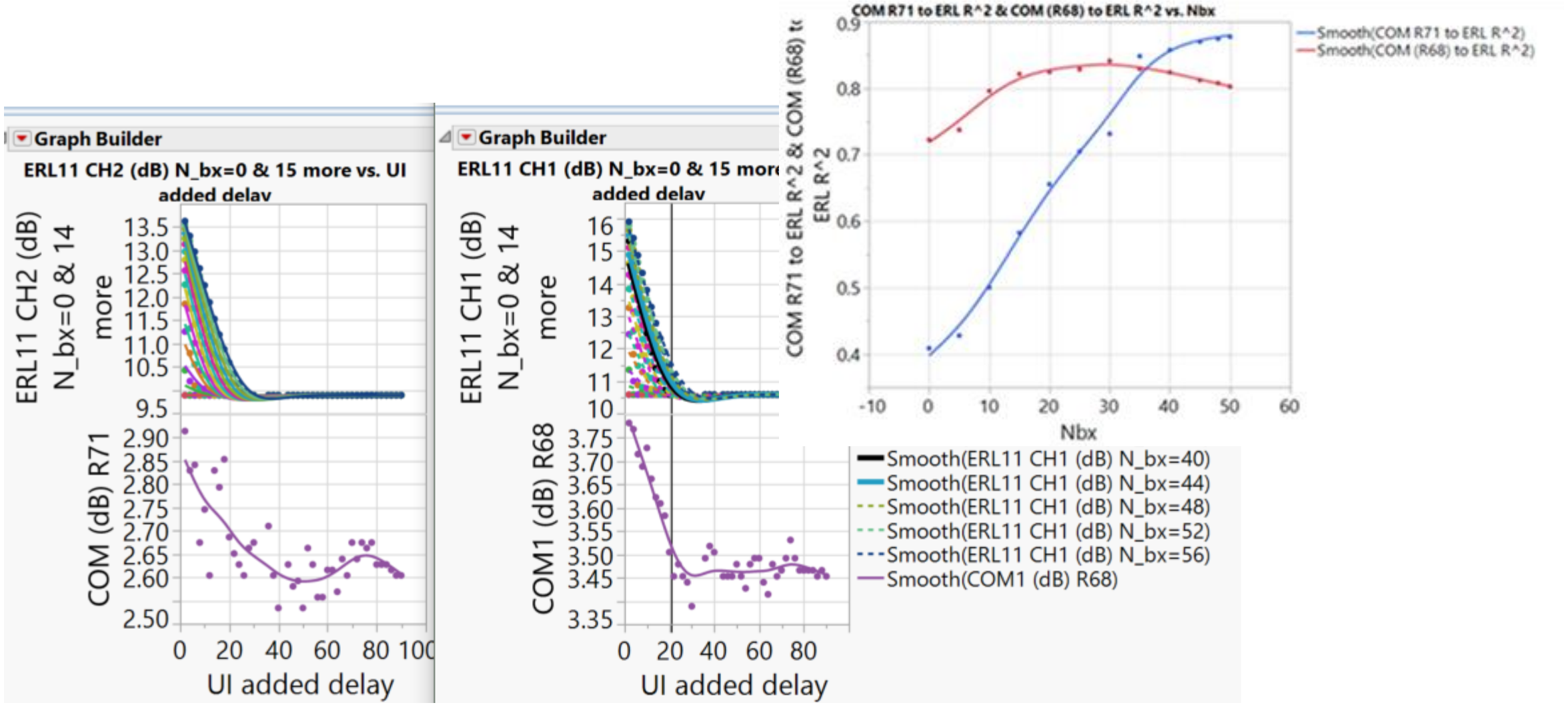
Visual estimate suggests N_{bx} should be about 42



A more pragmatic method uses R^2

- If we use all the COM values vs delay for R71 and R68. That gives me 2 vectors, COM(R#, UI (0:1:90))
- For each case (either R71 or R68) determine ERL for each delay case for a give N_{bx}, where N_{bx}= 0:2:60 (31 cases)
- For each case that results in 31 vectors of ERL vs delay ERL(R#, UI(0:1:90), N_{bx})
- R^2 is correlation for each case between COM(R#, UI (0:1:90)) and delay ERL(R#, UI(0:1:90), N_{bx})
- Then we plot R^2 vs N_{bx} for each case.
- Computation for ERL used Annex 93A.5 with β_x=0, ρ_x-0.618, and N = 2000

A more pragmatic approach place N_{bx} at 35



CL 163 Rx/Rx ERL estimate for package reference package variations

ERL and Pmax/Vf of reference package at TP0a

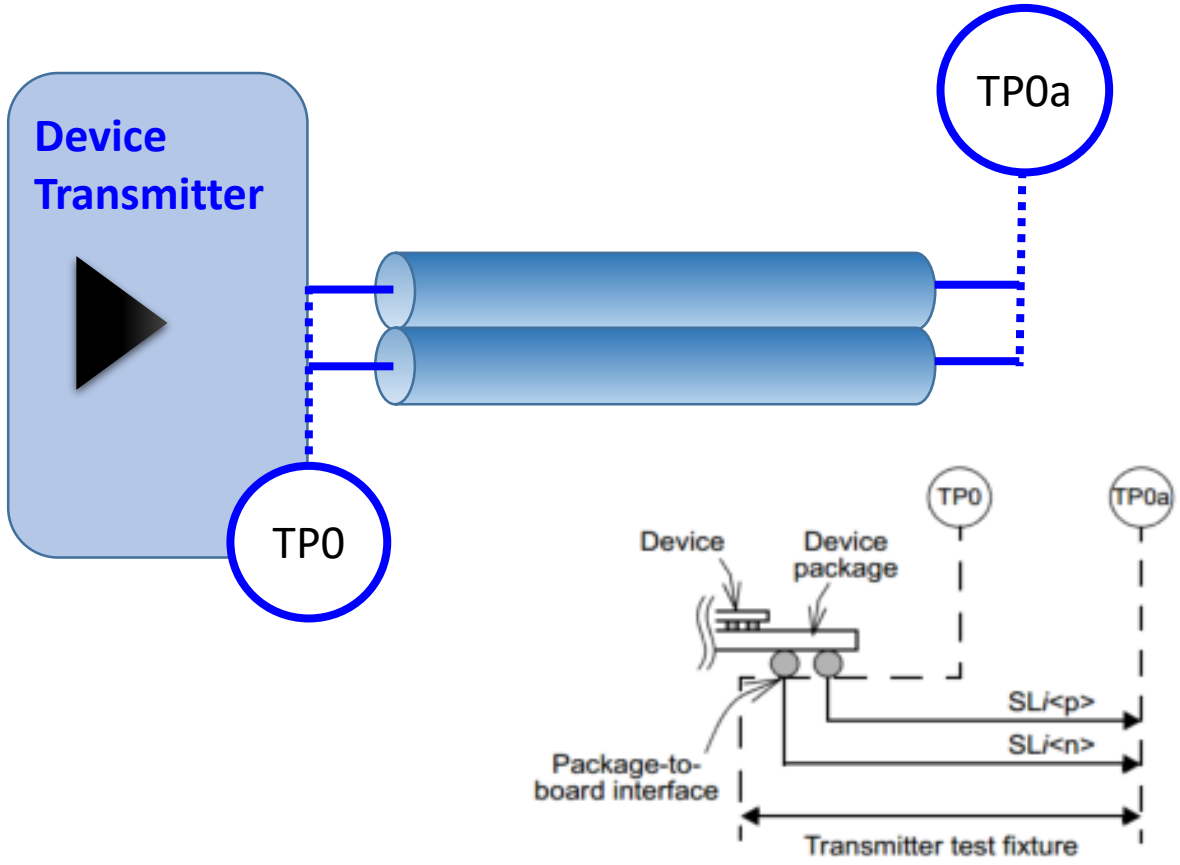
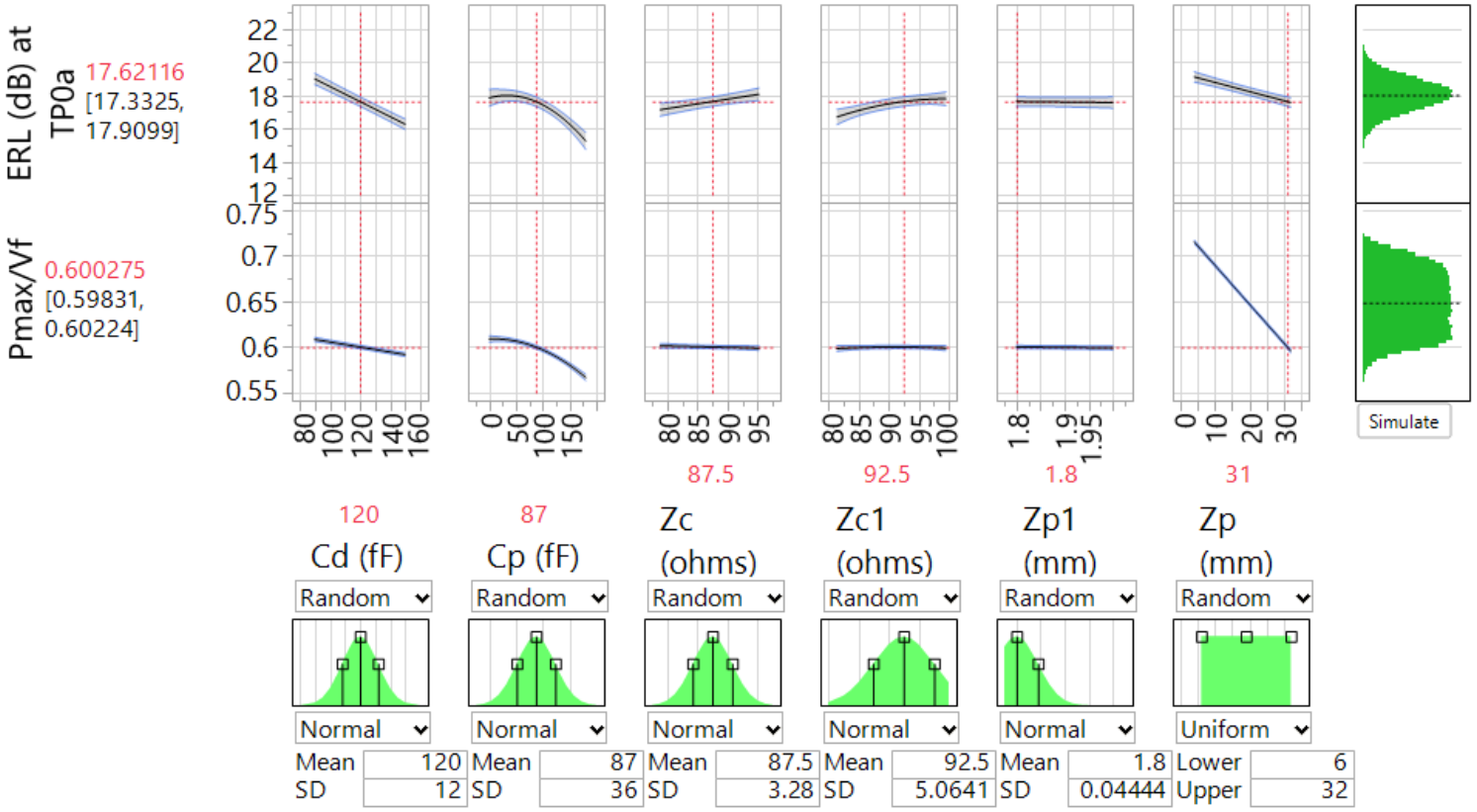


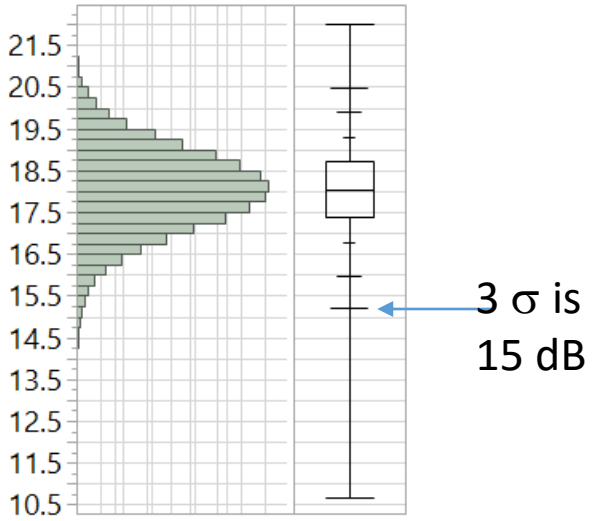
Figure 93–5—Transmitter test fixture and test points

Zp	Zp Pmax/ Vf TP0a	Zp Pmax /Vf Tp0	ERL (dB) Tp0a N_{bx}=42	ERL (dB) Tp0
12 mm	0.68	0.727	18.28	14.28
31 mm	0.540	0.577	17.67	14.72

Zp	Zp Pmax/ Vf TP0a	Zp Pmax /Vf Tp0	ERL (dB) Tp0a N_{bx}=48	ERL (dB) Tp0
12 mm	0.68	0.727	18.55	14.5
31 mm	0.540	0.577	18.07	15.05

Distribution suggest Tx/Rx ERL limits at tp0a





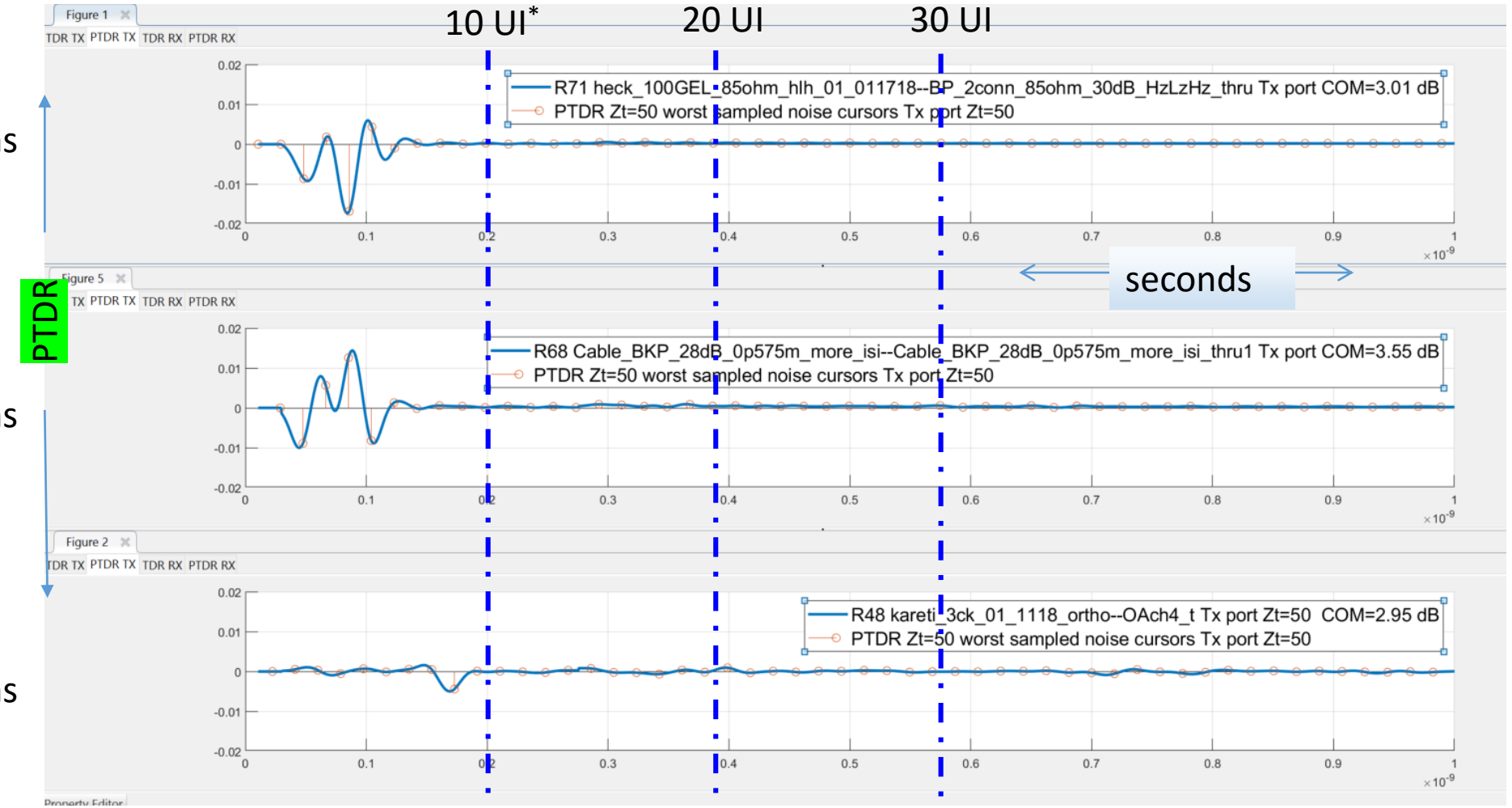
Selecting channel with reflection near TP0 for experimenting

PTDR of Clause 163 Channels with Reflections near TP0 and with COM ~ 3 dB

Larger reflections

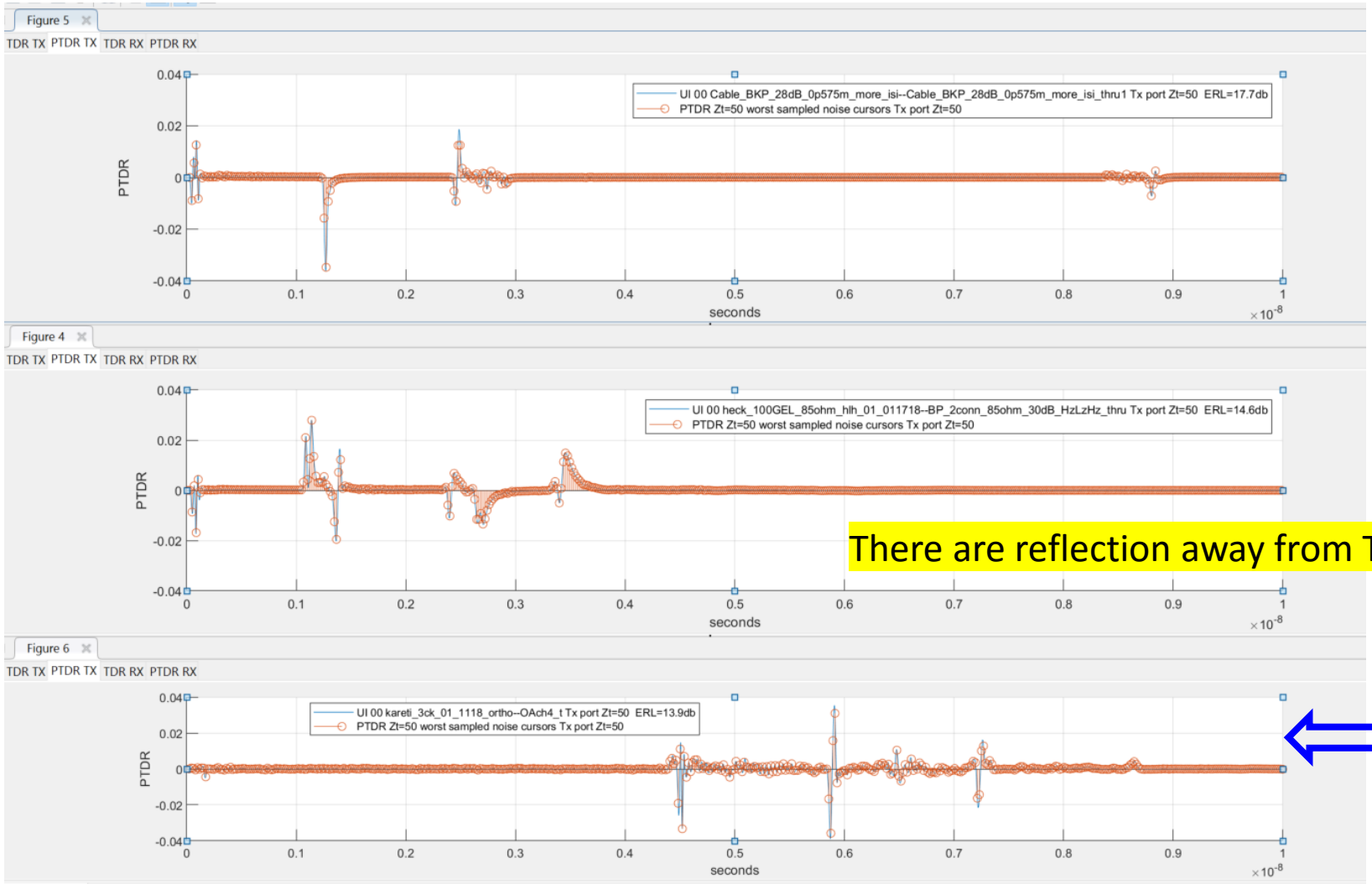
Larger reflections

Smaller reflections



*Delay through 30 mm package is ~ 10 UI

PTDR the rest of the story: All the channel have reflections



There are reflection away from TP0

Most all return loss is all comprehended in COM

Kappa (κ) may be used to determine impact of reflections (from healey_3ck_01a_0120)

- The transfer function from the transmitter input to the receiver output is the following

$$H_{21} = \frac{s_{21}^{(t)} s_{21} s_{21}^{(r)}}{1 - s_{22}s_{11}^{(r)} - s_{11}s_{22}^{(t)} + s_{11}^{(r)}s_{22}^{(t)}\Delta S}$$

$$\Delta S = s_{11}s_{22} - s_{21}s_{12}$$

$$s_{21} = s_{12}$$

- Note that $1/(1+x) \cong 1 + x + x^2 + \cdots$ for $|x| < 1$

κ2 κ1 κ1*κ2

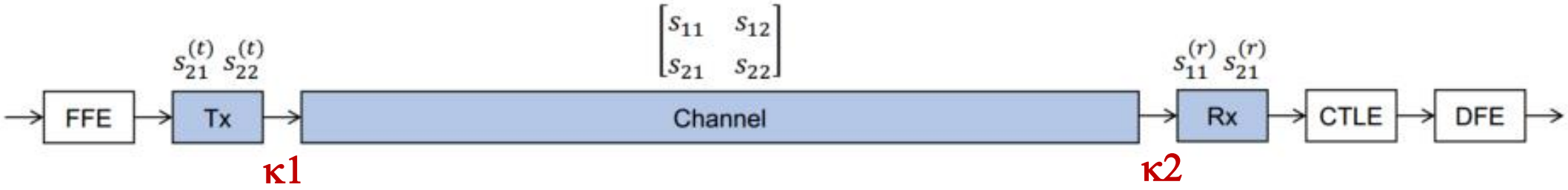
$$H_{21} \cong s_{21}^{(t)} s_{21} s_{21}^{(r)} \left(1 + s_{22}s_{11}^{(r)} + s_{11}s_{22}^{(t)} + s_{21}s_{21}s\right.$$

Rx-Tx re-reflection
Tx re-reflection
Rx re-reflection

- Constraints on s_{11}, s_{22}, $s_{11}^{(r)}$, and $s_{22}^{(t)}$, e.g., ERL, are imposed to limit the re-reflection

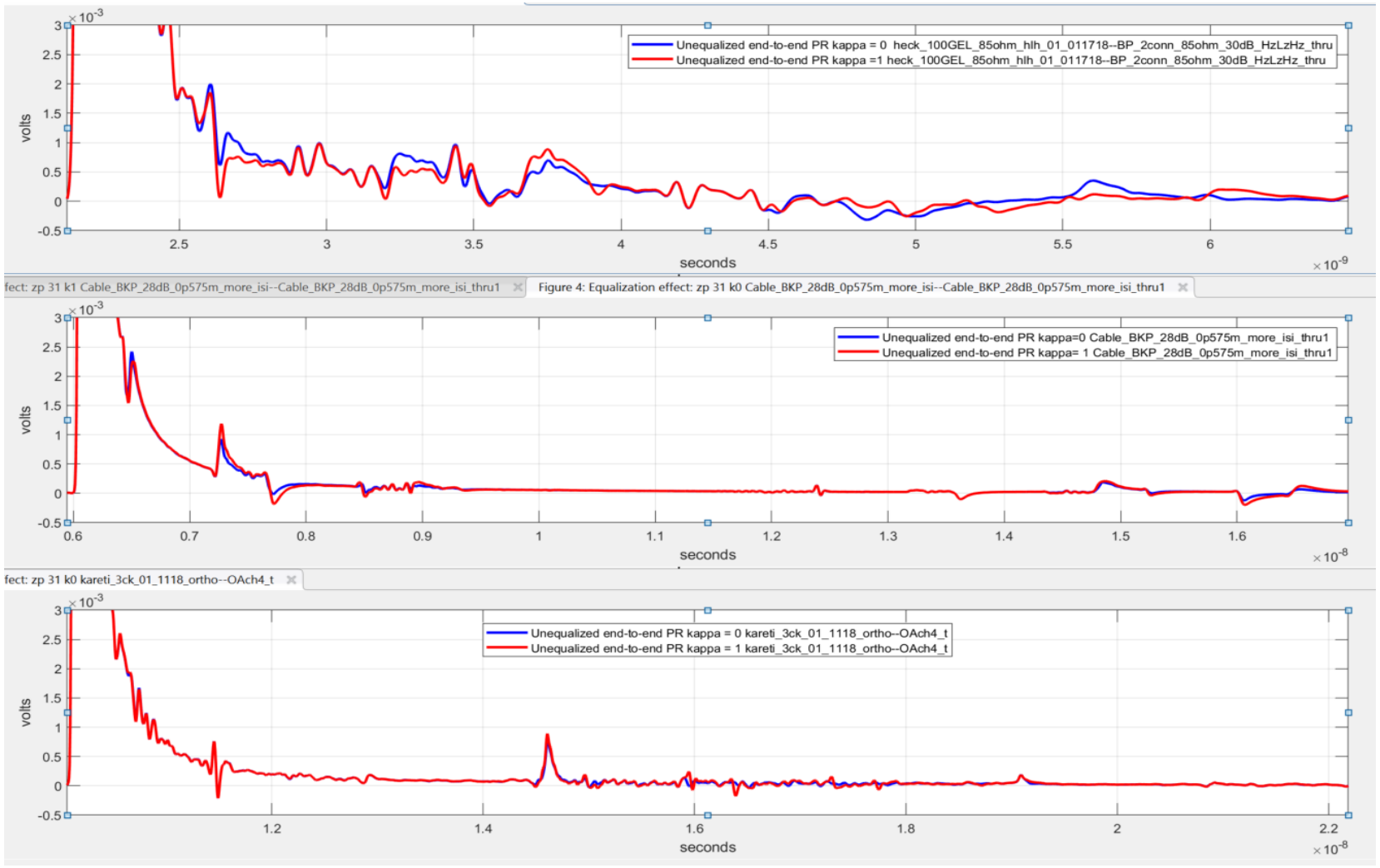
If κ1 and κ2 are zero, the reflection at port 1 and 2 are not permitted to occur
κ1 and κ2 can also apportion reflection

Delta COM is the difference between COM with:
κ1 and κ2 set to one minus
COM with κ1 and κ2 set to some other value

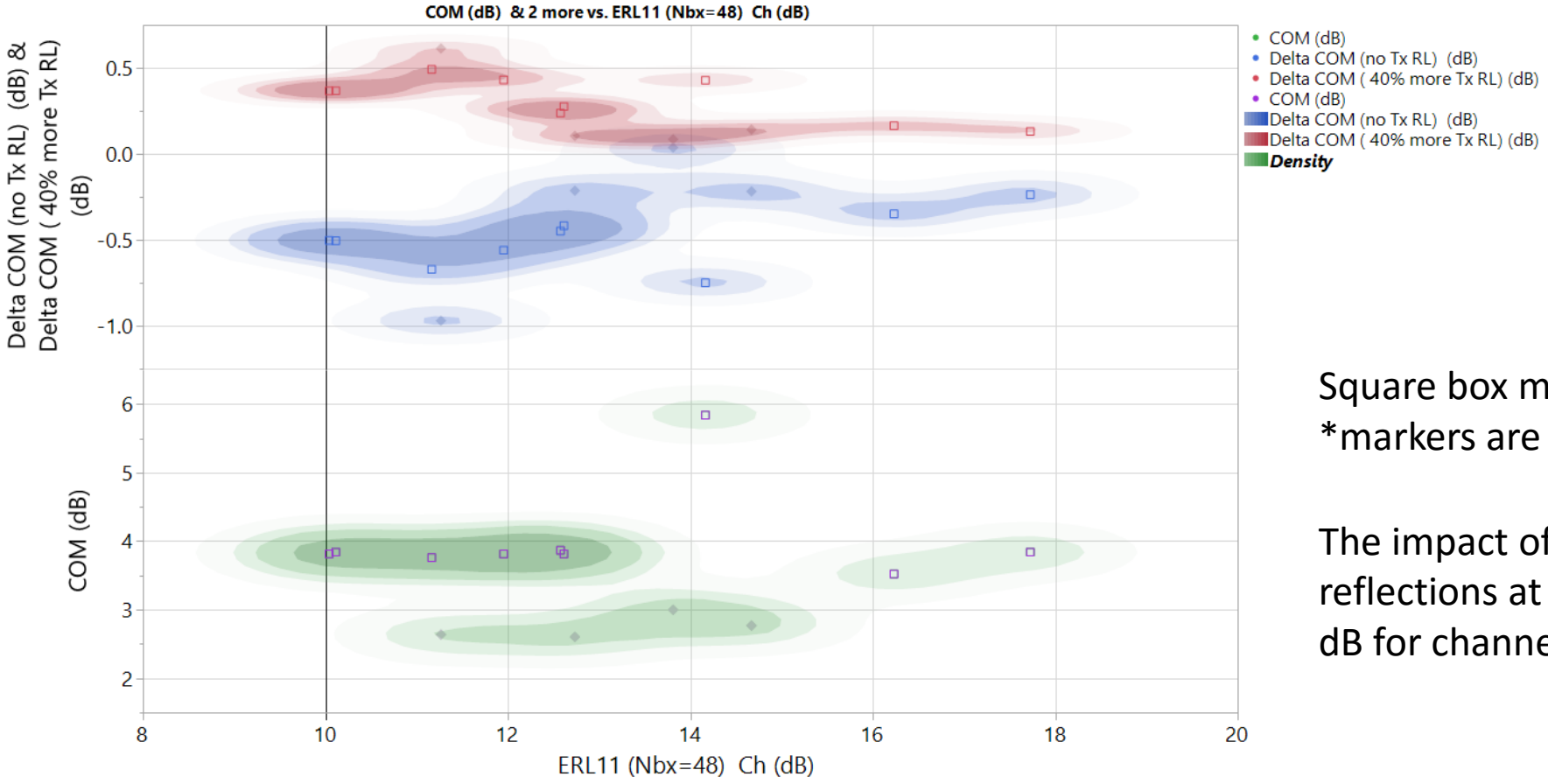


Delta COM

κ = 0 (no tp0 reflection) and κ=1 seen at the receiver at tp5



Start with: ERL_{min} = 10 dB



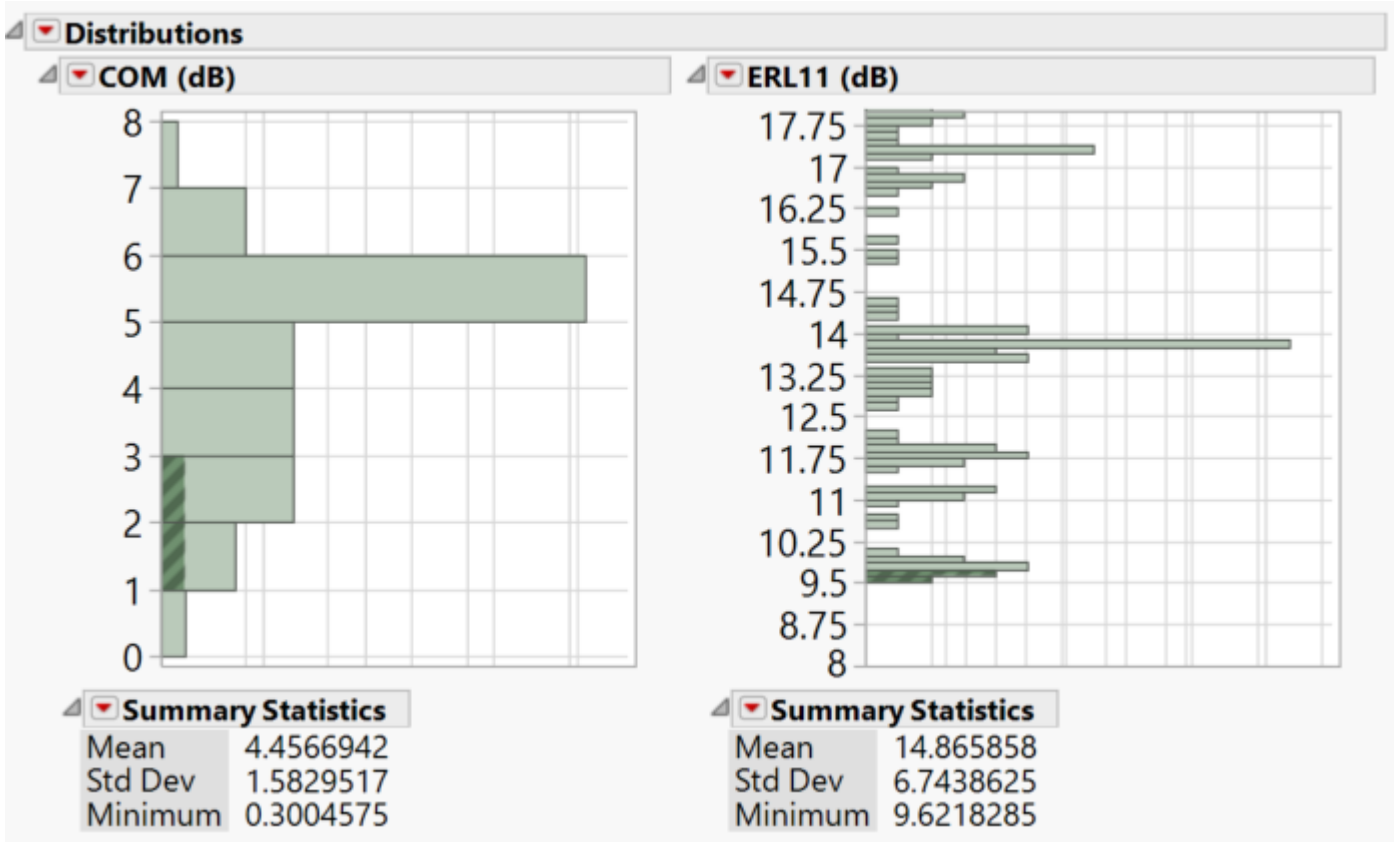
Square box markers are COM > 3.5 dB
*markers are COM <= 3dB

The impact of with and without reflections at tp0 is only about ½ dB for channels which pass COM

All channel with lower than 9.75 dB ERL Fail COM

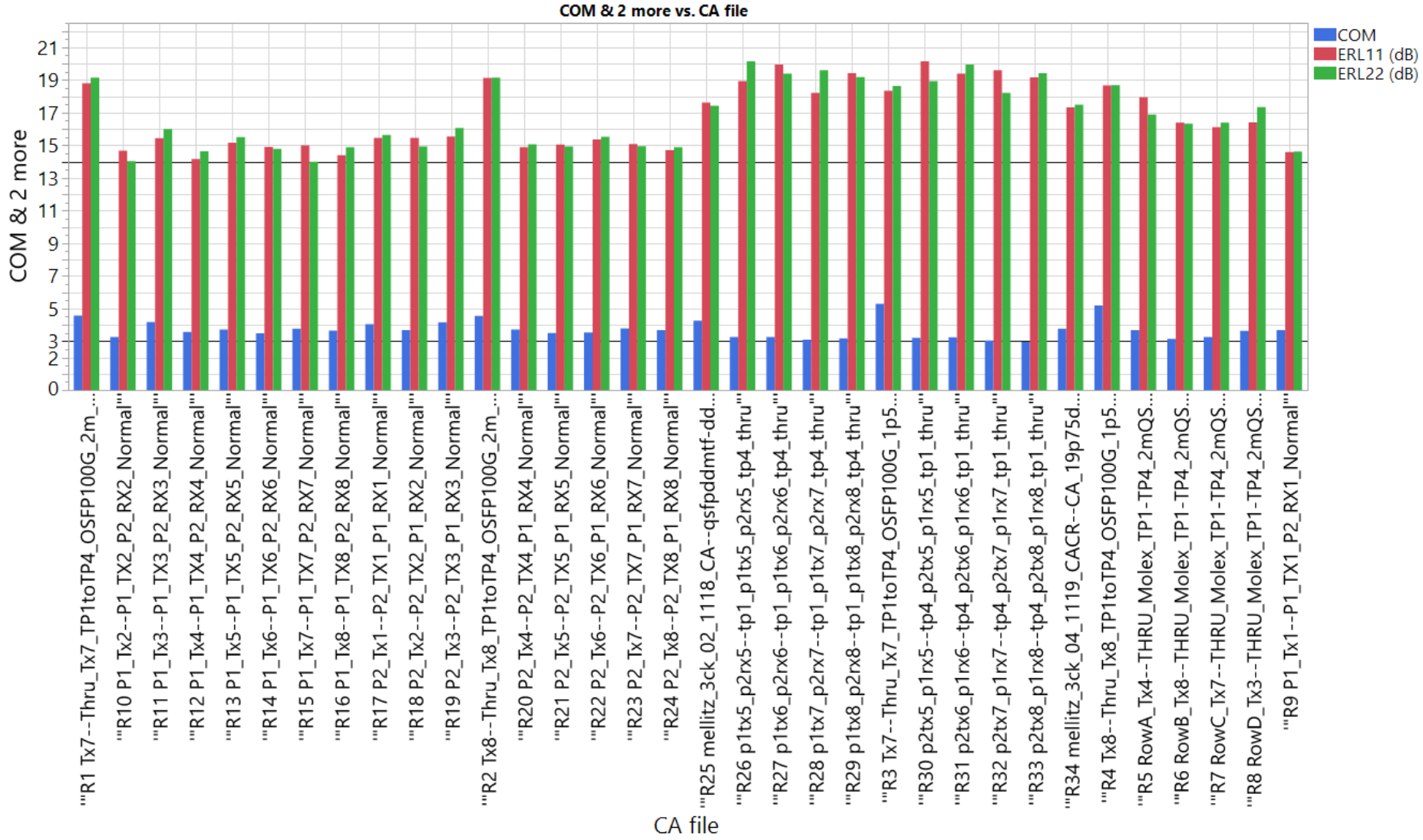
Computed for N_{bx}=42

ERL/N_{bx} ratio ~= 0.06 dB/N_{bx}



Cable Assembly Data

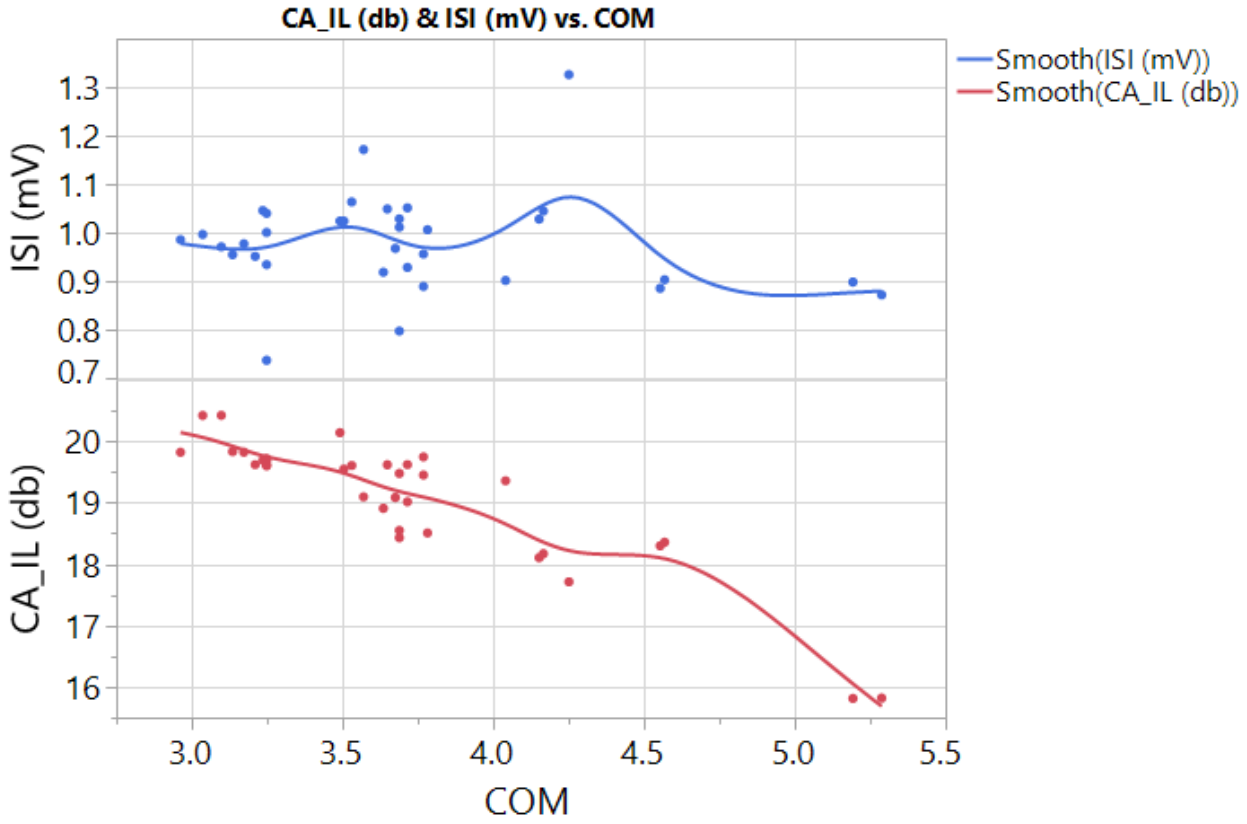
CA data COM and ERL (Nbx=42)



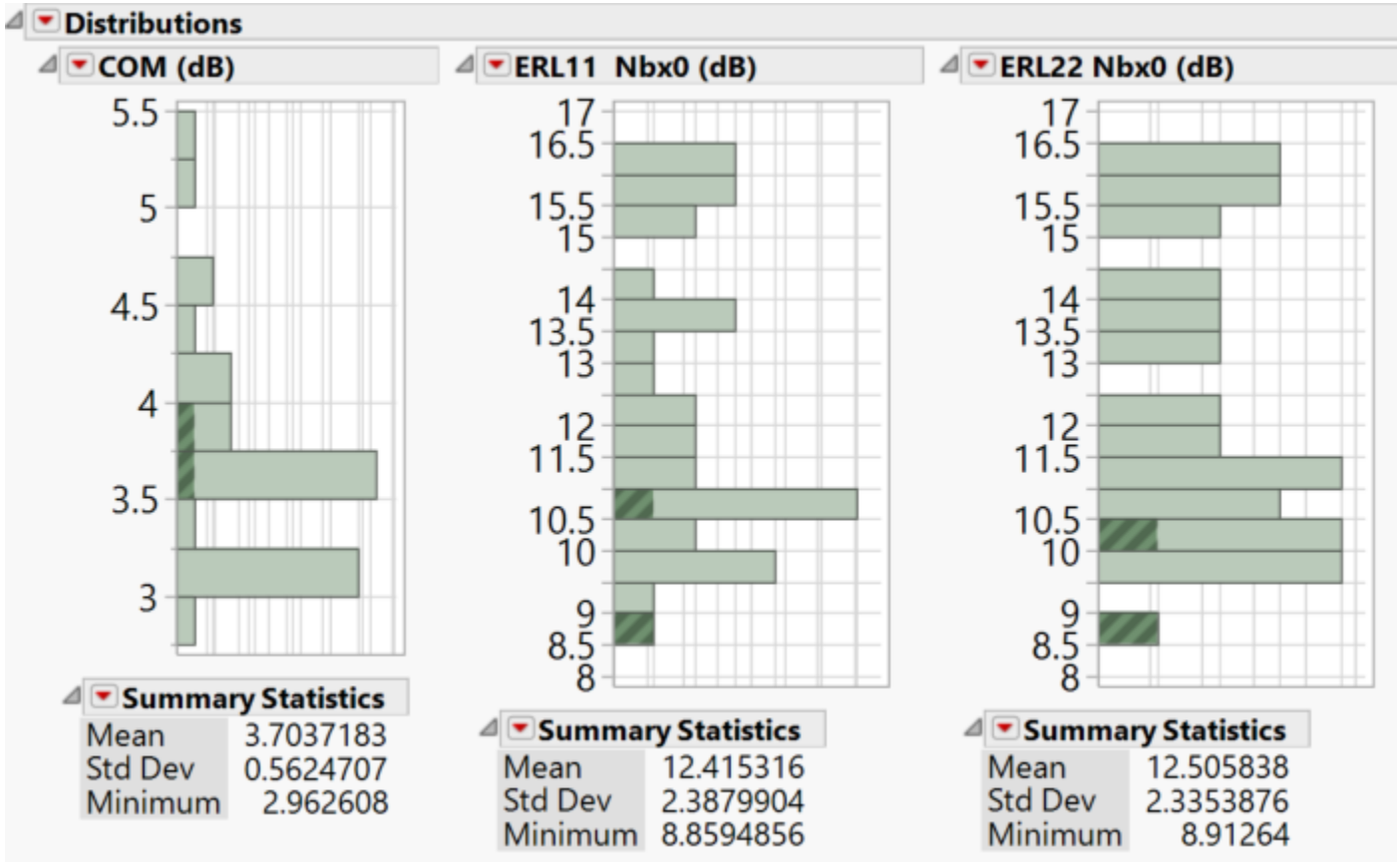
COM vs IL and ISI … correlations

COM correlated to Cable IL

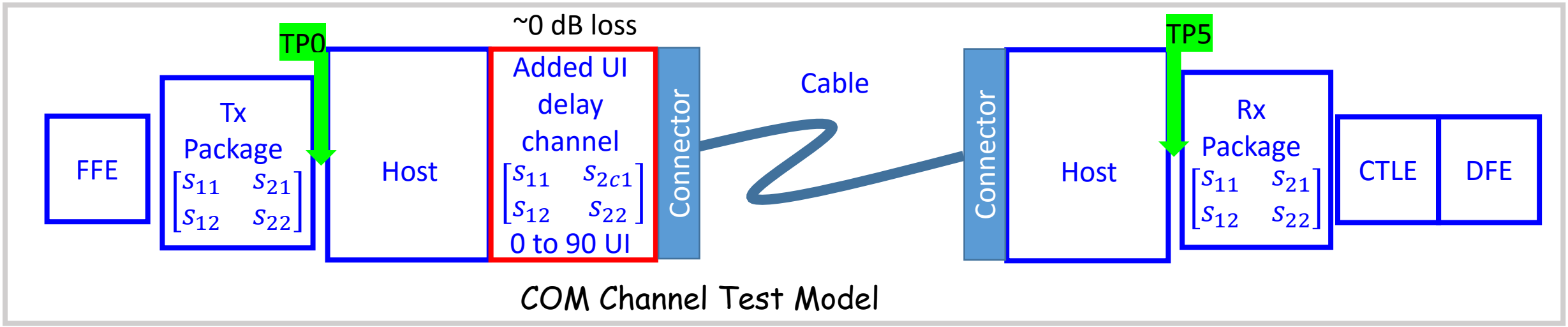
COM not correlated to ISI



Based on All posted CA channel ERL min looks like 8.5 dB with N_{bx}=0



DAC Cable Delay experiment

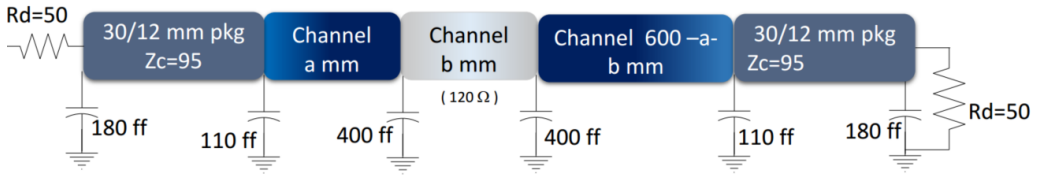


- ❑ Similar experiment what was done for packages and KR channels
- ❑ A similar experiment was done durn .3ck ERL developent

Look back at the ERL experiment in mellitz_3cd_01b_1117

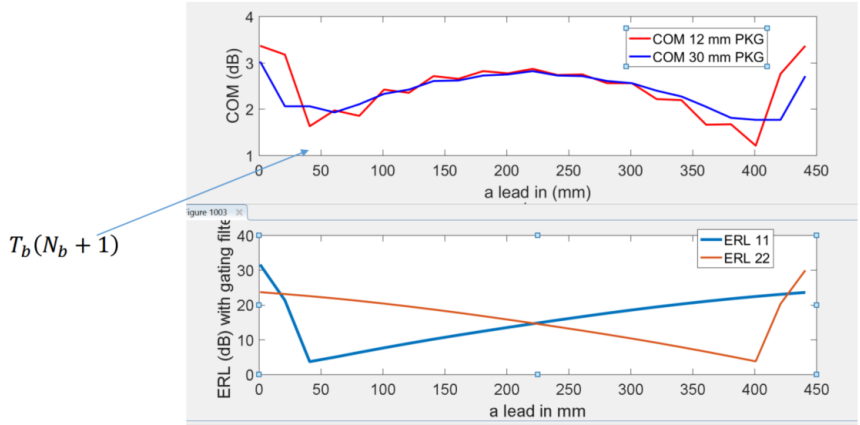
Would changing the amount of reflection alter the trends of the results?

- ❑ Change the capacitor to 400 ff from 200 ff
- ❑ Shorten the total length to 450 mm from 600 mm to keep around 3 dB of COM



mm	ff	Ω	mm	ff	mm	ff	mm	ff	mm	ff	mm	Ω	ff	Ω
30	180	95	12	110	a	400	b	400	450 -a-b	110	30	95	180	50

Similar trends regardless of reflection magnitude

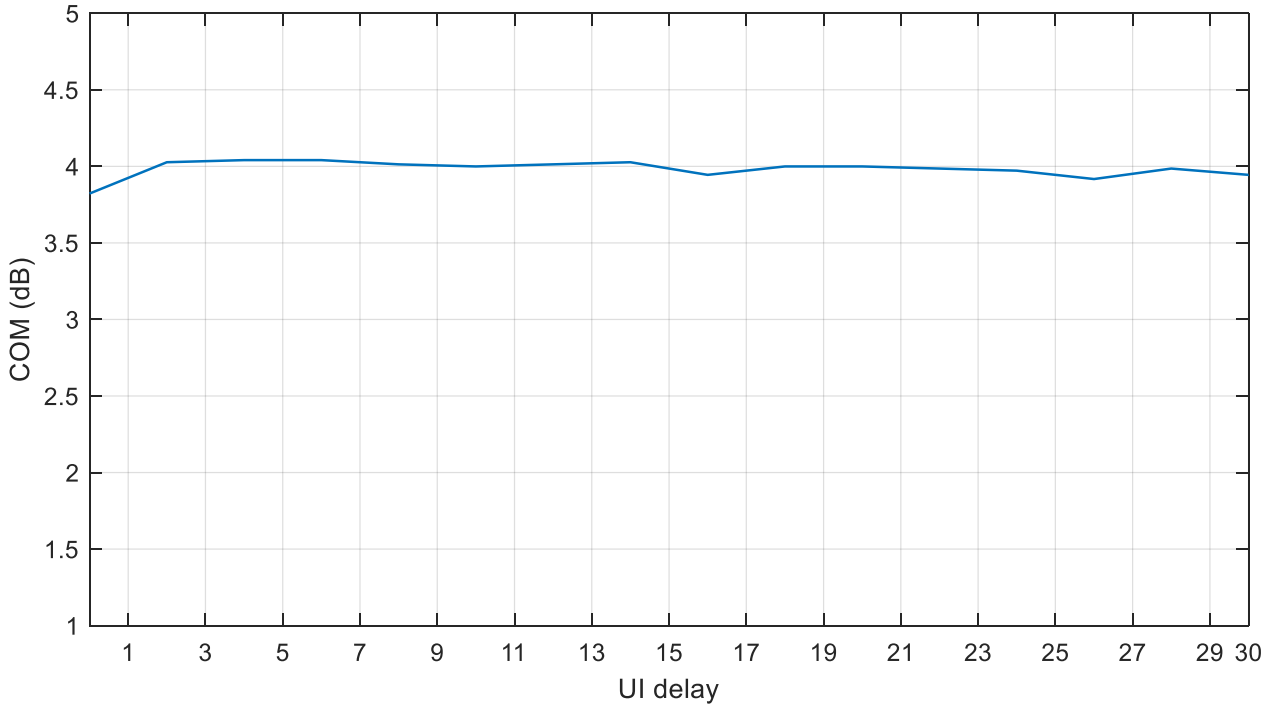


Takeaway:

- Similar effects on either end of the channel
- A key factor is the distance a channel reflection is from either Tx or Rx package

Hypothesis: Based on the above there should be little affect from the added delay aside from the expected resonances

As expect there is little impact from the delay and no obvious impact from the DFE reach



Supports the assertion that N_{bx} should be 0 for CR
Since the ERL is measured a far distance from the devices

ERL minimum values to be reviewed by vested parties

Clause/Annex	type	ERL min (dB) at TP0a	ERL min (dB)at TP0
162.9.3.4	Tx Host	TBD	TBD
162.9.4.5	Rx Host	TBD	TBD
162.11.3	CA	NA	8.5
163.9.1.1	Tx Chip	15	13
163.9.2.1	Rx Chip	15	13
163.10.2	Channel	NA	9.75
120F.3.1.1	Tx Chip	13.5	11.5
120F.3.2.1	Rx Chip	13.5	11.5
120F.4.3	Channel	TBD	TBD
120G.3.1.3	Host/Module	TBD	TBD