# P802.3ck D1.0
# Comment Resolution Agenda

P802.3ck Editorial Team

IEEE P802.3ck Task Force
January 2020

# KR: 163 (Phil)

| Topic | Comment # | Count |
|---|---|---|
| COM | [68], [139] | 2 |
| TP0a/TP5a Measurement | [30 31 benartsi_3ck_01_0320], [32] | 3 |
| RX Jitter tolerance | [33] | 1 |
| TX characteristics | [58 ran_3ck_01_0320] | 1 |
| Channel Characteristic | [39] | 1 |
| | Open comments | 8 |

Legend: [##,##,##] = related comments, ## = pivot comment, ##* = cross-clause comment, [##,##,author_nn] = related presentation

# Comment # 68

Comment:

*Cl* **163** *SC* **163.9.1** *P* **175** *L* **44** # 68

Mellitz, Richard Samtec

*Comment Type* **TR** *Comment Status* **D**

Vfmin should align with Av in COM table 163-10 since Np=200

*SuggestedRemedy*

Replace 0.4 with 0.413

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

For task force discussion.

D1.1 Spec. Note it is table 163-5.

**Table 163–5—Summary of transmitter specifications at TP0a**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate | | 53.125 ± 100 ppm | GBd |
| Differential pk-pk voltage (max.)[a]<br>Transmitter disabled<br>Transmitter enabled | 93.8.1.3 | <br>30<br>1200 | <br>mV<br>mV |
| DC common-mode voltage (max.)[1] | 93.8.1.3 | 1.9 | V |
| DC common-mode voltage (min.)[1] | 93.8.1.3 | 0 | V |
| AC common-mode RMS voltage (max.)[1] | 93.8.1.3 | 30 | mV |
| Effective return loss (ERL) (min.) | 163.9.1.1 | TBD | dB |
| Common-mode return loss (min.) | 93.8.1.4 | TBD | dB |
| Transmitter steady-state voltage, $v_f$ (min.)<br>Transmitter steady-state voltage, $v_f$ (max.) | 162.9.3.1.2 | 0.4<br>0.6 | V |

# Comment # 139

Comment:

| | | | | |
|---|---|---|---|---|
| *Cl* **163** | *SC* **163.10** | *P* **183** | *L* **13** | # 139 |

Dawe, Piers — Mellanox

*Comment Type* **TR** *Comment Status* **D**

Slide 6 of heck_3ck_01_0919 shows that the DFE taps are 2 and 3 are always strongly positive, and no taps strongly negative, yet the draft would allow such untypical/hypothetical channels that a real receiver need not, and maybe can't, cope with.
kasapi_3ck_01_1119 slide 7 shows the first tap also.
We need sensible minimum tap limits.

*SuggestedRemedy*

Add minimum tap weight limits:
Tap 1: min +0.3
Tap 2: min +0.05
Remembering that a tap weight limit isn't a hard pass-fail limit; channels can go outside it but pay a (very small, for one or two small excursions) increase in COM for the excess ISI noise that they cause:
All other taps: min -0.04 (looser than for CR).
Turn the existing "Normalized DFE coefficient magnitude limit"s into "Normalized DFE coefficient limit"s.
Update definition of COM in 93A.1.

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.

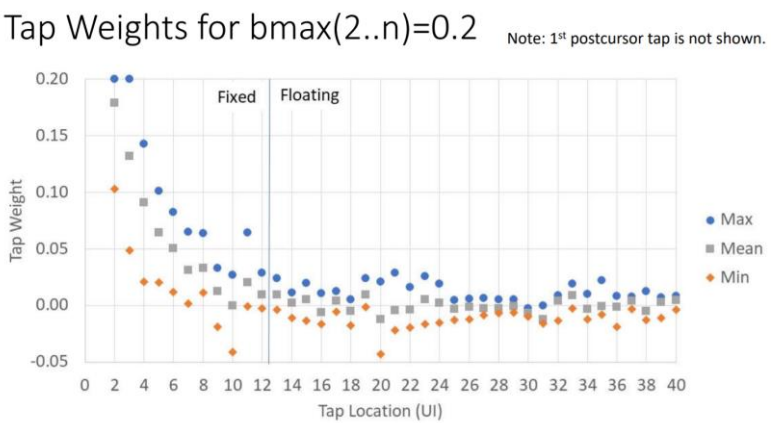
The comment does provide sufficient evidence that the suggested remedy will not hinder reasonable, practical channels.

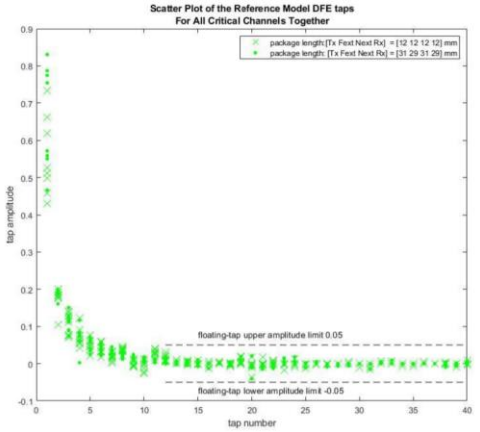
For task force discussion.

Summary of the suggested remedy:
b(1) : change [-0.85, 0.85] to [0.3, 0.85]
b(2): change [-0.3 0.3] to [0.05, 0.3]

b(3,…,Nb): change [-0.2 0.2] -> [-0.04, 0.2]

Related material:
http://www.ieee802.org/3/ck/public/19_11/kasapi_3ck_01_1119.pdf
http://www.ieee802.org/3/ck/public/19_09/heck_3ck_01_0919.pdf




D1.1 Spec:

| | | | |
|---|---|---|---|
| Decision feedback equalizer (DFE) length | $N_b$ | 12 | UI |
| Normalized DFE coefficient magnitude limit<br>$n = 1$<br>$n = 2$<br>$n = 3$ to $N_b$ | $b_{max}(n)$ | <br>0.85<br>0.3<br>0.2 | — |

| | | | |
|---|---|---|---|
| Normalized coefficient magnitude limit for DFE floating taps | $b_{gmax}$ | 0.05 | — |
| DFE floating tap tail root-sum-of-squares limit | $\sigma_{max}$ | 0.02 | — |
| DFE floating tap tail starting position | $N_{ts}$ | 25 | — |

# Comment # 30

Comment:

*Cl* **163** *SC* **163.9.1** *P* **175** *L* **26** # 30

Ben Artsi, Liav — Marvell

*Comment Type* **T** *Comment Status* **D** *TPO extrapolation*

TP0a has been shown to be extremely difficult to be used as a point to measure Specified Tx compliance parameters.

*SuggestedRemedy*

Measurement will still be done at TP0a, but Tx is to be specified at TP0.
A new annex is to be defined to specify method of extrapolating/simulating each of the Tx parameters from TP0 to TP0a.
A presentation will be provided.

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.

[The proposed change in the comment does not contain sufficient detail to understand the specific changes that satisfy the commenter.]

The suggested remedy does not provide sufficient detail to implement.

A presentation relating to this comment is anticipated for the March meeting.

Comment #35 addresses the same issue for Clause 120F.

For task force discussion.

See comment #35.

D1.1 Spec:

Table 163–5—Summary of transmitter specifications at TP0a

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate | | 53.125 ± 100 ppm | GBd |
| Differential pk-pk voltage (max.)[a]<br>Transmitter disabled<br>Transmitter enabled | 93.8.1.3 | <br>30<br>1200 | <br>mV<br>mV |
| DC common-mode voltage (max.)[1] | 93.8.1.3 | 1.9 | V |
| DC common-mode voltage (min.)[1] | 93.8.1.3 | 0 | V |
| AC common-mode RMS voltage (max.)[1] | 93.8.1.3 | 30 | mV |
| Effective return loss (ERL) (min.) | 163.9.1.1 | TBD | dB |
| Common-mode return loss (min.) | 93.8.1.4 | TBD | dB |
| Transmitter steady-state voltage, $v_f$ (min.)<br>Transmitter steady-state voltage, $v_f$ (max.) | 162.9.3.1.2 | 0.4<br>0.6 | V |
| Linear fit pulse peak (min.) | 162.9.3.1.2 | TBD × $v_f$ | V |
| Level separation mismatch ratio $R_{LM}$ (min.) | 120D.3.1.2 | 0.95 | — |

Related material:
http://www.ieee802.org/3/ck/public/20_03/benartsi_3ck_01_0320.pdf

- Call for action: Form a brain storming group to tailor the required mathematics

# Comment # 31

Comment:

*Cl* **163** *SC* **163.9.1.2** *P* **176** *L* **47** # 31

Ben Artsi, Liav Marvell

*Comment Type* **T** *Comment Status* **D** *TP0A TF*

A reference TP0 - TP0a test fixture is specified. It is also indicated that the difference between the test fixture and the actual implementation is to be taken into account in the measurement. It is not stated how to do this adjustment.

*SuggestedRemedy*

Specify an achievable range for the TP0 - TP0a test fixture: Loss @ ~26GHz <6dB ; ILD ; ERL? A presentation is to be provided with the actual suggestion

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.

The suggested remedy does not provide sufficient detail to implement. However, a presentation relating to this comment is anticipated at the March meeting.

D1.1 Spec:

**163.9.1.2 Transmitter test fixture**

Unless otherwise noted, measurements of the transmitter are made at the output of a test fixture (TP0a) as shown in Figure 163–3.

Related material:
http://www.ieee802.org/3/ck/public/20_03/benartsi_3ck_01_0320.pdf
The presentation calls for action to brainstorm solutions.

# Comment # 32

Comment:

Cl 163 SC 163.9.2.2 P 179 L 21 # 32

Ben Artsi, Liav Marvell

*Comment Type* **T** *Comment Status* **D** *(IR)*

The Rx test fixture is embedded as part of the interconnect used for the interference tolerance test. Thus, there is no reason to limit the loss and behavior so tightly as done on line 21. Doing so will not enable connecting more than very few (if any!) Rx lanes to TP5a for testing.

*SuggestedRemedy*

Recommend increasing loss limits to 4dB at 26.56GHz

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.

[The proposed change in the comment does not contain sufficient detail to understand the specific changes that satisfy the commenter.]

The suggested remedy does not provide a complete solution. For instance, a new insertion loss equation for Equation 163-1 is required.

For task force discussion.

D1.1 Spec:

4 dB ?

The insertion loss of the test fixture shall be between 1.2 dB and ~~1.6 dB~~ at 26.56 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.01 dB from 0.05 GHz to 26.56 GHz.

The updated proposed response:

Proposed Reject.

No evidence is provided that the impact on TP1a measurement will not be adversely affected.

# Comment # 33

Comment:

Cl 163 SC 163.9.2.4 P 180 L 47 # 33

Ben Artsi, Liav Marvell

*Comment Type* T *Comment Status* D *jitter tolerance*

Reciever jitter tolerance test is specified at specific frequency points with no specified extrapolation between frequency points. More specificaly, 5UI at 40KHz, 0.15UI at 1.33MHz 0.05UI at 4-40MHz. Tx is measured when applying high pass filter on the jitter filtering out much of the low frequency jitter of a transmitter. A transmitter may still comply with the TX specifications and have much more than 0.15UI of jitter at frequecies which reside around a few handers of Hz. Since there is no Rx jitter tolerance requirement at these frequencies: A transmitter may have relatively high jitter at low frequencies and still be compliant. The Rx may not be able to tolerate this jitter while being compliant as well. The interoperability between these specified Tx and Rx is questionable.

*SuggestedRemedy*

Add a sentence that the reciever is expected to meet any frequency point between the specified in table 163-9 while jitter tolerance requirement is linearly extrapolated between any consecutive specified frequency points.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

Add the following new text and equation:
"Although the jitter tolerance test is specified at discrete frequencies, a compliant receiver tolerates jitter at any frequency between 40 kHz and 40 MHz with peak-to-peak amplitude according to equation 163-new.

Equation 163-new:
jitter(f) = (0.05*4 MHz / f) for 40 kHz < f < 4 MHz
jitter(f) = 0.05 for 4 MHz < f < 40 MHz

The receiver under test shall meet the FEC symbol error ratio requirements for each case in Table 163–9.

**Table 163–9—Receiver jitter tolerance parameters**

| Parameter | Case A | Case B | Case C | Case D | Case E | Units |
|---|---|---|---|---|---|---|
| FEC Symbol error ratio | $10^{-3}$ | $10^{-3}$ | $10^{-3}$ | $10^{-3}$ | $10^{-3}$ | — |
| Jitter frequency | 0.04 | 1.333 | 4 | 12 | 40 | MHz |
| Jitter amplitude (pk-pk) | 5 | 0.15 | 0.05 | 0.05 | 0.05 | UI |

D1.1 Spec:

### 163.9.2.4 Receiver jitter tolerance

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 163–9. The test setup shown in Figure 93–12, or its equivalent, is used. The test channel meets the insertion loss requirement for Test 2 in Table 163–8. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0a. The test procedure is the same as the one described in 120D.3.2.1, with the following exceptions:

# Comment # 58

Comment:

Cl 163 SC 163.9.1 P 175 L 35 # 58

Ran, Adee Intel

*Comment Type* T *Comment Status* D

As was discussed in the January 2020 meeting there is interest in enabling DC-coupled channels in some applications (mainly backplane and C2C) when the two link partners support this operation. Avoiding AC coupling capacitors in the channels can help board design, improve signal integrity, and reduce costs, and it is becoming a common requirement.

Current channel specs refer back to 93.9.4 where it is stated that AC coupling capacitors may not exist between TP0 and TP5, but in that case some specifications may need modifications for interoperability (without stating the modifications explicitly). This leaves the burden of defining new Rx and Tx specifications to implementers and integrators - with no standard to assist them.

Indeed, the current transmitter specifications in 120F.3.1 and in 163.9.1 allow high common mode voltage up to 1.9 V, which is detrimental for DC coupling with modern CMOS devices. This high value is also not useful for Tx design with modern applications.

DC coupling can be supported by limiting the Tx common mode voltage to a more reasonable and useful range. If this is done, the existing specs may be useable without change for DC coupled channels (although receivers may still need special support for this).

This proposal is specific for KR and C2C specifications which require on-board AC coupling; CR and C2M have AC coupling in the cable and in the module, respectively, so they need a separate discussion.

*SuggestedRemedy*

In the transmitter characteristics tables of Clause 163 and Annex 120F, Change the Tx common mode voltage to be between 0.2 and 0.8 volts.

Additional content may be beneficial for the AC coupling subclauses. I intend to provide some text in a presentation, to complement the suggested Tx specs.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

A presentation related to this comment is anticipated at the March meeting.

In Table 163-5 and Table 120F-1, change DC common-mode voltage (max.) to ~~0.8 V~~, and DC common-mode voltage (min.) to 0.2 V.

For task force discussion.

D1.1 Spec:

**Table 163–5—Summary of transmitter specifications at TP0a**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate | | 53.125 ± 100 ppm | GBd |
| Differential pk-pk voltage (max.)[a]<br>Transmitter disabled<br>Transmitter enabled | 93.8.1.3 | <br>30<br>1200 | <br>mV<br>mV |
| DC common-mode voltage (max.)[1] | 93.8.1.3 | 1.9 | V |
| DC common-mode voltage (min.)[1] | 93.8.1.3 | 0 | V |
| AC common-mode RMS voltage (max.)[1] | 93.8.1.3 | 30 | mV |

Related material:
http://www.ieee802.org/3/ck/public/20_03/ran_3ck_01_0320.pdf

| | | | |
|---|---|---|---|
| DC common-mode voltage (max.)[1] | 93.8.1.3 | ~~1.9~~ 0.9 | V |
| DC common-mode voltage (min.)[1] | 93.8.1.3 | ~~0~~ 0.2 | V |

Note: Modified from 0.8 in suggested remedy

Note:
Change 0.8 V in proposed response to 0.9 V

# Comment # 39

Comment:

*Cl* **163** *SC* **163.10** *P* **181** *L* **26** # 39

Ben Artsi, Liav Marvell

*Comment Type* **T** *Comment Status* **D**

Differential to common mode conversion loss is not defined for a TP0 to TP5 interconnect channel characteristics

*SuggestedRemedy*

Specify that the differential to common mode conversion loss of TP0 to TP5 shall be [TBD] and correlated to the capability defined in 162.11.5 when measured with an MCB

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

For task force discussion.

Reference in D1.1 CL162:

**162.11.5 Differential to common-mode conversion loss**

The cable assembly differential to common-mode conversion loss shall meet the requirements of TBD.

**162.11.6 Common-mode to common-mode return loss**

The cable assembly common-mode to common-mode return loss shall meet the requirements of TBD.