D1.2 Comments

Comment#180,#181,#182

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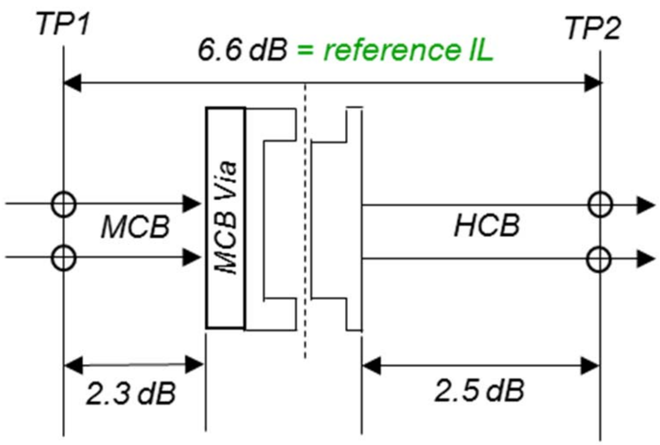
Comment#180

- Proposals for 162B.1 Mated Test Fixtures specification
- Provide specifications for TBDs;
  - 162B.1.3.1 Mated test fixtures differential insertion loss FOM_{ILD}
  - 162B.1.3.2 Mated test fixtures differential return loss
  - 162B.1.3.3 Mated test fixtures common-mode conversion insertion loss
  - 162B.1.3.6 Mated test fixtures integrated crosstalk noise

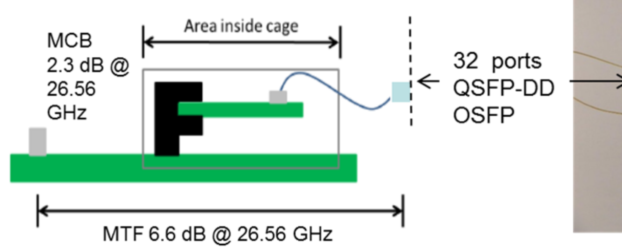
Mated Test Fixture Specifications

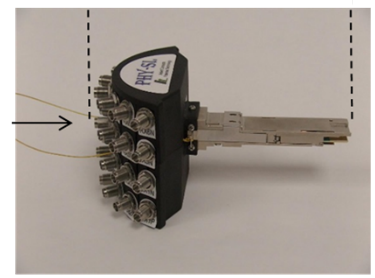
- **Measurements with compliant PCB IL - HCB and MCB**

Mated Test Fixture Adopted in Baseline



Note: 2.3 dB MCB PCB includes test point IL and MCB Via allowance is 0.2 dB





Mated test fixtures

162B.1.3.2 Mated test fixtures differential return loss

The differential return loss of the mated test fixtures measured at each test fixture interface shall meet the values determined using Equation (162B–6).

$$DRL(f) \geq \{TBD\} \quad (162B–6)$$

for $0.01\ \text{GHz} \leq f \leq 50\ \text{GHz}$

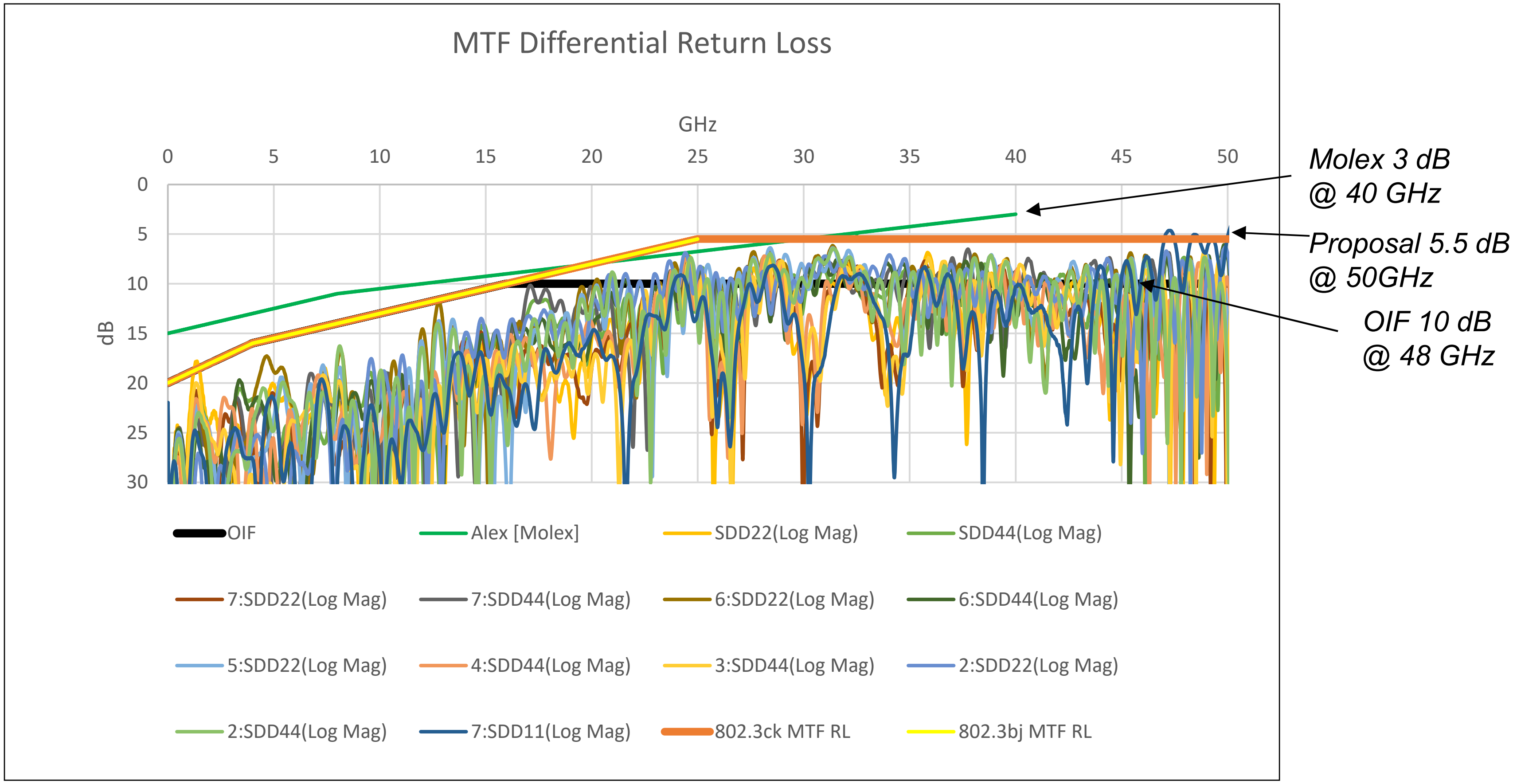
where

$DRL(f)$	is the differential return loss in dB at frequency f
f	is the frequency in GHz

The mated test fixtures differential return loss is illustrated in Figure 162B–4.

- *DRL(f)≥ TBD*

MTF Differential Return Loss



Differential Return Loss =

20-f_{GHz} 0.01/0.05 (TBD) GHz ≤ f_{GHz} < 4 GHz

18-0.5*f_{GHz} 4 GHz ≤ f_{GHz} < 25 GHz

5.5 25 GHz ≤ f_{GHz} < 40/50 (TBD) GHz

OIF

- MTF MIN (DRL) = -20+f (dB) 50MHz < f < 4GHz
- MTF MIN (DRL) = -18+f/2 (dB) 4GHz < f < 16GHz
- MTF MIN (DRL) = -10 (dB) 16GHz < f < 48GHz

Mated test fixtures

162B.1.3.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures measured at either test fixture test interface shall meet the values determined using Equation (162B–7). This parameter is common-mode to differential-mode conversion insertion loss.

$$CMCIL(f) \geq \{TBD\} \tag{162B–7}$$

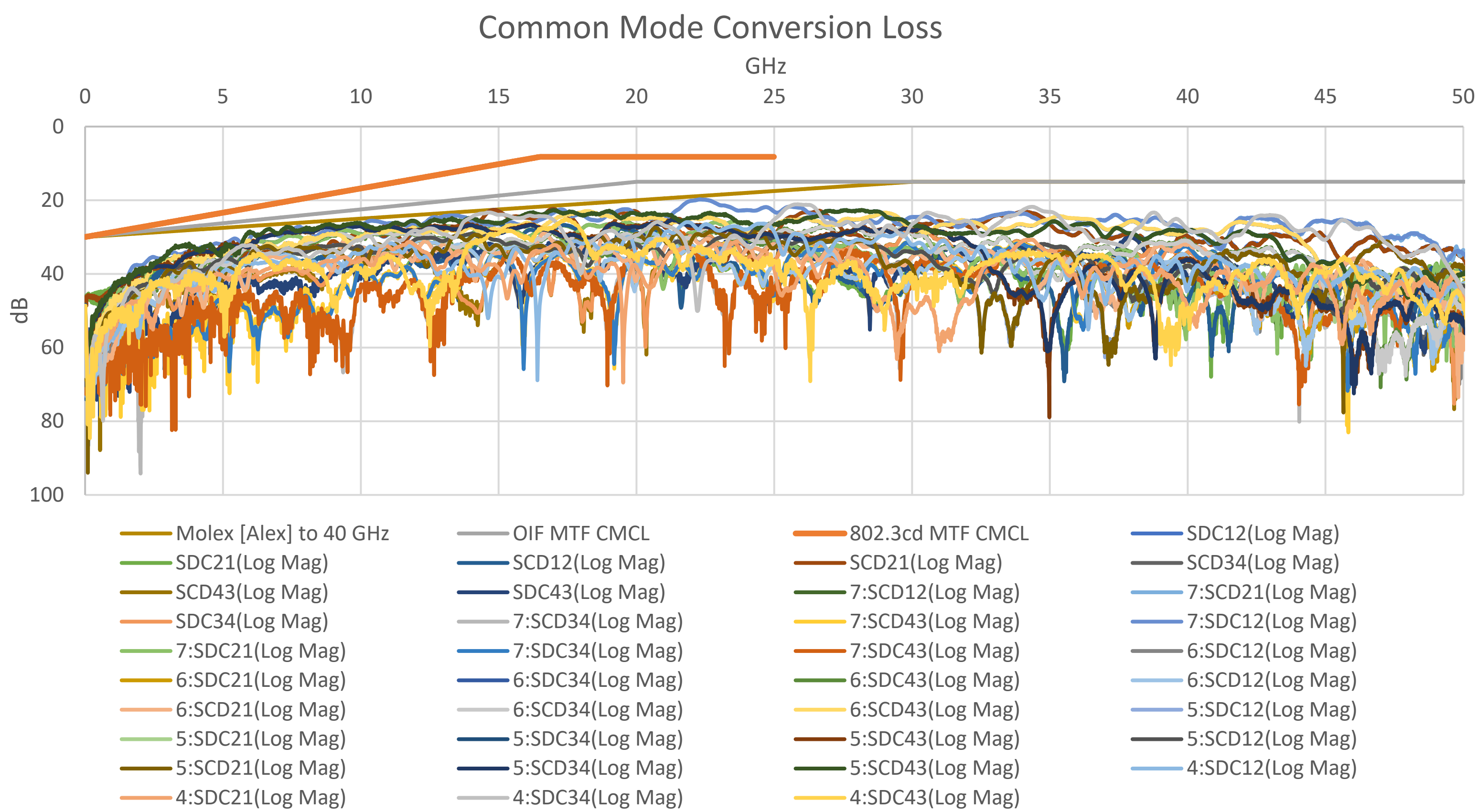
where

$CMCIL(f)$	is the common-mode conversion insertion loss in dB at frequency f
f	is the frequency in GHz

The mated test fixtures common-mode conversion insertion loss is illustrated in Figure 162B–5.

- *CMCIL(f)≥ TBD*

MTF Common Mode Conversion Loss



Common Mode Conversion Loss =

$30-0.5*f_{GHz}$ 0.01/0.05 TBD GHz ≤ f_{GHz} < 30 GHz

15 30 GHz ≤ f_{GHz} ≤ 40/50 TBD GHz

OIF

- MTF MIN () = -30+(21/28)*f (dB) 50MHz < f < 20GHz
- MTF MIN () = -3 (dB) 20MHz < f < 58GHz

Mated test fixtures

- **162B.1.3.1 Mated test fixtures differential insertion loss**

The FOM_{ILD} is calculated according to 93A.4 with f_b=53.125 GHz, T_t=(TBD) ps, and f_r=0.75 × f_b. The fitted insertion loss and insertion loss deviation are computed over the range f_{min}=0.01 GHz to f_{max}=40 GHz. FOM_{ILD} shall be less than (TBD) dB.

  - f_{max}=?
  - FOM_{ILD} = TBD
  - T_{max}= TBD

162B.1.3.2 Mated test fixtures differential return loss

The differential return loss of the mated test fixtures measured at each test fixture interface shall meet the values determined using Equation (162B–6).

$$DRL(f) \geq \{TBD\} \quad (162B\text{–}6)$$

for 0.01 GHz ≤ f ≤ 50 GHz

where

$DRL(f)$	is the differential return loss in dB at frequency f
f	is the frequency in GHz

The mated test fixtures differential return loss is illustrated in Figure 162B–4.

Mated test fixtures

162B.1.3.6 Mated test fixtures integrated crosstalk noise

The SFP112 mated test fixture integrated near-end crosstalk noise voltage for the disturber near-end crosstalk loss is determined according to the method in 110B.1.3.7 using the parameters shown in Table 162B–1 and shall meet the specification in Table 162B–2.

Table 162B–1—SFP112 mated test fixture integrated near-end crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	53.125	GBd
3 dB reference receiver bandwidth	f_r	39.84	GHz
Near-end disturber peak differential output amplitude	A_{nt}	TBD	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	TBD	ps

Table 162B–2—SFP112 mated test fixture integrated near-end crosstalk noise voltage

Parameter	Value	Units
Integrated near-end crosstalk noise voltage	Less than TBD	mV

Mated test fixtures

Table 162B–3—Multi-lane mated test fixture integrated crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	53.125	GBd
3 dB reference receiver bandwidth	f_r	39.84	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	TBD	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	TBD	ps

Table 162B–4—Multi-lane mated test fixture integrated crosstalk noise

Parameters	Value	Units
MDFEXT integrated crosstalk noise voltage	less than TBD	mV
MDNEXT integrated crosstalk noise voltage	less than TBD	mV
Total integrated crosstalk noise voltage	less than TBD	mV

162B.1.1.6 Mated test fixtures (ICN) Tables

Description	Symbol	Value	Units
Symbol rate	f_b	53.125	GBd
3dB reference receiver bandwidth	f_r	39.84	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	TBD	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	TBD	ps

Comment#181

- Proposals for 162.11 Cable assembly characteristics
- Provide specifications for TBDs;

Table 162–14—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 26.56 GHz	162.11.2	19.75	dB
Minimum insertion loss at 26.56 GHz	162.11.2	11	dB
Minimum cable assembly ERL[a]	162.11.3	TBD	dB
Differential to common-mode return loss	162.11.4	TBD	dB
Differential to common-mode conversion loss	162.11.5	TBD	dB
Common-mode to common-mode return loss	162.11.6	TBD	dB
Minimum COM	162.11.7	3	dB

[a]Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

Cable assembly specifications

162.11.2 Cable assembly insertion loss

The measured insertion loss of a cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in TBD and illustrated in TBD.

The measured insertion loss at 26.56 GHz of a cable assembly shall be less than or equal to 19.75 dB.

Cable assembly specifications

162.11.3 Cable assembly ERL

ERL of the cable assembly at TP1 and at TP4 are computed using the procedure in 93A.5 with the values in Table 162–15. Parameters that do not appear in Table 162–15 take values from Table 162–16. The value of T_{fx} is twice the delay from TP1 or TP4 to the connector of the specific cable assembly test fixture. Note that test fixtures are specified in 162B.1.

Table 162–15—Cable assembly ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	TBD	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	7000	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI

Cable assembly ERL at TP1 and at TP4 shall be greater than or equal to TBD dB for cable assemblies that have a COM less than 4 dB.

Cable assembly specifications

162.11.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet the requirements of TBD.

162.11.5 Differential to common-mode conversion loss

The cable assembly differential to common-mode conversion loss shall meet the requirements of TBD.

162.11.6 Common-mode to common-mode return loss

The cable assembly common-mode to common-mode return loss shall meet the requirements of TBD.

Cable assembly specifications

162.11.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 162.11.7.1 and the procedure in 93A.1, where T_r is TBD ps for $H_t(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 162D), as described in 162.11.7.2.

COM parameter values for the three cable assembly types are provided in Table 162–16.

Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. COM for any channel within the cable assembly shall be greater than or equal to 3 dB for both Test 1 and Test 2.

Cable assembly specifications

Table 162–16—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	53.125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model			
Single-ended device pad capacitance	C_d	1.2×10^{-4}	nF
Single-ended device series inductance	L_s	0.12	nH
Single-ended device bump capacitance	C_b	0.3×10^{-4}	nF
Transmission line length, Test 1	z_p	12	mm
Transmission line length, Tx Test 2	z_p	31	mm
Transmission line length, Rx Test 2	z_p	29	mm
Single-ended package capacitance at package-to-board interface	C_p	8.7×10^{-5}	nF
Transmission line characteristic impedance	Z_c	87.5	Ω
Transmission line 2 length	z_{p2}	1.8	mm
Transmission line 2 characteristic impedance	Z_{c2}	92.5	Ω
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz

Cable assembly specifications

Table 162–16—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.54	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.34 0 0.02	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.12 0.02	—
Transmitter equalizer, 3rd pre-cursor coefficient Minimum value Maximum value Step size	$c(-3)$	 –0.06 0 0.02	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.2 0 0.02	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB

Cable assembly specifications

Table 162–16—COM parameter values *(continued)*

Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	f_b / 2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 2.5 f_b	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	f_b / 80	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.413 0.413 0.608	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	TBD	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ for $n = 3$ to N_b	$b_{max}(n)$	 0.85 0.3 0.2	—
Number of DFE floating tap banks	N_{bg}	3	
Number of DFE floating taps per bank	N_{bf}	3	

Comment#183

- **Proposals for 162A Annex 162A TP0 and TP5 test point parameters and channel characteristics TBDs**

162A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are specified in TBD and TBD, respectively.

Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards with allowances for ball grid array (BGA) footprint and host connector footprints is 6.875 dB at 26.56 GHz and the recommended minimum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 2.3 dB at 26.56 GHz. The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss from TP0 to TP2 or TP3 to TP5 given in TBD and an assumed mated connector loss of 1.6 dB.

Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.975 dB at 26.56 GHz.