

C2C Channel Equalization with Several Eta0

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Overview

❑ C2C COM analysis

- 4 Lim channels between 16.5 to 17.5 dB loss
- 1 Gore PCB channel with 20 dB loss
- 1 Gore cabled channel with 20 dB loss

❑ Equalizer considered 6T DFE

- Results are with 1x, 2.5x, 5x, and 10x of η_0 ($8.2e-9$) for more representative receive noise
- Case I - [13, 11] mm package
- Case II – [31, 29] mm package

❑ COM 2.9.3 key difference with COM 2.7.6

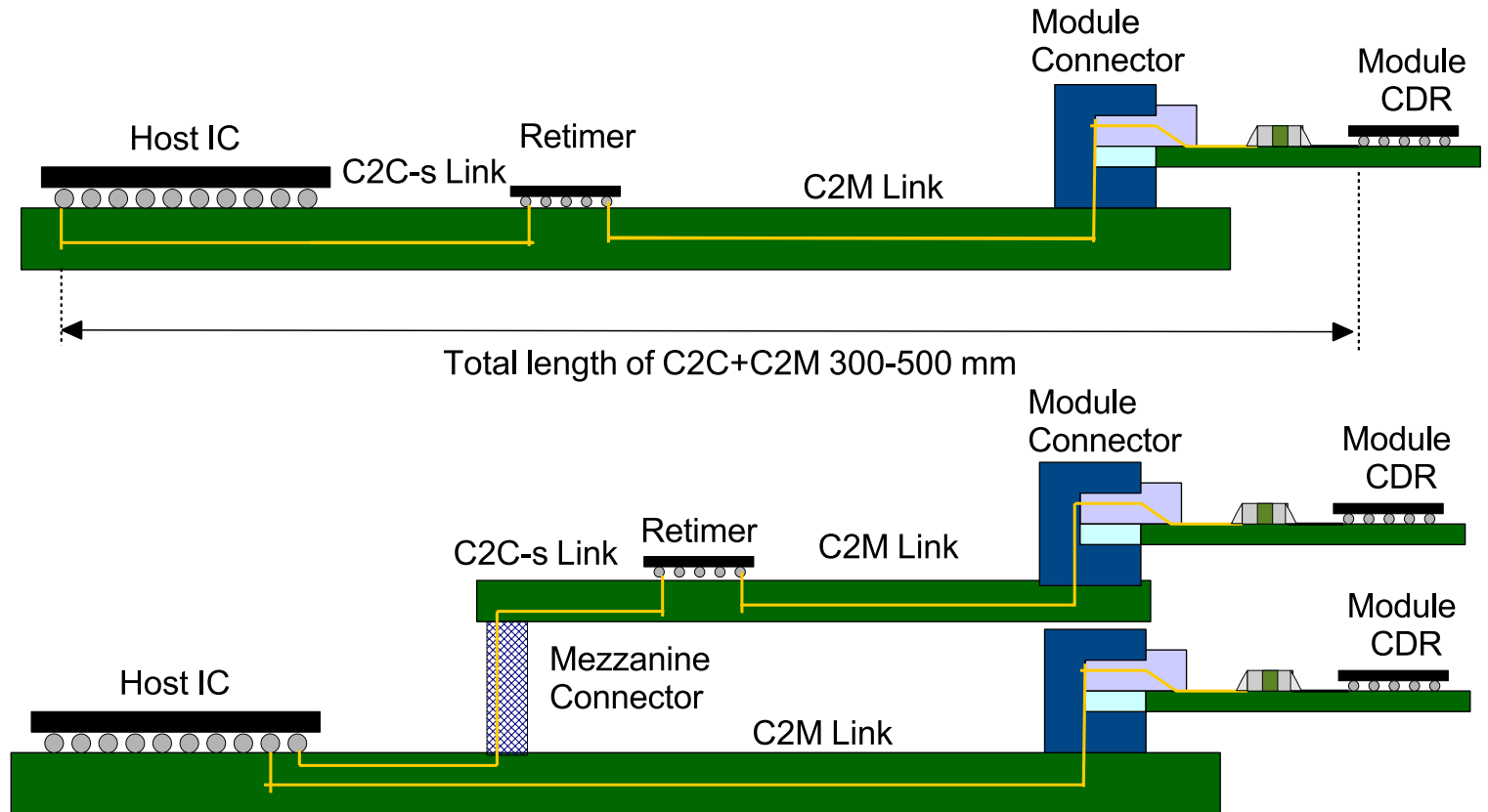
- ERL result with COM 2.9.3 are 3-8 dB lower than ERL results from COM 2.7.6

❑ Addressing comments xyz.

Two Common C2C Applications

□ These two common C2C applications can be satisfied with ~300 mm trace and by repurposing 16 dB C2M budget

- Connecting to far-side of the ASIC IO may require retimer
- Modules mounted on mezzanine card.



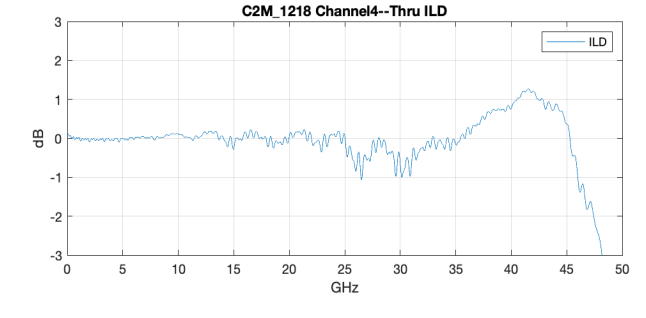
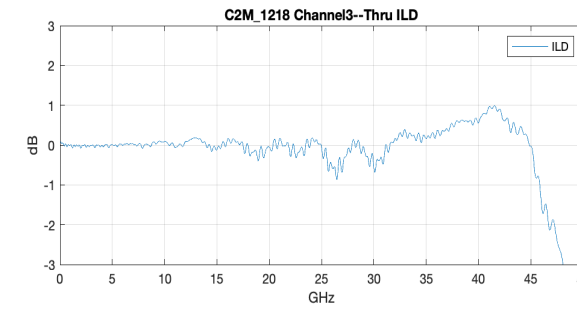
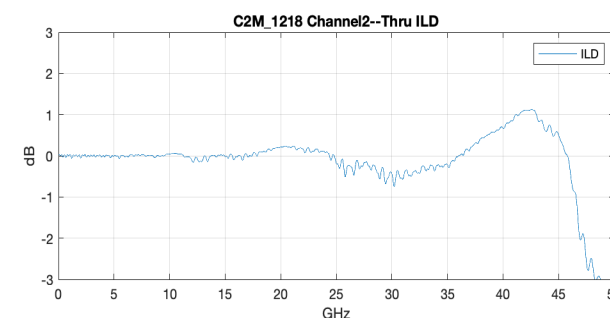
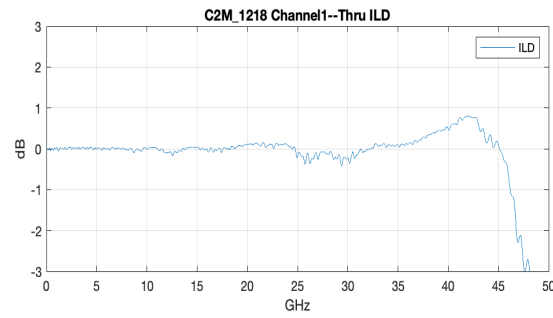
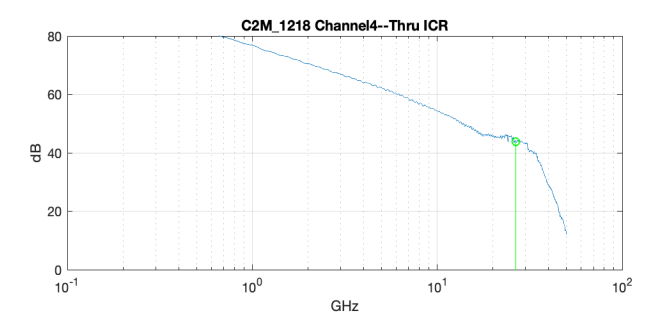
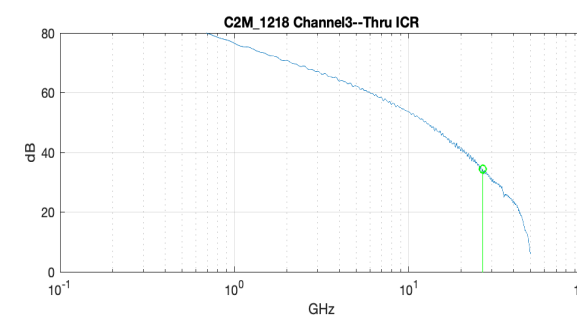
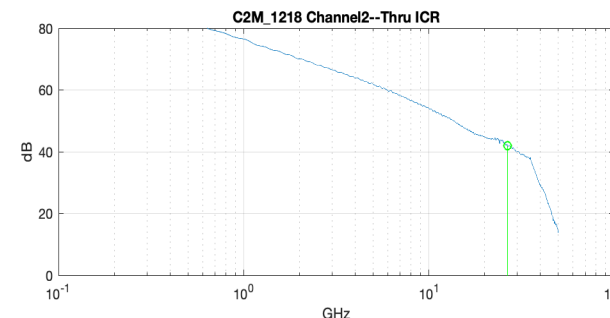
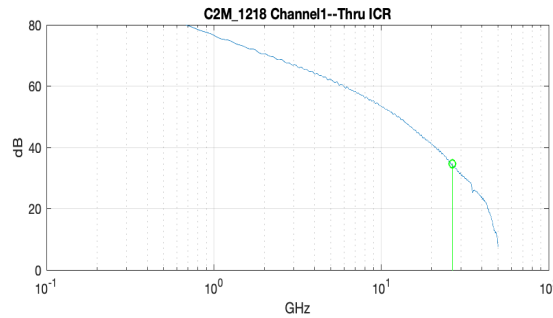
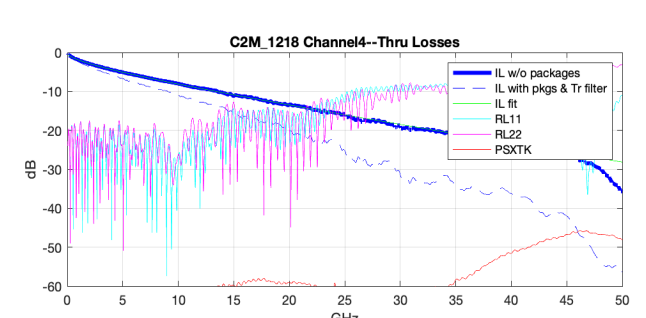
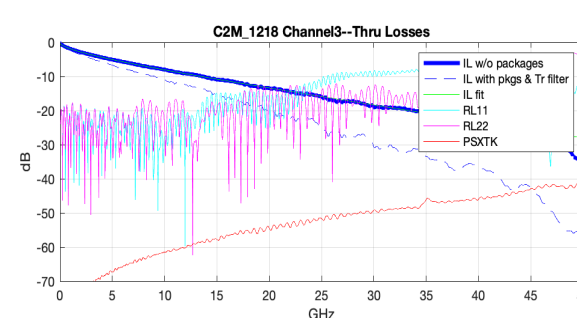
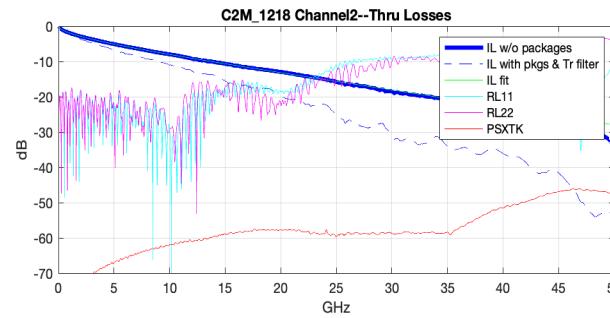
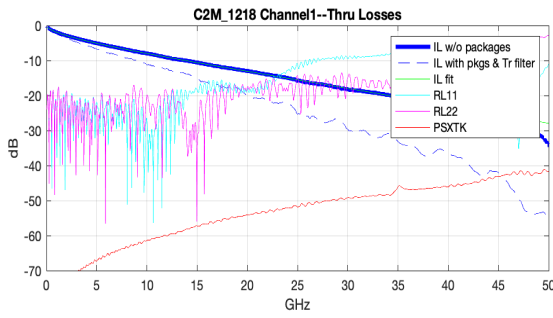
COM 2.9.3 Table for C2C

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0.0009909 0.0002772]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]	RESULT_DIR	.\results\100GEL_KR_{date}\		benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
L_s	[0.12, 0.12]	nH	[TX RX]	SAVE_FIGURES	0	logical	Table 92-12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	Port Order	[1 3 2 4]		Parameter	Setting	
z_p select	[1 2]		[test cases to run]	RUNTAG	KR_eval_		board_tl_gamma0_a1_a2	[0.3.8206e-04 9.5909e-05]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[11 29; 1.8 1.8]	mm	[test cases]	Operational			board_Z_c	100	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (TX)	110.3	mm
z_p (RX)	[11 29; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (NEXT)	110.3	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	DER_0	1.00E-05		z_bp (FEXT)	110.3	mm
R_0	50	Ohm		T_r	0.006160714	ns	z_bp (RX)	110.3	mm
R_d	[50 50]	Ohm	[TX RX]	FORCE_TR	1	logical	C_0	[0.29e-4]	nF
A_v	0.413	V		Local Search	2		C_1	[0.19e-4]	nF
A_fe	0.413	V		TDR and ERL options			Include PCB	0	logical
A_ne	0.608	V		TDR	1	logical	Floating Tap Control		
L	4			ERL	1	logical	N_bg	0	0 1 2 or 3 groups
M	32			ERL_ONLY	0	logical	N_bf	0	taps per group
filter and Eq				TR_TDR	0.01	ns	N_f	40	UI span for floating taps
f_r	0.75	*fb		N	2000		bmaxg	0.05	max DFE value for floating taps
c(0)	0.54		min	beta_x	0		B_float_RSS_MAX	0.02	rss tail tap limit
c(-1)	[-0.34:0.02:0]		[min:step:max]	rho_x	0.618		N_tail_start	25	(UI) start of tail taps limit
c(-2)	[0:0.02:0.12]		[min:step:max]	fixture delay time	[0 0]	[port1 port2]	ICN parameters		
c(-3)	[-0.06:0.02:0]		[min:step:max]	TDR_W_TXPKG	0		f_v	0.723	*Fb
c(1)	[-0.2:0.05:0]		[min:step:max]	N_bx	6	UI	f_f	0.723	*Fb
N_b	6	UI		Receiver testing			f_n	0.723	*Fb
b_max(1)	0.85			RX_CALIBRATION	0	logical	f_2	39.844	GHz
b_max(2..N_b)	0.2			Sigma BBN step	5.00E-03	V	A_ft	0.600	V
b_min(1)	-0.85			Noise, jitter			A_nt	0.600	V
b_min(2..N_b)	-0.2			sigma_RJ	0.01	UI	TBD in document under consideration		
g_DC	[-20:1:0]	dB	[min:step:max]	A_DD	0.02	UI	new		
f_z	21.25	GHz		eta_0	0.000000082	V^2/GHz			
f_p1	21.25	GHz		SNR_TX	33	dB			
f_p2	53.125	GHz		R_LM	0.95				
g_DC_HP	[-4:1:0]		[min:step:max]						
f_HP_PZ	0.6640625	GHz							

Lim C2C Channels

- **Total of 4 channels were built with optimized host ASIC, retimer & mezzanine connector footprint (shallow via breakout). Both shallow and long via are considered at connector and retimer footprint.**
 - Channel 1: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
 - Channel 2: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (long via); including 2 FEXT & 2 NEXT
 - Channel 3: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
 - Channel 4: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (long via) ; including 2 FEXT & 2 NEXT
 - http://www.ieee802.org/3/ck/public/tools/c2c/lim_3ck_05_0719_c2c.zip.

Lim C2C Channels



COM Summary for Lim C2C Channels for Several Eta_0

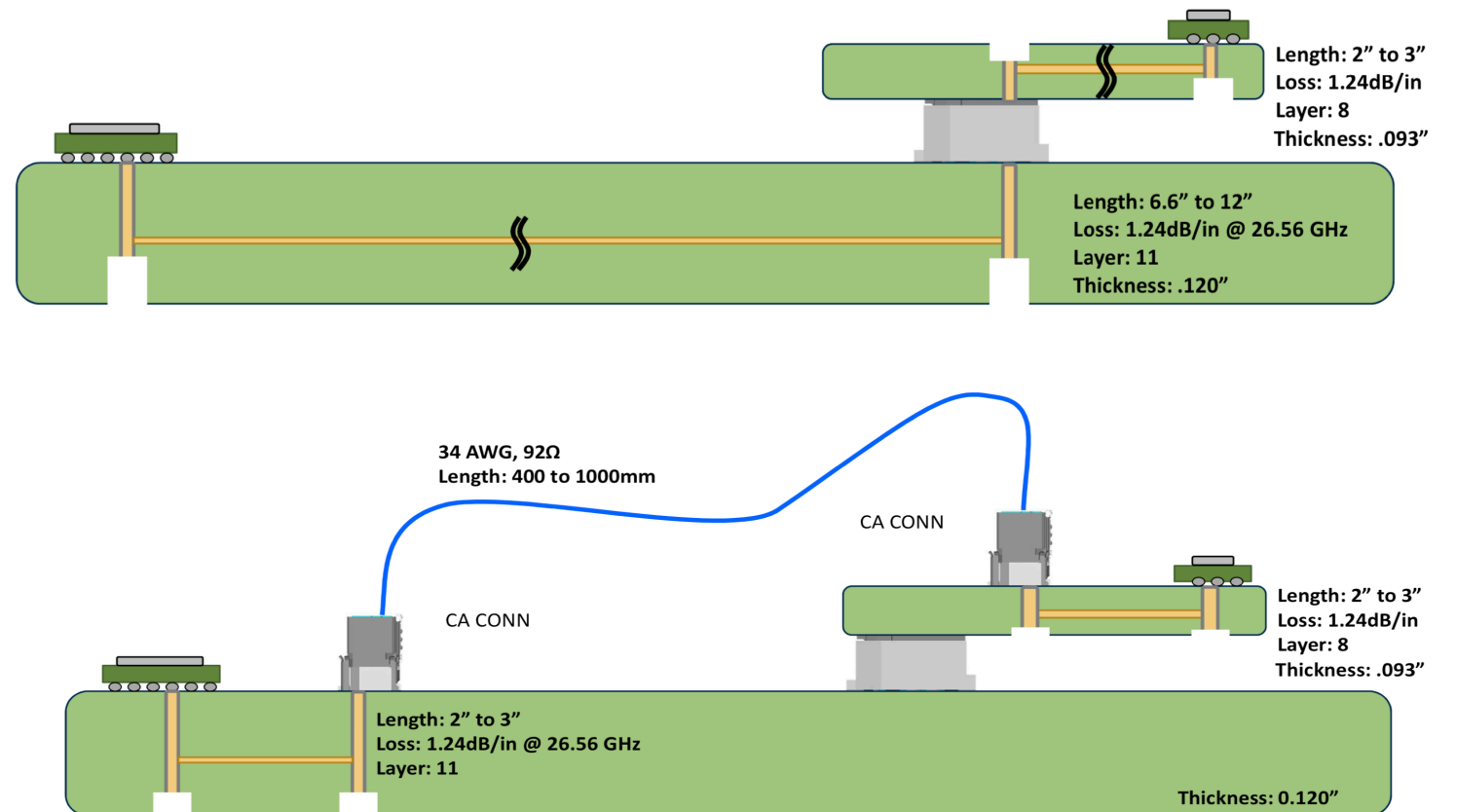
Lim C2C Channel 1	Eta_0 Noise (V ² /GHz)	Actual DFE Taps (Largest taps case I or II)	Fitted IL at 26.55 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	COM Case I	COM Case II
Lim C2C Channel 1 FOM ILD=0.06 ICN=1.87 mV ERL11=14.1 (18.4)* ERL22=13.4 (17.4)*	1x=8.2E-9	[0.346, 0.061, 0.052, 0.033, 0.032, 0.007]	16.6	24.7	4.2	5.1
	2.5x=2.05E-8	[0.356, 0.03, 0.008, 0.012, 0.021, 0.004]	16.6	24.0	3.9	4.3
	5x=4.1E-8	[0.455, 0.04, 0.028, 0.025, 0.03, 0.009]	16.6	24.0	3.4	3.5
	10x=8.2E-8	[0.50, 0.08, 0.05, 0.038, 0.038, 0.015]	16.6	25.4	2.7	2.2
Lim C2C Channel 2 FOM ILD=0.095 ICN=1.34 mV ERL11=14.0 (18.4)* ERL22=13.1 (16.2)*	1x=8.2E-9	[0.385, -0.012, 0.012, 0.004, 0.025, 0.012]	16.4	28.2	5.1	5.3
	2.5x=2.05E-8	[0.442, 0.007, 0.008, 0.013, 0.025, 0.013]	16.4	28.2	4.6	4.5
	5x=4.1E-8	[0.487, 0.032, 0.035, 0.016, 0.033, 0.018]	16.4	28.2	3.9	3.6
	10x=8.2E-8	[0.53, 0.07, 0.058, 0.03, 0.041, 0.024]	16.4	28.2	3.1	2.3
Lim C2C Channel 3 FOM ILD=0.108 ICN=1.81 mV ERL11=13.1 (17.3)* ERL22=12.5 (15.4)*	1x=8.2E-9	[0.322, -0.067, -0.036, -0.069, 0.009, -0.007]	16.7	27.4	3.7	4.5
	2.5x=2.05E-8	[0.42, -0.028, -0.02, 0.003, 0.016, 0.002]	16.7	27.4	3.4	3.9
	5x=4.1E-8	[0.518, 0.144, 0.086, 0.058, 0.046, 0.014]	16.7	27.4	3.1	3.02
	10x=8.2E-8	[0.53, 0.07, 0.058, 0.03, 0.041, 0.024]	16.7	27.4	2.4	1.8
Lim C2C Channel 4 FOM ILD=0.125 ICN=1.18 mV ERL11=13.0 (17.1)* ERL22=11.2 (14.4)*	1x=8.2E-9	[0.322, -0.067, -0.036, -0.069, 0.009, -0.007]	16.8	29.3	4.6	4.7
	2.5x=2.05E-8	[0.45, -0.038, -0.015, -0.006, 0.019, 0.007]	16.7	27.4	4.2	4.1
	5x=4.1E-8	[0.49, 5e-4, 0.007, 0.006, 0.027, 0.012]	16.7	27.4	3.7	3.2
	10x=8.2E-8	[0.64, 0.06, 0.03, 0.02, 0.037, 0.021]	16.7	27.4	2.8	1.9

* ERL results with COM 2.7.6 are lower.

Gore C2C Channels

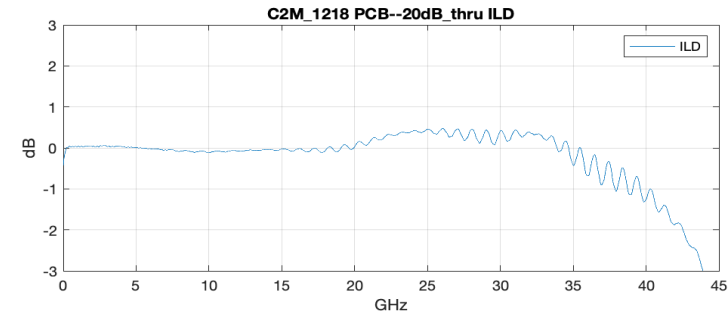
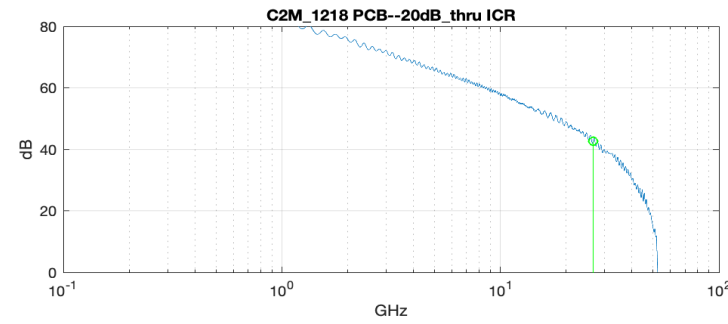
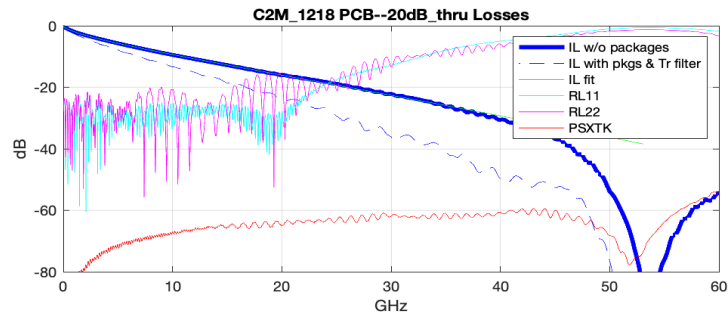
Construction of C2C channels based on PCB and cable construction provided by Brandon Gore

– http://www.ieee802.org/3/ck/public/19_05/gore_3ck_01a_0519.pdf

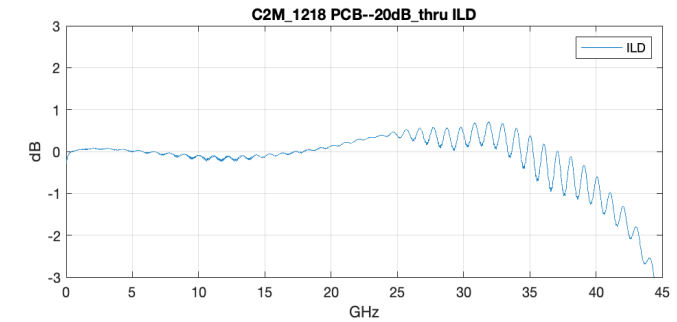
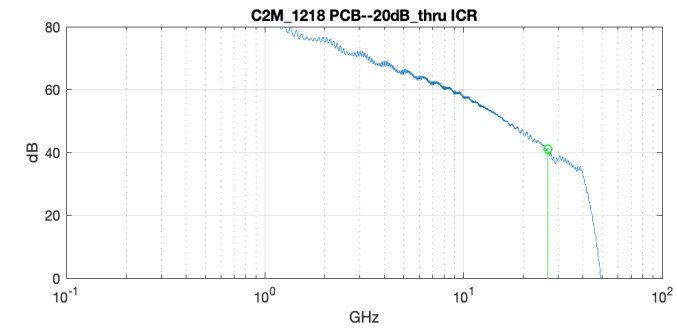
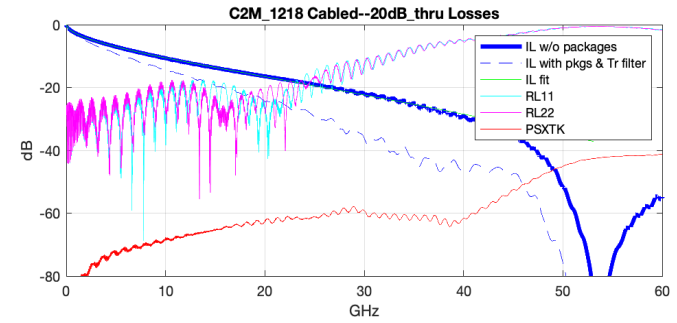


Gore C2C 20 dB Channels

PCB Channel



Cabled Channel



Core C2C Channel

Lim C2C Channel 1	Eta_0 Noise (V ² /GHz)	Actual DFE Taps (Largest taps case I or II)	Fitted IL at 26.55 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	COM Case I	COM Case II
Core C2C Channel 1 FOM ILD=0.13 ICN=0.69 mV ERL11=14.7 (22.8)* ERL22=14.9 (15.8)*	1x=8.2E-9	[0.331, -0.057, -0.036, -0.016, 0.003, -0.004]	20.2	30.1	5.3	5.3
	2.5x=2.05E-8	[0.53, 0.015, -0.013, -0.012, 0.02, -0.005]	20.2	30.1	4.5	4.1
	5x=4.1E-8	[0.53, 0.015, -0.013, -0.012, 0.02, -0.005]	20.2	30.1	3.6	2.8
	10x=8.2E-8	[0.65, 0.11, 0.04, 0.022, 0.042, 0.01]	20.2	30.1	2.4	1.1
Core C2C Channel 2 FOM ILD=0.118 ICN=0.69 mV ERL11=14.0 (22.8)* ERL22=13.1 (15.8)*	1x=8.2E-9	[0.385, -0.012, 0.012, 0.004, 0.025, 0.012]	20.2	30.1	5.1	4.9
	2.5x=2.05E-8	[0.428, -0.026, 0.016, -0.005, 0.011, 0.002]	20.2	30.1	4.3	3.6
	5x=4.1E-8	[0.428, 0.026, -0.016, 0.005, 0.011, 0.002]	20.2	30.1	3.3	2.2
	10x=8.2E-8	[0.54, 0.079, 0.05, 0.034, 0.035, 0.016]	20.2	30.1	1.9	0.4

* ERL results with COM 2.7.6 are lower.

Summary

- ❑ **Eta_0 of 8.2e-9 produces only 0.577 mV RMS noise assuming 40 GHz BW which is several time lower than practical low power C2C receiver**
- ❑ **The analysis considered several eta_0 values for Lim and Gore channels**
 - 1x currently in draft 1.2 - all Lim and Gore Channels pass with significant margin above 3 dB COM
 - 2.5x 0.3-1 dB of COM penalty - all Lim and Gore Channels pass 3 dB COM
 - 5.0x 1- 2 dB of COM penalty – all Lim Channels pass 3 dB COM but some instance of Gore channel fail 3 dB COM
 - 10x 2-4 dB of COM penalty – Both Lim and Gore channels fail 3 dB COM
 - Eta_0 COM penalty is somewhat higher because Lim channels have an ICN<1.87 mV and Gore channels ICN are <0.7 mV
- ❑ **Recommend to go with eta_0=4.1E-8 (5x) for C2C which equates to about 1.3 mV of RMS noise**
 - C2M also uses the same eta_0=4.1E-8.