C2M Methodology, CTLE Gain, and DFE Taps

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July 7, 2020

Overview

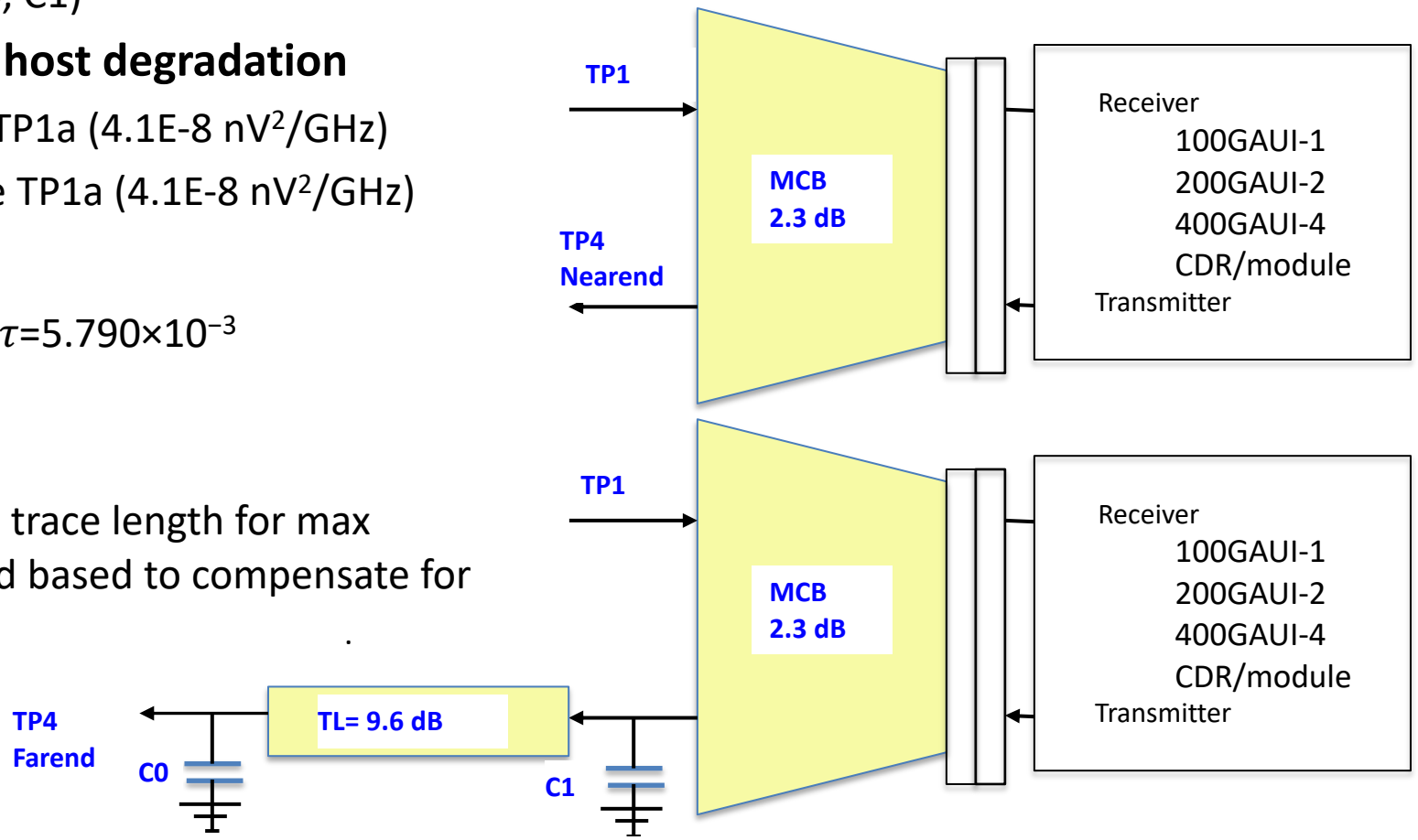
- **Module to ASIC test methodology option**
  - Measured naked
  - Use CR (C0, C1) to account for long barrel vias
  - Increase eta_0 to account for long barrel vias
- **Module output measurement test points**
- **COM analysis at TP4 nearend and farend**
- **Penalty associated from fixed module TX FIR**
- **Addressing D1.2 comments 191, 192, 193, 194, 195, 196, 197, 201, 202, 211, 212.**

Module to ASIC Test Methodology Comments 211 and 212

- **Unlike ASIC-Module the Module-ASIC output at TP4 and TP5 measured with compliance board and reference trace typically has COM >6 dB dB with 4T DFE receiver**
  - If one replaces module compliance board with realistic host with long barrel via and a short stub then COM can drop by ~ 2 dB
  - COM can drop to 2-3 dB for realistic channel if one include the ASIC package
- **The method of benartsi_3ck_01a_0719 for CR link have been studied for module-chip TP4/farend measurements with (C0, C1)= (29, 19 fF)**
  - TP4 is measured directly without C0/C1
  - TP4 farend is measured with C0/C1
  - Benartsi method applied to C2M require C0/C1 be cascaded with the module S4P but actual measurement ignores the interaction between module and C0-TL-C1
  - C0-TL-C1 in effect is a low pass filter plus some interaction between C0-C1
- **An alternate method without above issue and sensitivity to reflection is to increase eta_0 to account for realistic board implementation without using (C0, C1)**
  - Eta_0 increased to 4x of TP1a noise (4.1E-8) at TP4 nearend to account for the host
  - Eta_0 increased to 2x of TP1a noise (4.1E-8) at TP4 farend account for the host.

TP4 Nearend and Farend Test Methods Comments 211 and 212

- **Option I - Benartsi method**
  - TP4 nearend measured directly
  - TP4 farend measured with addition of (C0, C1)
- **Option II – Increase eta_0 to account for host degradation**
  - TP4 near end measured with eta_0 4x of TP1a (4.1E-8 nV^2/GHz)
  - TP4 farend measured with eta_0 2x of the TP1a (4.1E-8 nV^2/GHz)
- **Transmission line parameters**
  - $\gamma 0=0$, $a1 = 3.8206\times10^{-4}$, $a2 = 9.5909\times10^{-5}$, $\tau = 5.790\times10^{-3}$
  - TP4 is MCB output measurement
  - TP4 is measured at MCB output
  - TP5 is measured with addition of 244 mm trace length for max channel loss (trace length may be adjusted based to compensate for MCB loss deviation from 2.3 dB)



COM 2.9.3 Module to Host (CDR PKGs 2, 7, 8 mm)

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.1	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nF	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2 3]		[test cases to run]
z_p (TX)	[2 7 8]	mm	[test cases]
z_p (NEXT)	[2 7 8]	mm	[test cases]
z_p (FEXT)	[2 7 8]	mm	[test cases]
z_p (RX)	[0 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.72		min
c(-1)	-0.18		[min:step:max]
c(-2)	0.04		[min:step:max]
c(1)	-0.04		[min:step:max]
N_b	4	UI	
b_max(1)	0.3		
b_max(2..N_b)	0.1		
g_DC	[-14:1:-4]	dB	[min:step:max]
f_z	12.5	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:-1]		[min:step:max]
f_HP_PZ	1.3275	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.15		
ffe_backoff	1		

0.7

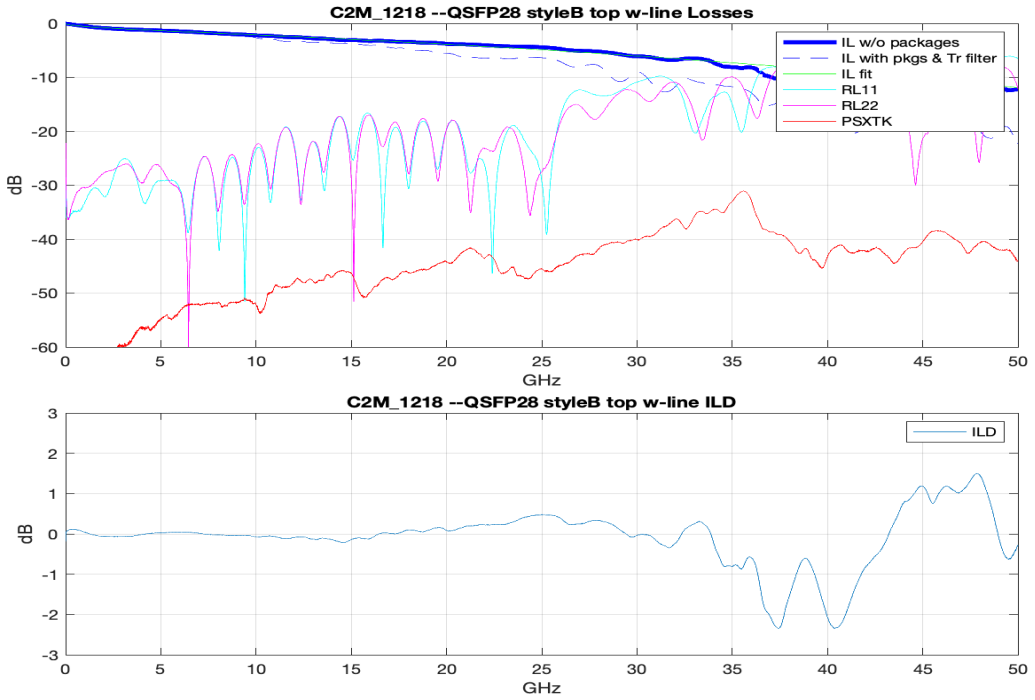
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	0.0000E+00	
rho_x	0.618	
fixture delay time	[0 0]	port1 port2]
TDR_W_TXPKG	1	
N_bx	4	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	0.000000041	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5]	Ohm

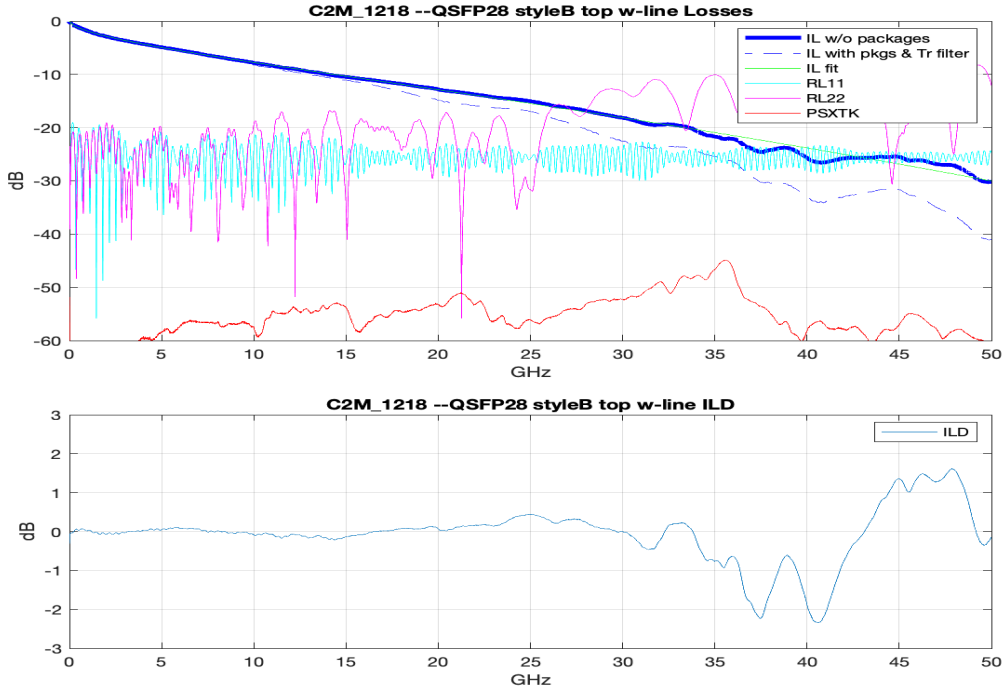
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*68*	mm
z_bp (NEXT)	*68*	mm
z_bp (FEXT)	*68*	mm
z_bp (RX)	*1*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**1**	**logical**
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	2	taps per group
N_f	12	UI span for floating taps
bmaxg	0.1	DFE value for floating
B_float_RSS_MAX	**0.03**	rss tail tap limit
N_tail_start	**25**	UI) start of tail taps limi
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.825	GHz
A_ft	0.410	V
A_nt	**0.600**	V
heck_3ck_03b_0319	**Adopted Mar 2019**	**kasapi_3ck_02_1119**
walker_3ck_01d_0719	**Adopted July 2019**	**Adopted Nov 2019**
result of R_d=50		under consideration
benartsi_3ck_01a_0719	**no used for KR**	
mellitz_3ck_03_0919		

TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

Mated board IL = 5.2 dB
Total IL with 8 mm PKG=8.0 dB



Mated board + 220 mm trace IL = 16.1 dB
Total IL with 8 mm PKG=18.6 dB



Yamaichi QSFP56 Mated Board Near End TP4

- **Mated board COM with addition of PCB trace and C0/C1***
  - Having a fixed single TX FIR setting result in only ~0.5 dB of penalty at TP4 as the TX FIR is set for half way
  - DFE B1-B4<|0.05|.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II/III	EW UI Case I/II/III	VEC dB Case I/II/III	COM dB Case I/II/III
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=13.9 (15.1)* dB ERL22=10.8 (11.2)* dB Optimum TX FIR	HCB-MCB (eta0 5x)	5.2	7.3	57/40/54	0.19/0.16/0.19	7.0/9.2/6.9	5.1/3.7/5.3
	HCB-MCB (eta0 20x)	5.2	7.3	55/38/52	0.19/0.16/0.19	7.3/9.7/7.2	4.9/3.4/5.0
	+ 68 mm (eta0 5x)	8.7	10.3	42/40/44	0.22/0.16/0.19	5.9/7.3/6.2	6.2/4.9/5.9
	+68 mm+C0/C1 (eta0 5x)	8.9	11.0	43/32/40	0.19/0.13/0.19	6.5/9.0/6.8	5.6/3.8/5.3
	+68 (eta0 20x)	8.7	10.4	44/38/41	0.19/0.16/0.19	6.4/7.9/6.8	5.6/4.5/5.3
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=13.9 (15.1)* dB ERL22=10.8 (11.2)* dB TX FIR [0.04 -0.18 0.72 -0.04]	HCB-MCB (eta0 5x)	5.2	7.3	48/34/46	0.19/0.16/0.19	7.5/10/7.4	4.7/3.3/4.8
	HCB-MCB (eta0 20x)	5.2	7.3	45/32/48	0.19/0.16/0.19	7.9/10.5/7.9	4.5/3.1/4.5
	+ 68 mm (eta0 5x)	8.7	10.3	43/34/39	0.19/0.16/0.19	6.1/7.9/6.3	6.0/4.5/5.7
	+68 mm+C0/C1 (eta0 5x)	8.9	11.0	40/27/36	0.19/0.16/0.19	6.5/9.6/7.1	5.5/3.5/5.1
	+68 mm (eta0 20x)	8.7	10.4	41/31/36	0.19/0.16/0.19	6.7/8.6/7.1	5.4/4.0/5.1

* ERL with COM 2.76 were higher.

Yamaichi QSFP56 Mated Far End TP5 Results

- **Mated board COM with addition of PCB trace and C0/C1***
  - Addition of C0/C1 reduces COM by 0.3-0.4 dB and the same can be done by increasing eta_0 to 10x
  - Having a fixed single TX FIR setting result in only ~0.2 dB of penalty as the 4T DFE does a better job for under emphasis
  - DFE B1max<0.3, B2-B4<0.03.

Channel	Configuration	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=13.9 (14.6) dB ERL22=10.8 (10.7) dB Optimum TX FIR	+215mm (eta0 5x)	16.2	17.6	25/21/23	0.19/0.16/0.19	6.1/7.3/6.5	5.9/4.9/5.6
	+215mm +C0/C1 (eta0 5x)	16.0	18.1	22/19/21	0.19/0.16/0.19	6.5/7.9/6.9	5.6/4.5/5.2
	+215mm (eta0 10x)	15.8	17.6	25/22/23	0.19/0.16/0.19	6.6/7.6/6.9	5.5/4.7/5.2
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=13.9 (14.6)* dB ERL22=10.8 (10.8)* dB TX FIR [0.04 -0.18 0.72 -0.04]	+215mm (eta0 5x)	16.3	18.7	25/21/23	0.19/0.16/0.19	6.1/7.2/6.5	5.9/4.9/5.6
	+215mm +C0/C1 (eta0 5x)	16.3	19.6	24/19/21	0.19/0.16/0.19	6.5/8.8/6.9	5.6/4.4/5.2
	+215mm (eta0 10x)	16.2	17.6	23/19/21	0.19/0.16/0.19	6.7/8/7.2	5.3/4.4/5.0

* ERL with COM 2.76 were higher.

COM Analysis on Lim TP4 Nearebd Channels 1a/2a

- **Lim TP4 QSFP-dd channels similar to an MCB output**
  - TP4 output are measured with eta_0 5x (4.1E-8) and 20x (1.64e-7) in order to account for host channels
  - Sub-optimum TX FIR has ~ 0.6 dB COM penalty as the TX FIR is set for half way through the channel
  - DFE [B1-4]max<0.05.

Channel	TX Setting/Noise	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Lim Channel 1a TP4 FOM ILD = 0.113 ICN = 2.1 mV ERL11=11.7 dB, ERL22=10.3 dB	Optimum eta0 5x	5.4	6.7	80/62/78	0.25/0.19/0.25	5.6/7.6/5.4	6.4/4.7/6.7
	Fixed* eta0 5x	5.4	6.7	57/45/60	0.22/0.19/0.22	6.8/9.0/6.5	5.3/3.7/5.6
	Optimum eta0 20x	5.4	6.7	69/49/68	0.22/0.16/0.22	6.1/8.6/5.9	6.0/4.0/6.2
	Fixed* eta0 20x	5.4	6.7	54/42/57	0.19/0.19/0.19	7.2/9.6/6.8	5.0/3.5/5.2
Lim Channel 2a TP4 FOM ILD = 0.13 ICN = 3.7 mV ERL11=10.7 dB, ERL22=9.2 dB	Optimum eta0 5x	6.0	8.2	57/40/50	0.19/0.19/0.19	6.0/9.1/6.8	6.0/3.7/5.3
	Fixed* eta0 5x	6.0	8.2	56/35/48	0.19/0.16/0.19	6.1/9.9/6.9	5.9/3.4/5.2
	Optimum eta0 20x	6.0	8.2	60/38/48	0.19/0.16/0.19	6.4/9.6/7.2	5.7/3.5/5.0
	Fixed* eta0 20x	6.0	8.2	53/33/46	0.19/0.16/0.19	6.5/10.5/7.4	5.6/3.1/4.8

*** TX FIR [0.04 -0.18 0.72 -0.04]**

COM Analysis on Lim TP4 Farend

- **Lim TP4 channels 1a/2a measured with eta_0 10x, but Lim channel 1b/2b which include host mid-depth via and BGA foot print is measured with eta_0 5x**
  - Fixed TX FIR penalty is ~0.3 dB excluding case II (7 mm) which causes pathological standing wave
  - DFE B1max<0.3, B2-B4<0.07.

Channel	TX Setting/Noise	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II/III	EW UI Case I/II/III	VEC dB Case I/II/II	COM dB Case I/ II/III
Lim Channel 1a TP4+210 mm FOM ILD = 0.12 ICN = 0.70 mV ERL11=11.7 dB, ERL22=10.3 dB	Optimum eta0 10x	16	17.5	25/22/23	0.19/01.9/0.19	6.2/7.5/6.5	5.8/4.8/5.6
	Fixed* eta0 10x	16	17.5	25/21/24	0.19/01.9/0.19	6.5/7.6/6.6	5.5/4.7/5.5
Lim Channel 2a TP4 +200 mm FOM ILD = 0.14 ICN = 1.3 mV ERL11=10.7 dB, ERL22=9.2 dB	Optimum eta0 10x	16.2	17.7	21/20/22	0.19/01.9/0.19	6.9/7.8/7.3	5.2/4.5/4.9
	Fixed* eta0 10x	16.2	17.7	23/20/20	0.19/0.19/0.19	7.1/7.9/7.5	5.0/4.5/4.8
Lim Channel 1b TP5 FOM ILD = 0.11 ICN = 1.8 mV ERL11=12.2 dB, ERL22=11.9 dB	Optimum eta0 5x	14.8	16.3	26/22/24	0.16/0.16/0.19	6.7/8.2/7.0	5.4/4.3/5.2
	Fixed* eta0 5x	14.8	16.3	24/21/24	0.19/0.16/0.19	7.1/8.4/7.1	5.1/4.2/5.0
Lim Channel 2b TP5 FOM ILD = 0.11 ICN = 1.7 mV ERL11=12.8 dB, ERL22=11.3 dB	Optimum eta0 5x	15.0	17.1	27/25/25	0.19/01.9/0.19	6.3/7.2/7.0	5.7/5.0/5.2
	Fixed* eta0 5x	15.0	17.1	28.1/25/25	0.19/01.9/0.19	6.5/7.4/7.0	5.6/4.8/5.2

*** TX FIR [0.04 -0.18 0.72 -0.04]**

COM Analysis on Lim Channel 1b and 2b – Module to ASIC at Slicer

- **Lim 9” host PCB with QSFP-dd connector, mid-depth via, and with ASIC foot printed included**
  - Given the Lim channel already include mid-depth via and ASIC foot print the eta_0 noise is kept at 5x (4.1E-8 nV^2/GHz)
  - Sub-optimum TX FIR has no more than 0.4 dB penalty
  - The 7 mm CDR package create pathological standing wave resulting in <3 dB COM similar issue has been observed at TP1a
  - DFE B1max<0.58, B2-B4<0.18.

Channel	TX Setting/Noise	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II/III	EW UI Case I/II/III	VEC dB Case I/II/II	COM dB Case I/ II/III
Lim Channel 1b TP5 FOM ILD = 0.11 ICN = 1.8 mV ERL11=12.2 dB, ERL22=11.9 dB	Optimum eta0 5x	14.8	19.2	22/14/20	0.16/0.09/0.13	7.2/12.7/9.5	5.0/2.3/3.5
	Fixed* eta0 5x	14.8	19.2	21/12/15	0.16/0.09/0.13	7.3/13.6/10.5	4.9/2.0/3.1
Lim Channel 2b TP5 FOM ILD = 0.11 ICN = 1.7 mV ERL11=12.8 dB, ERL22=11.3 dB	Optimum eta0 5x	15.0	19.8	22/16/18	0.16/0.13/0.13	6.8/11.6/9.5	5.3/2.6/3.5
	Fixed* eta0 5x	15.0	17.1	21/14/17	0.16/0.13/0.13	6.9/12.2/10.5	5.2/2.4/3.1

* TX FIR [0.04 -0.18 0.72 -0.04]

Response to Comment 191 and 193

- **The three method of measuring TP4 nearend/fareend are:**
  - Direct measurement – results measured are more optimistic and require tightening the limits
  - With addition of C0/C1 – true cascading is complex and result may have dependency based on MCB and C0/C1
  - Increase the eta_0 – increase eta_0 is accounting for the long barrel via and BGA crosstalk
    - More predictable VEC/VEO but the increase noise may not impair EW
    - This is the recommended method.

	Parameters	Direct Measurement Eta_0=4.1E-8	With addition of C0/C1	Nearend Eta_0=1.6E-7 Farend Eta_0=8.2e-8
TP4 Nearend Limits	VEC	7.5	8.5 dB	8.0 dB
	VEO	45	40 mV	40 mV
	EW	0.19	0.16	0.175 UI
TP4 Farend Limits	VEC	7.5	8.5 dB	8.5 dB
	VEO	22.5	20 mV	20 mV
	EW	0.19	0.16	0.175 UI

Summary of comments recommendation

- **DFE tap weight limit comment 195**
  - TP4 nearend
    - B1(max) ≤ 0.15 and B[2-4] ≤ 0.05
  - TP4 farend
    - B1(max) ≤ 0.375 and B[2-4] ≤ 0.08
- **VEO/VEC**
  - TP4 nearend
    - VEC= 7.5 dB comment 193
    - VEO=40 mV comment 191
  - TP4 farend
    - VEC=7.5 dB comments 194/197
    - VEO=20 mV comments 192/196

Response to Comment 201, 202

- **CTLE tap weights at TP1a as specified in D1.2 and the proposed TP4 nearend and farend CTLE gains.**

CTLE HF (dB)	CTLE LF (dB)	TP1a D1.2	TP4 Nearend	TP4 Farend
0				
-1				
-2	[0:0.5:-1]	✓	✓	✓
-3	[0:0.5:-1]	✓	✓	✓
-4	[0:0.5:-2]	✓	✓	✓
-5	[0:0.5:-2]	✓	✓	✓
-6	[0:0.5:-2]	✓	-	✓
-7	[0:0.5:-2]	✓	-	✓
-8	[0:0.5:-3]	✓	-	✓
-9	[0:0.5:-3]	✓	-	✓
-10	[1:0.5:-3]	✓	-	✓
-11	[1:0.5:-3]	✓	-	-
-12	[1:0.5:-3]	✓	-	-
-13	[2:0.5:-3]	✓	-	-

Summary

- **Propose module output measurement**
  - TP4 measured directly
  - TP5 measured with addition of addition of CR (C0, C1) caps + ~244 mm trace
- **Module TX FIR is set based for a nominal setting such that TP4 and TP5 are met**
  - The data here indicate with single TX FIR setting can satisfy eye opening from min-max channel loss
  - The penalty associated with fix TX FIR is low enough (<0.5 dB) that we can greatly simplify the module-ASIC bring up and operation
- **For Lim and Yamaichi MCB/HCB if one constructs module-ASIC link the COM at slicer can be as low as 2.0 dB with 4T DFE due to short package reflection, which is similar to what has been observed on the ASIC-Module direction**
  - ASIC SerDes either would have to operate with as high as 13.6 dB VEC.