C2M module output spec at TP4

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Contributor

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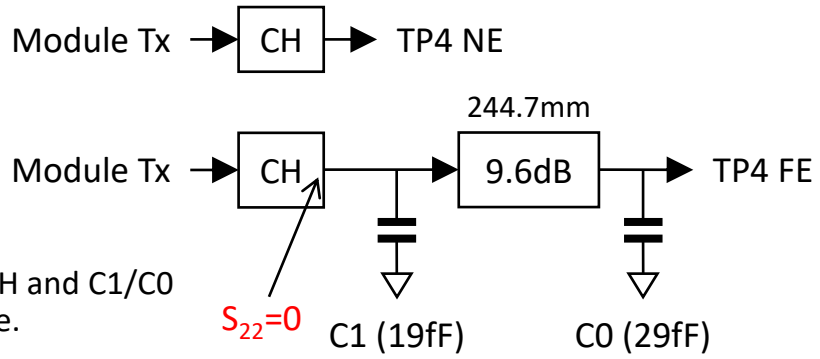
Objective

- Module output spec at TP4 in D1.2 has several TBDs.
- This work is to obtain reasonable values for some of those TBDs.
- This is an update of hidaka_3ck_adhoc_01_061020.
  - Removed reflection between channel and host trace for far-end eye according to a feedback at the ad hoc meeting.

Channel Set

ID	Channel Description	IL (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	ILD (dB)
1	lim_3ck_03_0719_m2c Channel1a_TP4	5.0766	11.6805	13.0886	3.0476	0.11369
2	lim_3ck_03_0719_m2c Channel2a_TP4	5.3441	12.3813	13.3755	2.5090	0.13794
3	Yamaichi QSFP top normal	5.5565	15.0307	14.977	4.5338	0.034735
4	Yamaichi QSFP bottom normal	5.5589	15.3961	14.9139	4.6743	0.043043
5	Yamaichi QSFP top worst	5.7402	12.4466	12.8948	4.2753	0.062142
6	Yamaichi QSFP bottom worst	5.8852	12.9025	12.6977	4.4045	0.073612

- Channel 1 and 2 are taken from IEEE P802.3ck channel data web page.
- Channel 3 thru 6 are constructed from Yamaichi QSFP data contributed by Mr Hiroaki Kukita.
  - This QSFP data includes NEXT channel from TP1 to TP4 for TP4 simulation.
  - QSFP was cascaded with module PCB (ito_3ck_01_1118_PCBtrace/Module_Board.s4p) on the module side, and synthesized MCB (with reference IL of MCB defined as EQ 162B-2 and its minimum phase plus same propagation delay as 58.63mm PCB that has 2.3dB loss at 26.5625GHz) on the host side.
- Port 1 : module side (Tx), Port 2 : host side (Rx)
- For TP4 NE (Near End), port 2 is directly measured.
- For TP4 FE (Far End), port 2 is attached with C1 (19fF) + 9.6dB PCB (244.7mm) + C0 (29fF) before measurement.
  - S22 of CH is forced to zero to remove reflection between CH and C1/C0 in order to replicate real measurement at TP4 using a scope.



Simulation Conditions

- 42 test cases for each of TP4 Near End and TP4 Far End
  - 6 C2M channels
  - 7 cases of Tx PKG zp ([2 3 4 5 6 7 8] mm)
    - No Rx PKG
- TX FIR settings
  - Two TX FIR settings : Optimized for each of TP4 Near End or TP4 Far End
  - One TX FIR setting : Optimized for TP4 Far End
- COM parameters (full list in back up)
  - COM tool version 2.93

Parameter	Value	Parameter	Value	Parameter	Value
Tx C_d	85 fF	min c(0)	0.6	f_r	0.75 * fb
Tx L_s	120 pH	c(-1)	[-0.3:0.02:0]	T_r	6.160714 ps
Tx C_b	30 fF	c(-2)	[0:0.02:0.1]	DER_0	1E-5
Tx C_p	75 fF	c(-3)	[0]	sigma_RJ	0.01 UI
Tx R_d	45 ohm	c(1)	[-0.1:0.05:0]	A_DD	0.02 UI
A_v	0.391 V	g_DC	[-14:1:-3]	eta_0	4.1E-8V^2/GHz
A_fe	0.391 V	g_DC_HP	[-3:0.5:0]	SNR_TX	33 dB
A_ne	0.417 V	f_z	12.58 GHz	R_LM	0.95
N_b	4	f_p1	20 GHz		
b_max(1)	0.4	f_p2	28 GHz		
b_max(2..4)	0.15	f_HP_PZ	fb / 40		

VEC results

- For Near End, all simulated cases barely passed VEC ≤ 7.0 dB.
- For Far End, all simulated cases barely passed VEC ≤ 6.5 dB.

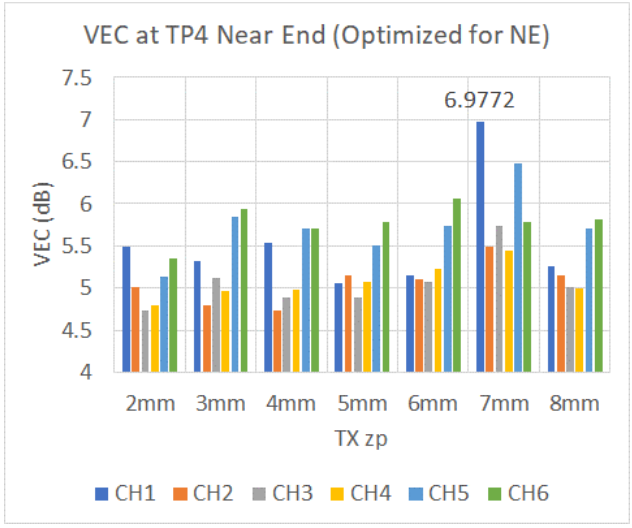
- Including margin, we recommend the following specifications:

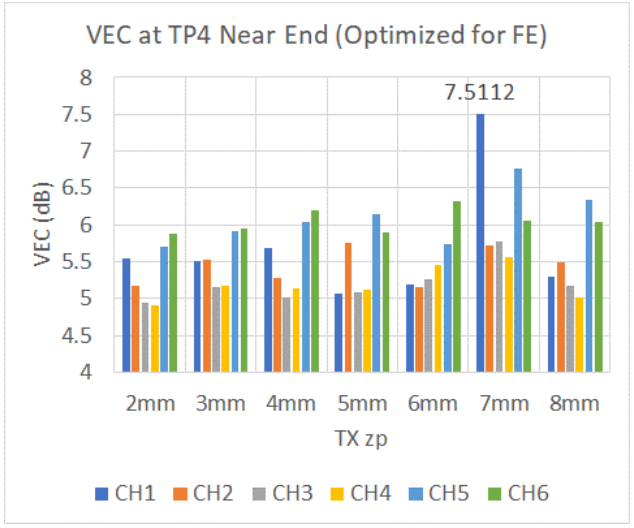
With two TX FIR settings for each of Near End and Far End

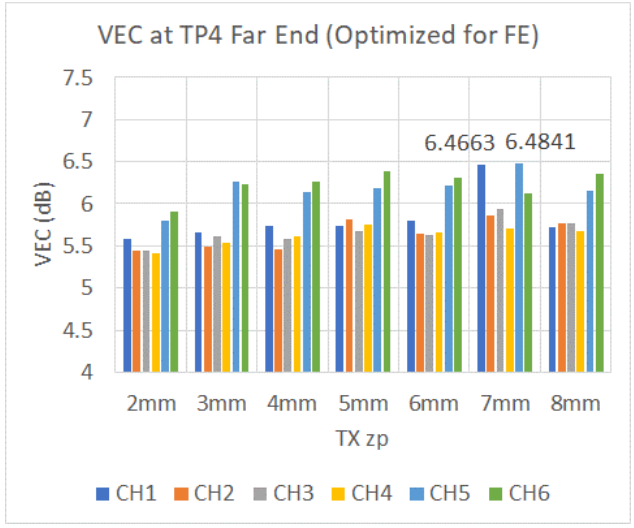
VEC at TP4 Near End	≤ 7.5 dB
VEC at TP4 Far End	≤ 7.0 dB

With one TX FIR setting

VEC at TP4 Near End	≤ 8.0 dB
VEC at TP4 Far End	≤ 7.0 dB







EH results

- For Near End, all simulated cases barely passed EH ≥ 52.5 mV.
- For Far End, all simulated cases barely passed EH ≥ 25.0 mV.

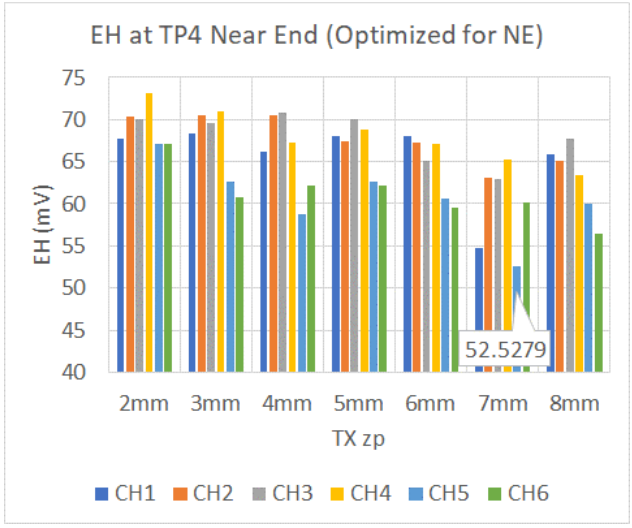
- Including margin, we recommend the following specifications:

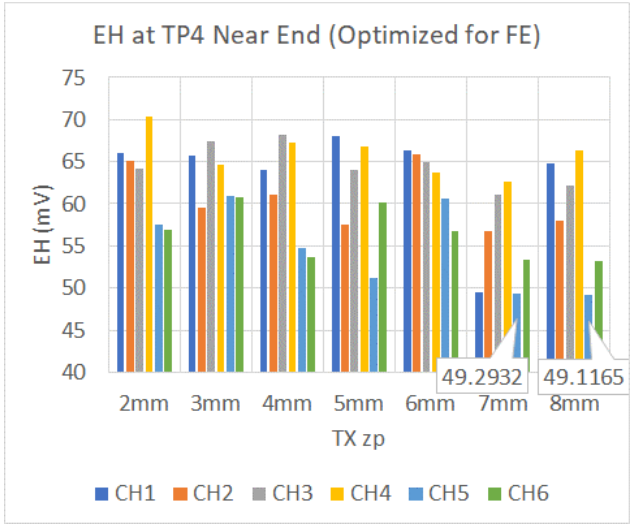
With two TX FIR settings for each of Near End and Far End

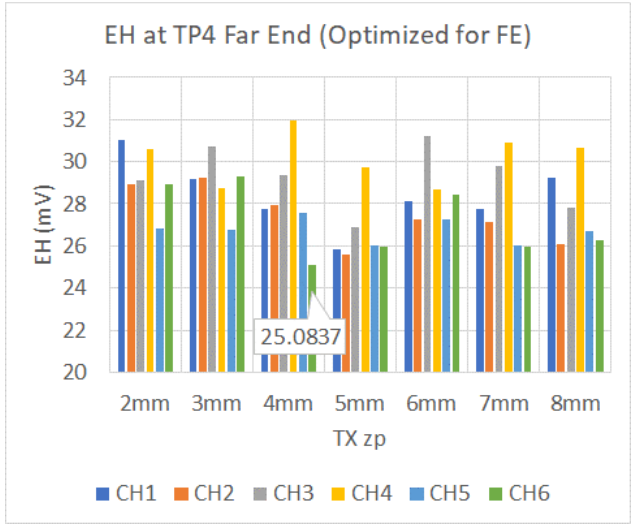
EH at TP4 Near End	≥ 50.0 mV (or 24.0mV to restrict max swing)
EH at TP4 Far End	≥ 24.0 mV

With one TX FIR setting

VEC at TP4 Near End	≥ 45.0 mV
VEC at TP4 Far End	≥ 24.0 mV



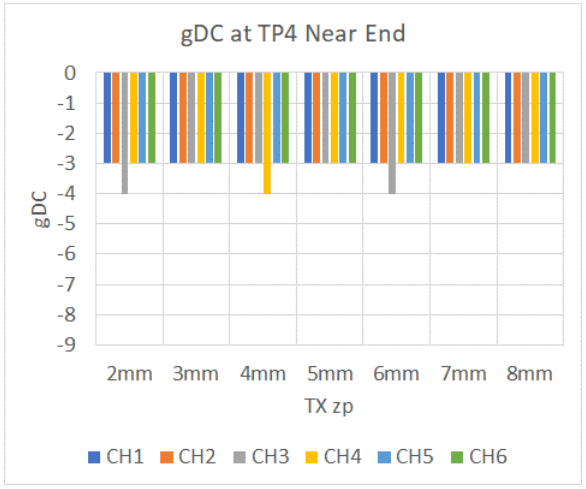


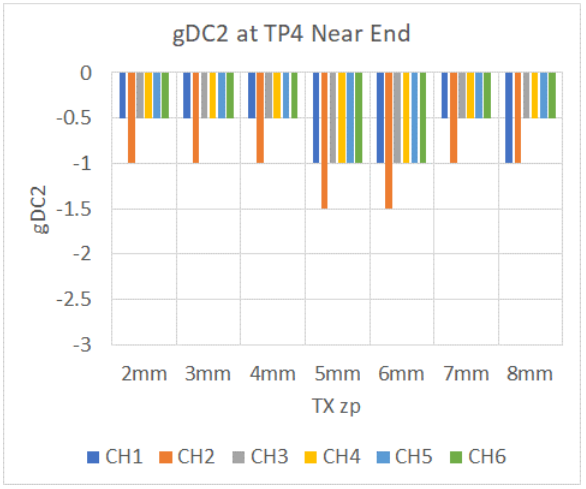


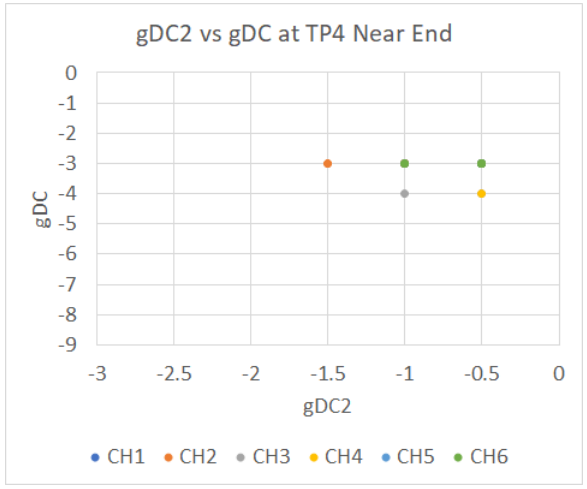
CTLE results

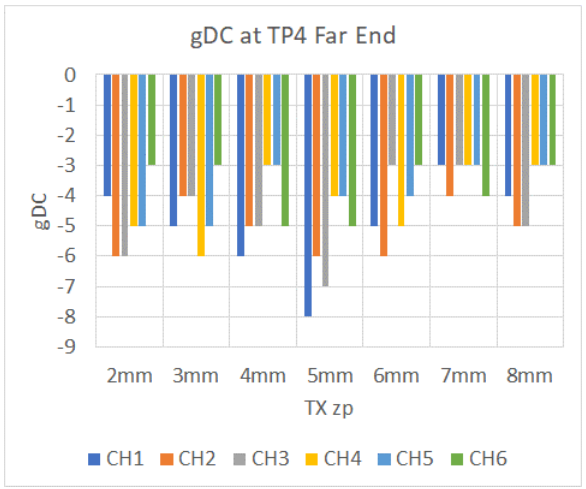
- We recommend the following specifications:

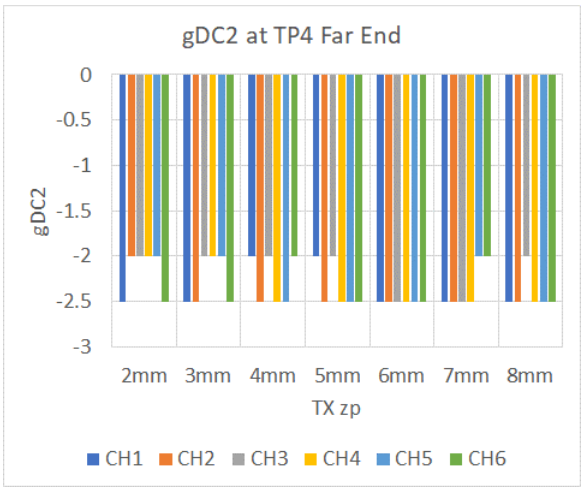
gDC at TP4 Near End	∈ [-5.0:1.0:-3.0]	gDC2 at TP4 Near End	∈ [-2.0:0.5:0.0]
gDC at TP4 Far End	∈ [-9.0:1.0:-3.0]	gDC2 at TP4 Far End	∈ [-3.0:0.5:-1.5]

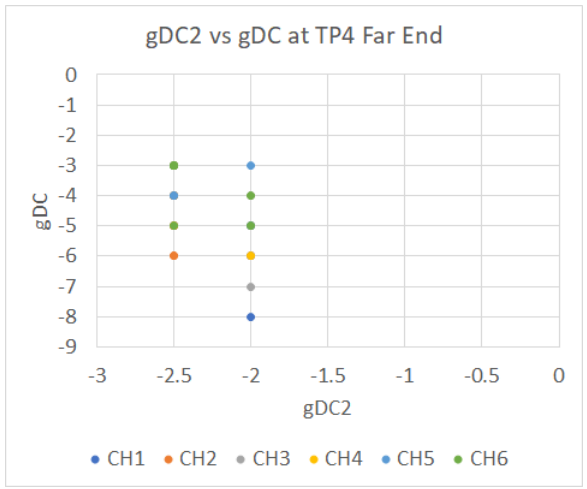








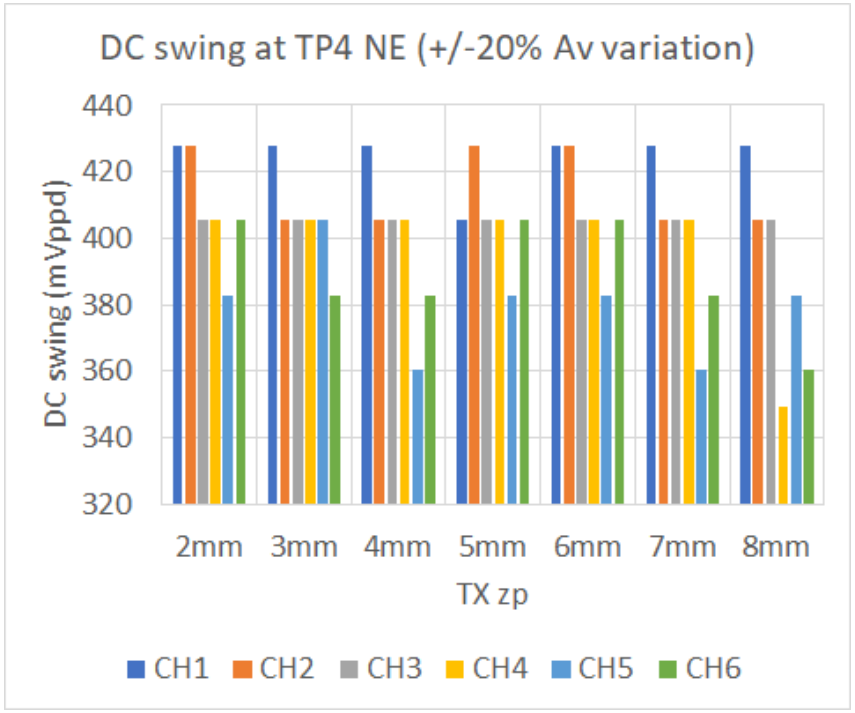


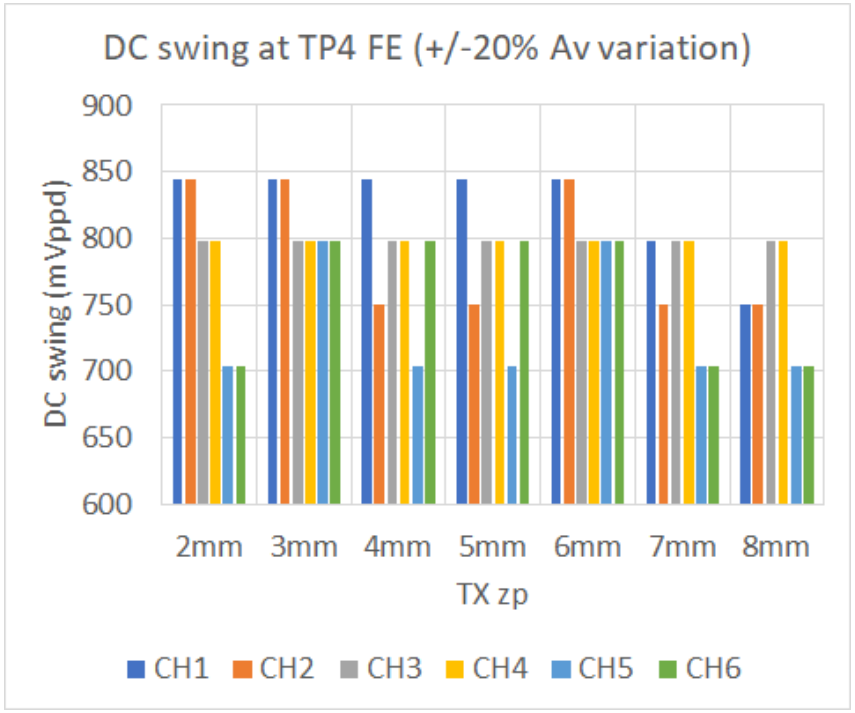


Max DC Swing (assuming ±20% variation of Av)

- Conditions to estimate Max DC Swing
  - Assume the traditional ±20% variation of TX output amplitude
  - Ignore the effects of variation of TX termination resistor and noise
  - TP4 Far End : Av = 0.391V * 1.2/0.8
  - TP4 Near End : Av = 0.391V * 1.2/0.8 * 24/50 (assuming 24mV EH spec at Near End)

- We recommend the following specifications for two module TX FIR settings:
  Swing at TP4 Near End < 500mVppd Swing at TP4 Far End < 900mVppd

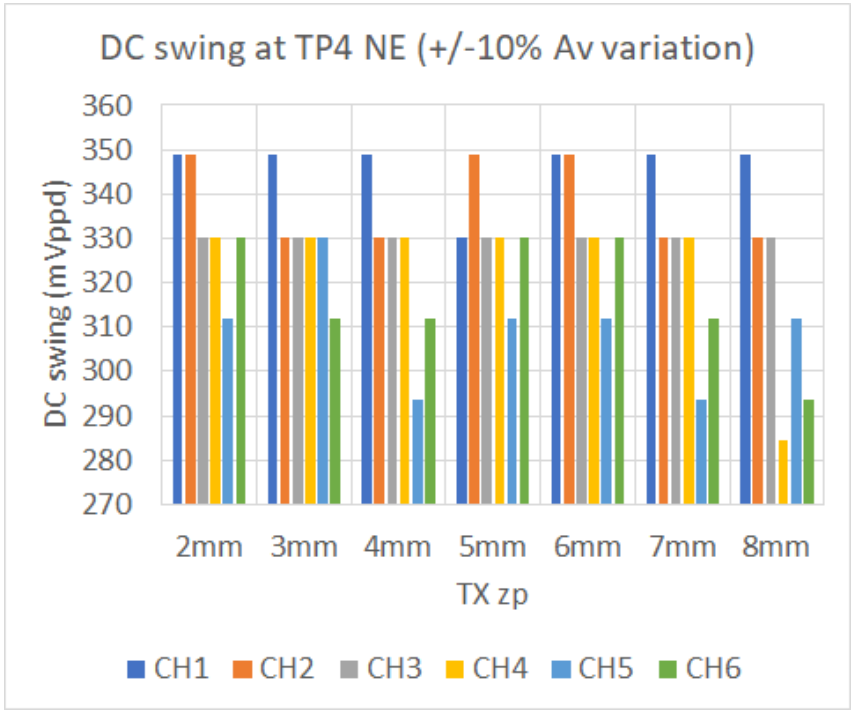


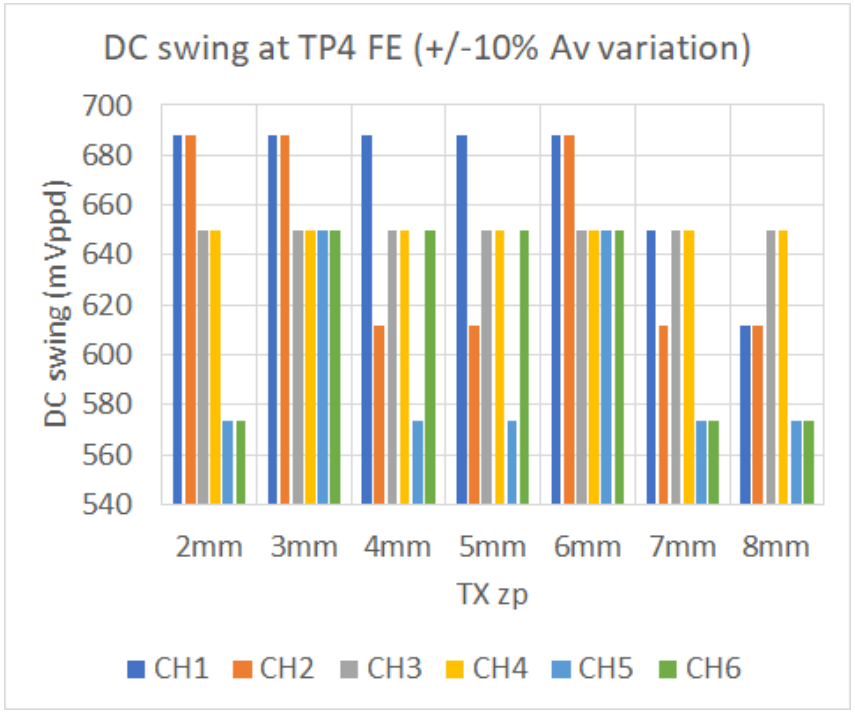


Max DC Swing (assuming ±10% variation of Av)

- Conditions to estimate Max DC Swing
  - Assume a tightened ±10% variation of TX output amplitude
  - Ignore the effects of variation of TX termination resistor and noise
  - TP4 Far End : Av = 0.391V * 1.1/0.9
  - TP4 Near End : Av = 0.391V * 1.1/0.9 * 24/50 (assuming 24mV EH spec at Near End)

- We recommend the following specifications for two module TX FIR settings:
  Swing at TP4 Near End < 400mVppd Swing at TP4 Far End < 750mVppd





Summary

- We recommend the following specifications at TP4:

		TP4 Near End			TP4 Far End
Option		Option A	Option B	Option C	
Module TX FIR		Two settings		One setting	
Near End Swing		Smaller than FE	Same as FE	Same as FE	
Near End EH		Same as FE	Larger than FE	Larger than FE	
VEC		≤ 7.5 dB	≤ 7.5 dB	≤ 8.0 dB	≤ 7.0 dB
EH		≥ 24.0 mV	≥ 50.0 mV	≥ 45.0 mV	≥ 24.0 mV
Swing	±20% Av	≤ 500mVppd	≤ 900mVppd	≤ 900mVppd	≤ 900mVppd
	±10% Av	≤ 400mVppd	≤ 750mVppd	≤ 750mVppd	≤ 750mVppd
gDC		min -5.0 dB max -3.0 dB step 1.0 dB			min -9.0 dB max -3.0 dB step 1.0 dB
gDC2		min -2.0 dB max 0.0 dB step 0.5 dB			min -3.0 dB max -1.5 dB step 0.5 dB

- TP4 Far End Swing ≤ 600mVppd leaves 0% room for tolerance of Av

Backup Slides

TP4 COM Spread Sheet

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.85e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[2 6; 0 0]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[2 6; 0 0]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.75e-4 0.0e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.391	V	
A_fe	0.391	V	
A_ne	0.417	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(-3)	[-0.00:0.02: 0]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.4		
b_max(2..N_b)	0.15		
b_min(1)	**-0.4**		
b_min(2..N_b)	**-0.15**		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:0.5:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	

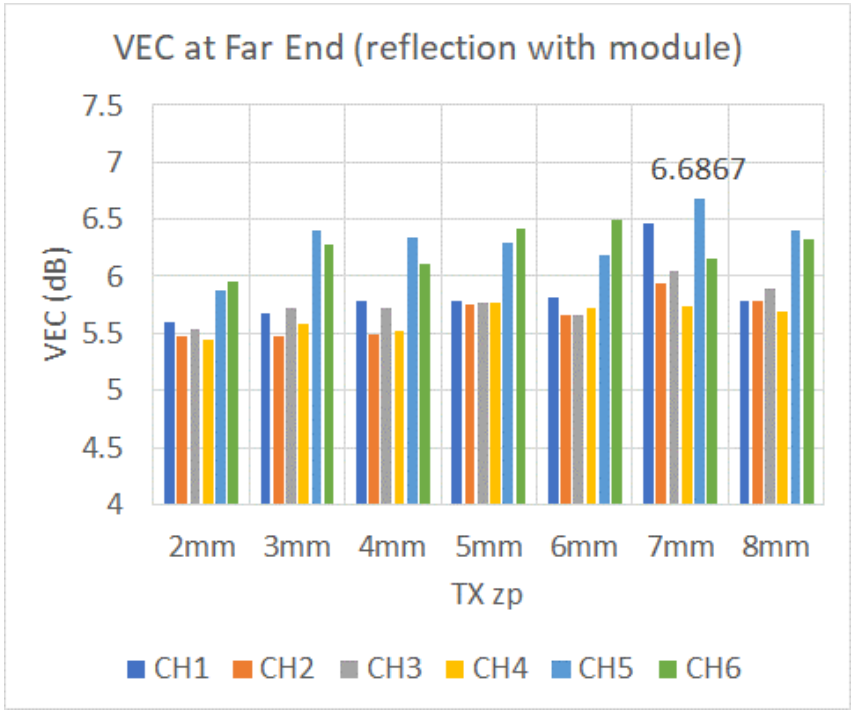
I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	**10.5**	dB
DER_0	1.00E-05	
T_r	**0.006160714**	ns
FORCE_TR	1	logical
Local Search	**0**	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	**0.01**	ns
N	400	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	**4**	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

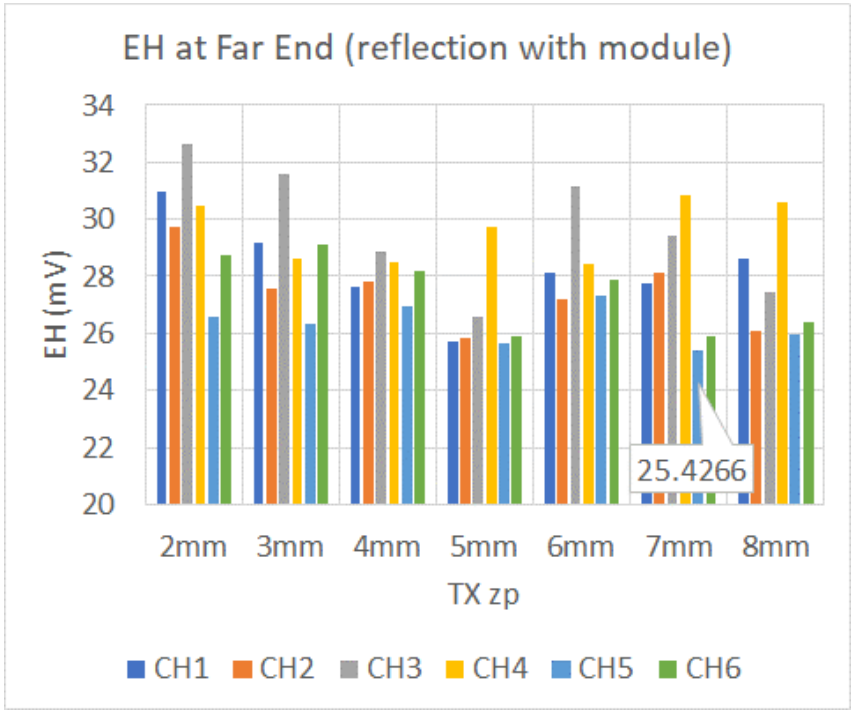
Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	**[0 0.0009909 0.0002772]**	
package_tl_tau	**6.141E-03**	**ns/mm**
package_Z_c	**[87.5 87.5 ; 92.5 92.5]**	**Ohm**
benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	0	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.844	GHz
A_ft	0.600	V
A_nt	**0.600**	V

TBD in document	**under consideration**
new	

VEC/EH with reflection between CH and C0/C1

- This is the simulation result by simply concatenating S-parameters of channel and C1+PCB+C0.
  - It includes the reflection noise between channel and C1+PCB+C0, which does not exist in real TP4 measurement.
  - This is the result presented in hidaka_3ck_adhoc_01_061020 at the ad hoc meeting.
- There is small effect of reflection between CH and C1+PCB+C0.

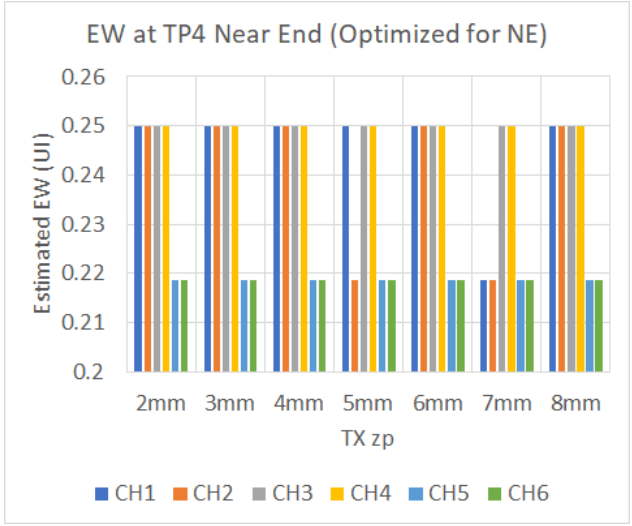


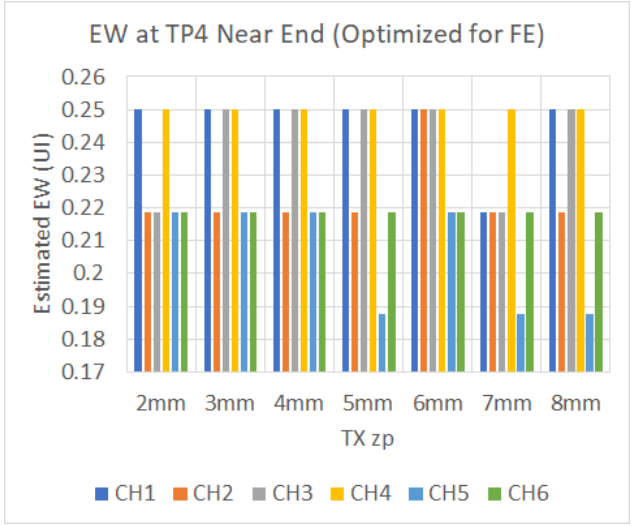


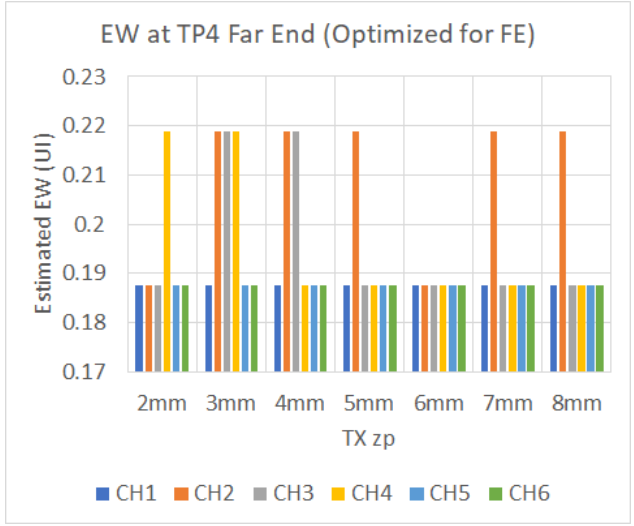
EW results

- This may be inaccurate, because the algorithm in the COM tool is not compliant to 120E.4.2.
- Resolution is limited to 1/32 UI.

- Full waveform simulation or measurement is required to get a reasonable spec value.

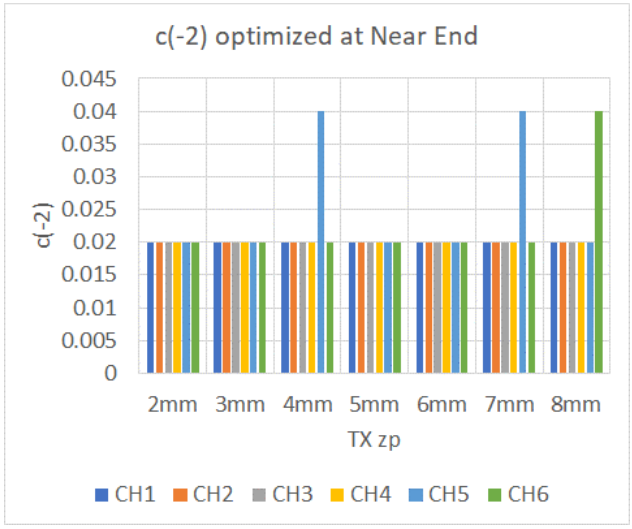


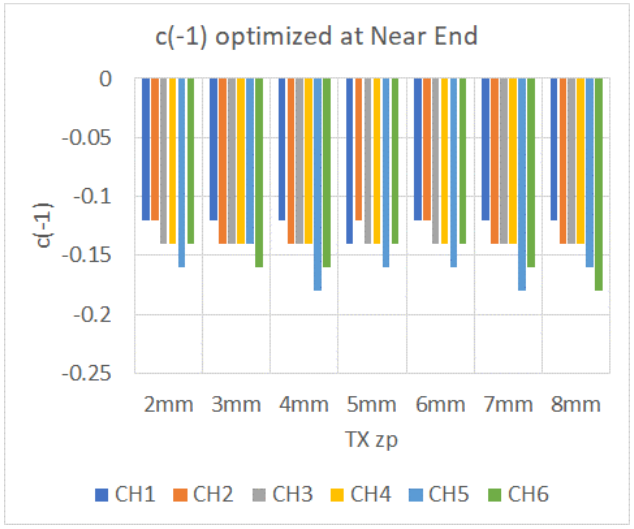


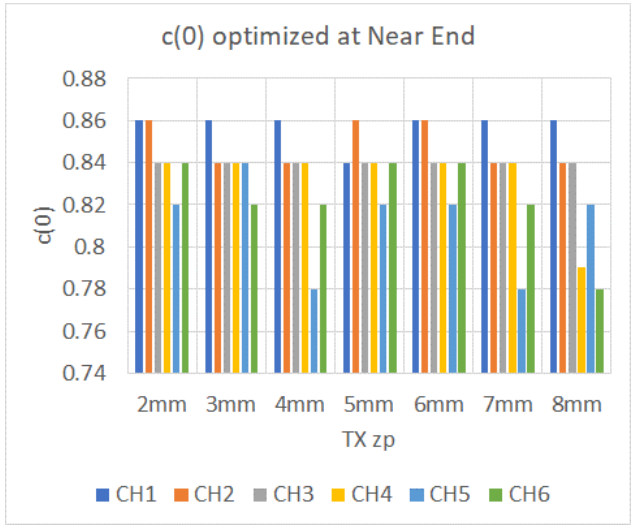


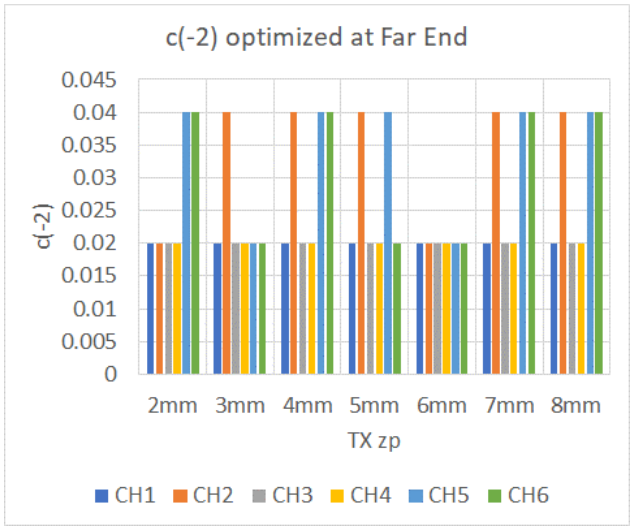
TX FIR Tap Weights

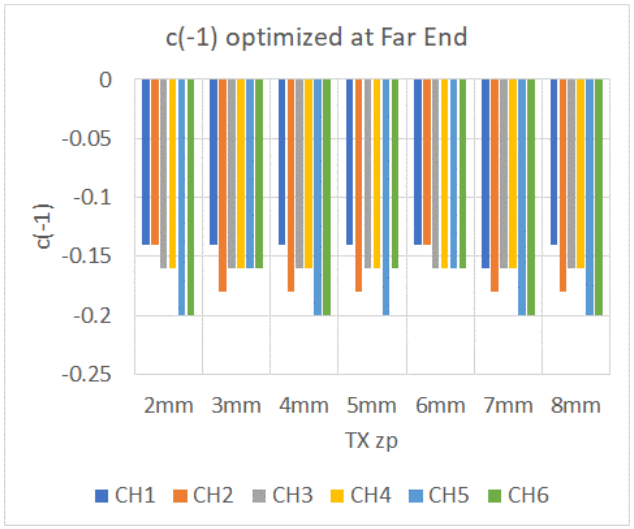
- c(+1) = 0.0 in all cases except CH4, zp=8mm, optimized for Near End where C(+1) = –0.05

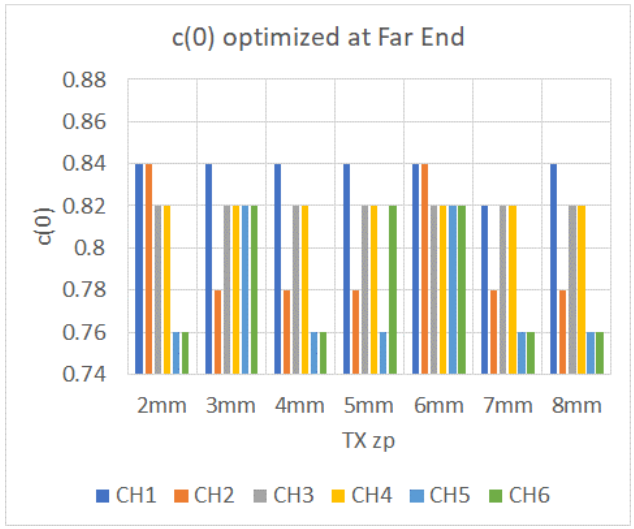






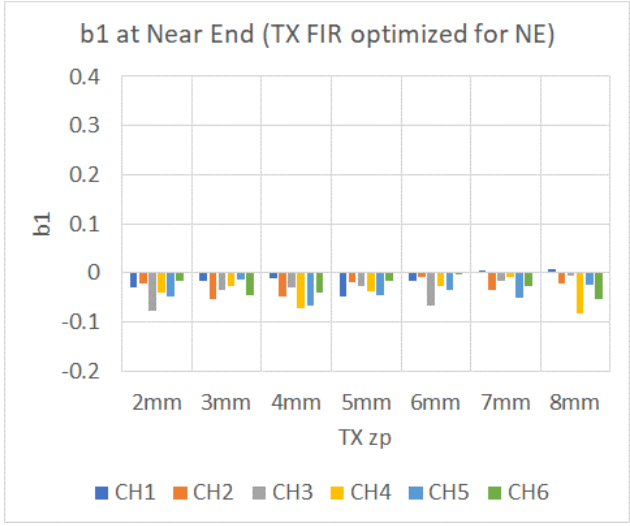


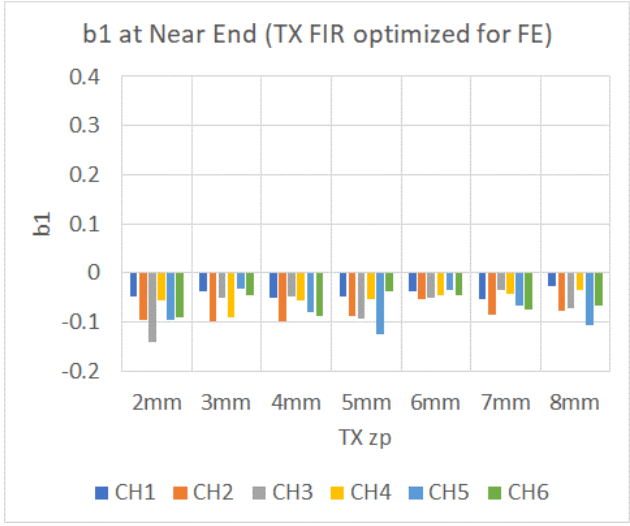


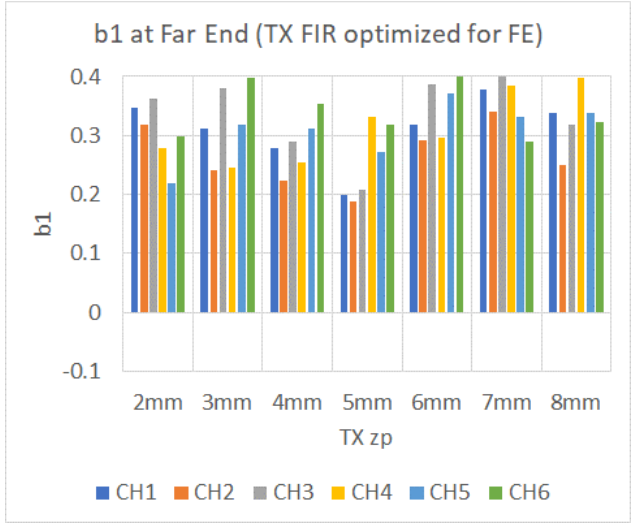


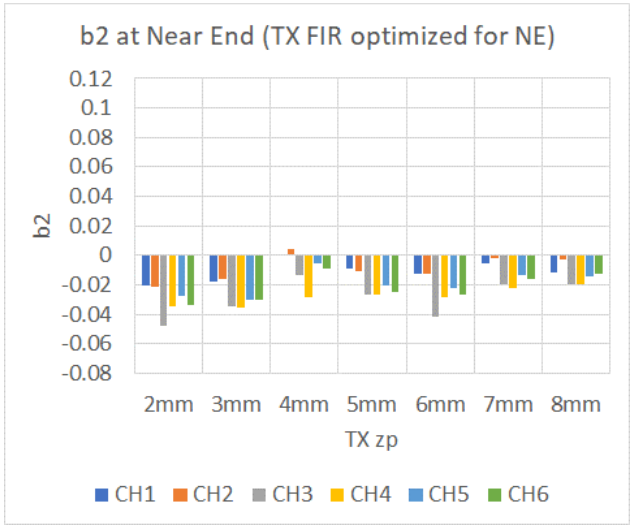
DFE Tap weights b1, b2

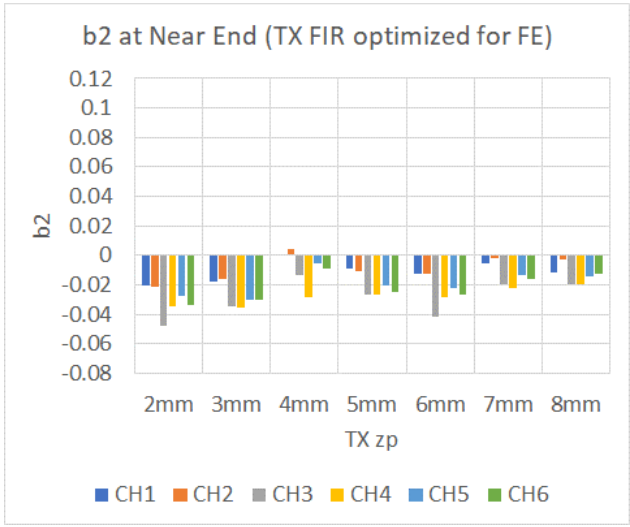
- TX FIR optimized for FE is overequalized at NE

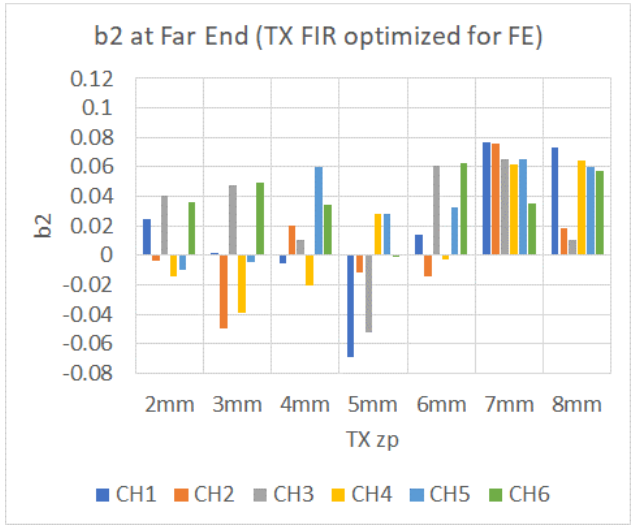












DFE Tap weights b3, b4

- TX FIR optimized for FE is overequalized at NE