Concerns with stressed input tests in Annex 120G 8023ck_D1p3 V2

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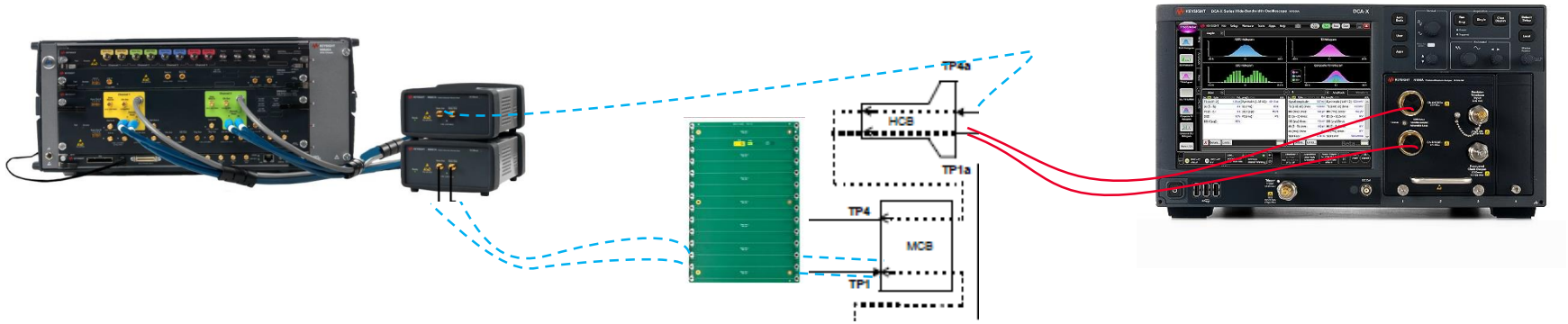
KEYSIGHT TECHNOLOGIES

IEEE 802.3ck Receiver Input Test

FIRST RESULTS

- In Concerns with Stressed Input Tests in Annex 120G we reported experimental results of stressed input test calibration procedure not meeting Draft 1.3 targets. Potential explanations were mentioned by the WG during the discussion
  - Impact of sinusoidal Jitter (50mUI @ 40MHz) on VEC not taken into account in the simulations
  - Use of non-optimal equalizer settings (over de-emphasis)
  - Not compliant test channels?



- In this presentation we report
  - performance with different channels simulated on the sampling scope
  - Impact of SJ on mated HCB-MCB (experimental)

Reference setup – stressed input test

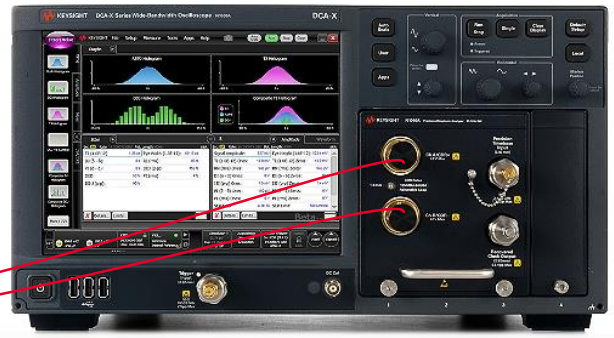
REFERENCE SETUP FOR SIMULATION

M8045A PG

2 or **3 pre-cursors**, 1 post-cursor
53.125Gbaud PAM4 (max 1.8V diff pp)
Inject SJ, RJ

Cable de-embeded in scope
Skew corrected in scope

N1000A+N1060A



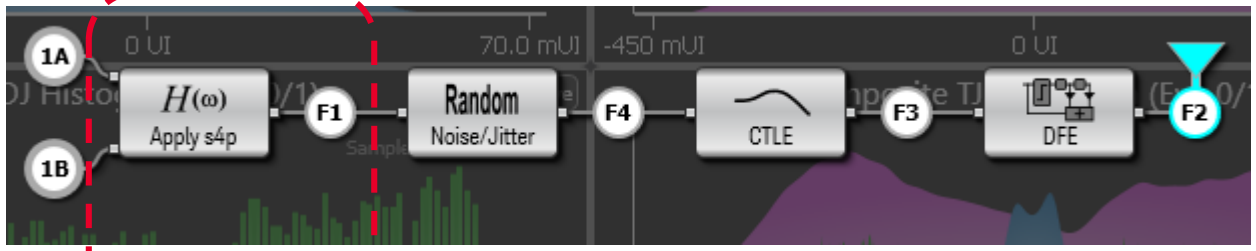
Tx de-emphasis and CTLE settings from COM

No aggressor lanes

Internal CDR **OR** clean clock
40GHZ Butterworth filter

Expected differences with real channel measurement

- Full control of skew
- Perfect 50Ohm matching between BERT & SCOPE



channel
(Simulated .s4p)

Rx **referred noise**

CTLE

4-Tap **DFE**
(optimized)

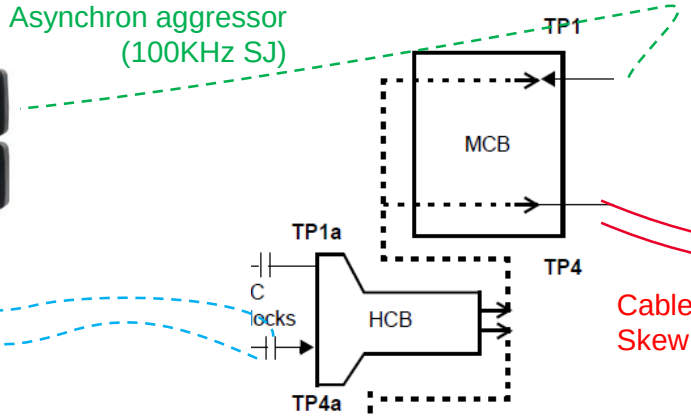
Experimental setup – stressed input test

HOST INPUT NEAR-END TEST

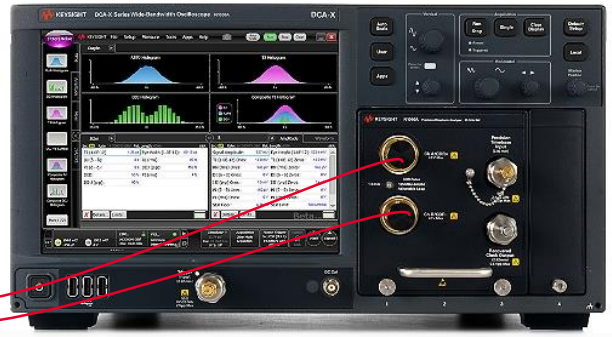
M8045A PG

2 or **3 pre-cursors**, 1 post-cursor
53.125Gbaud PAM4 (max 1.8V diff pp)
Inject SJ, RJ

Mated MCB-HCB (vendor **B**)



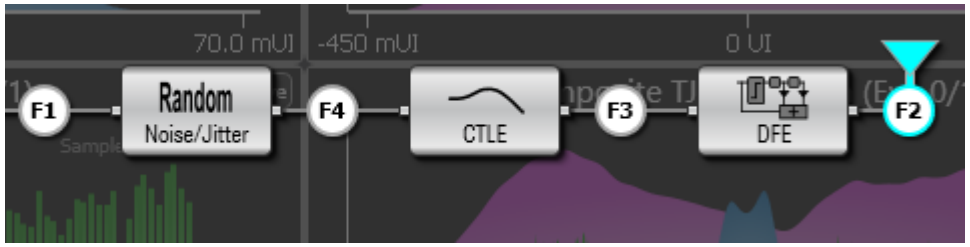
N1000A+N1060A



Cable de-embeded in scope
Skew corrected in scope

CTLE autotune **Internal** CDR
40GHZ Butterworth filter

Tx de-emphasis and CTLE settings from COM



Rx **referred noise** **CTLE** 4-Tap **DFE** (optimized)

Impact of SJ

WITH SIMULATED CHANNELS

	S4p @ 26.56 GHz	Perfromance with and *without* 50mUI SJ @ 40MHz					
	SD21/SD11 [dB]	**VEC dB**	*VEC dB*	**EW [mUI]**	*EW [mUI]*	**EH [mV]**	*EH [mV]*
Cisco M8049A	-18/-19	**8.81**	*7.2*	**168**	*212*	**20.4**	*24.7*
ML+ M8049A	-18.6/-20	**12.4**	*9.2*	**114**	*162*	**11.2**	*16.4*
ML	-8/-17.5	**8.3**	*6.9*	**194**	*238*	**29.6**	*35*
Lim[1]	-14/-10	**6.7**	*5*	**218**	*260*	**31**	*38*
Tracy[2]	-15/-16.5	**7.9**	*6.5*	**194**	*244*	**27**	*32*
Kocsis[3]	-8/-8	**9.7**	*7.6*	**168**	*212*	**49**	*62*

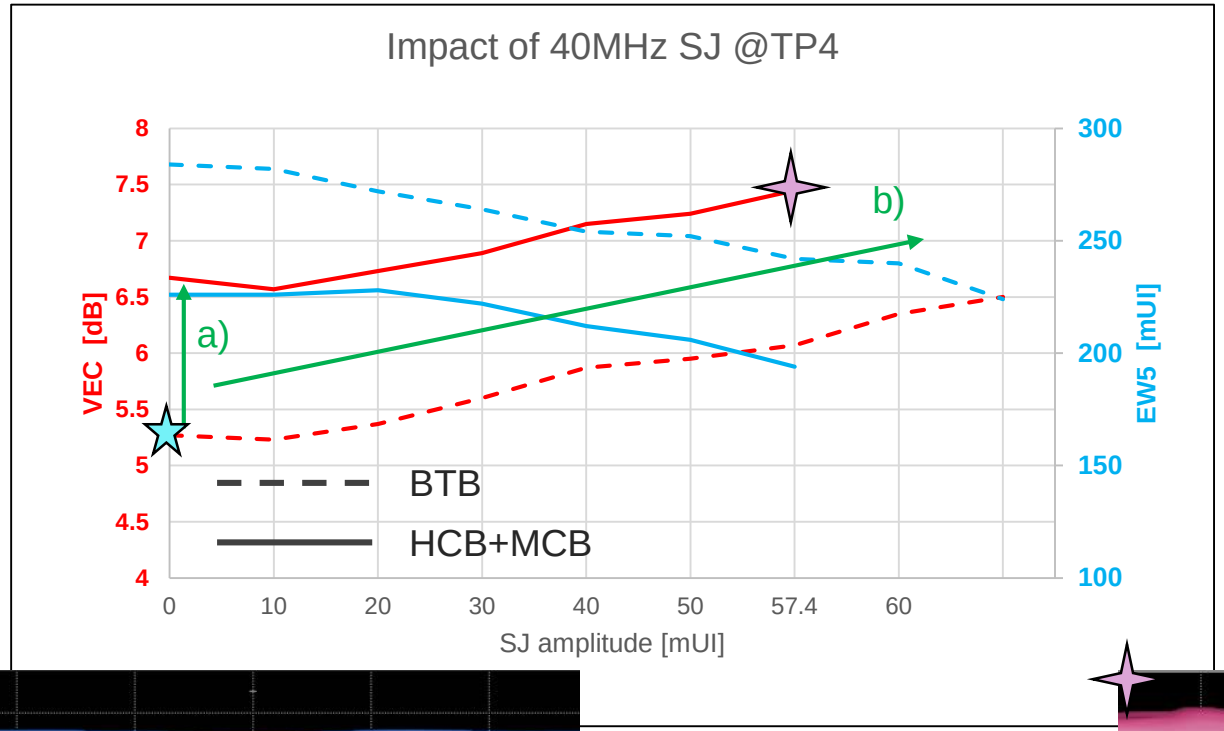
Observation

- >1dB VEC penalty for near-end (<10dB
- > 1.5dB VEC penalty far-end (>15dB)

Channels **considered in previous presentation present worse performance than reference channels discussed in [1,2]**

Impact of SJ

MATED MCB-HCB - EXPERIMENTAL



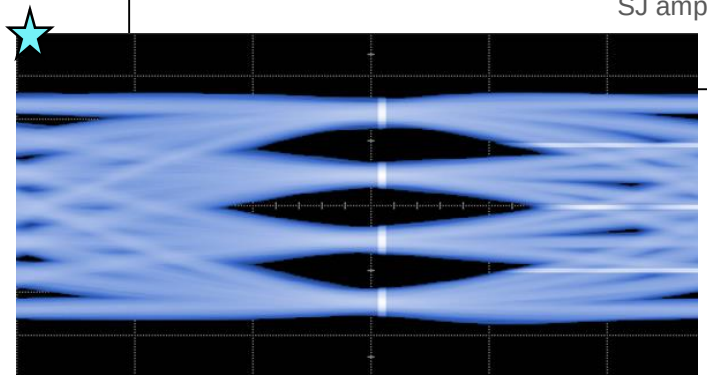
Observation

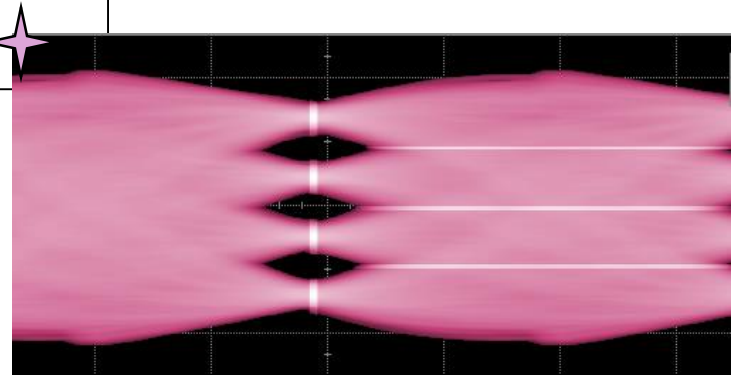
a) ~1dB VEC penalty for MCB-HCB vs BTB

- ✓ Can be reduced to xxx by using 9-taps FFE instead of DFE
  - Limited impact of x-talk (~0.2dB)
  - Limited de-emphasis accuracy (?)

b) 50mUI SJ → ~1dB VEC penalty

- SJ affects EW, EH and VEC
- Jitter-to-amplitude conversion





Discussion/Recomendations

STRESSED INPUT TEST – RESULTS OVERVIEW

I. Discussion

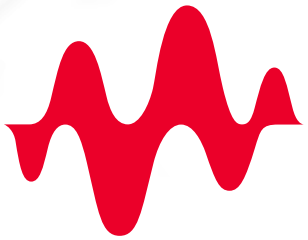
- It is no realistic that any compliant Tx with 50mUI SJ @ 40MHz can achieve
  - 7.5dB VEC @ TP1a (~xxdB IL channel)
  - 9.5dB VEC @ TP4 (~xxdB IL channel)
  - See also https://www.ieee802.org/3/ck/public/20_10/healey_3ck_01a_1020.pdf

II. Recommendations

A) Reduce the jitter tolerance test from 50mUI to TBD (20mUI)

B) Increase VEC limit for stress input

- 7.5→ 9 dB for host input test
- 9.5→ 11dB for module input test



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Tx Characterization

@TP0V WITH 50MUI SJ @ 40MHZ

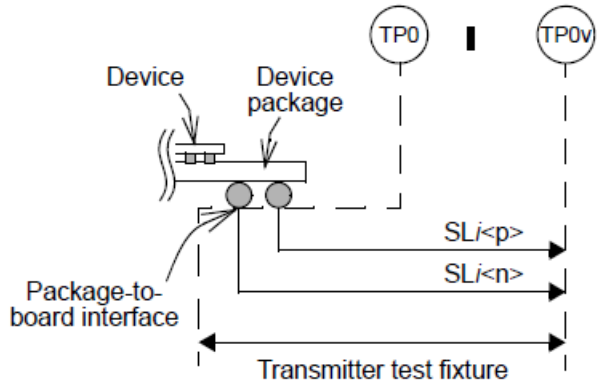


Figure 163–3—Transmitter test fixture and test points

TP0 to **TP0v** replica trace embedded in the scope for Tx measurement

Table 23-13. Host-to-Module Electrical Recommendations at TP0a

Parameter	Symbol	Min.	Max.	Unit	Conditions
Baud Rate		36.0	58.0	Gsym/s	
Differential Voltage, pk-pk	T_Vdiff	750	-	mV	See Note 1
DC Common Mode Voltage	T_Vcm	-0.3	2.8	V	See Note 2
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-	Equation 17-4	dB	at TP0
Transition Time: 20% to 80%	T_tr, T_tf	6.5	-	ps	With emphasis off
Common-mode return loss	T_SCC22	$-6 + 3*f/f_b$	-	dB	
Common Mode Noise, RMS	T_Ncm	-	12	mV	
Uncorrelated Jitter RMS (standard deviation of the probability distribution)	T_J_{RMS}		0.023	UI_{RMS}	See Note 3
Uncorrelated Jitter (time interval from 0.005% to 99.995% of the probability distribution)	T_J_{4u}		0.118	UI	See Note 3
Even-Odd Jitter (EOJ)	T_EOJ		0.019	UI	
		32.5	-	dB	See Section 17.3.1.6.4 for definition

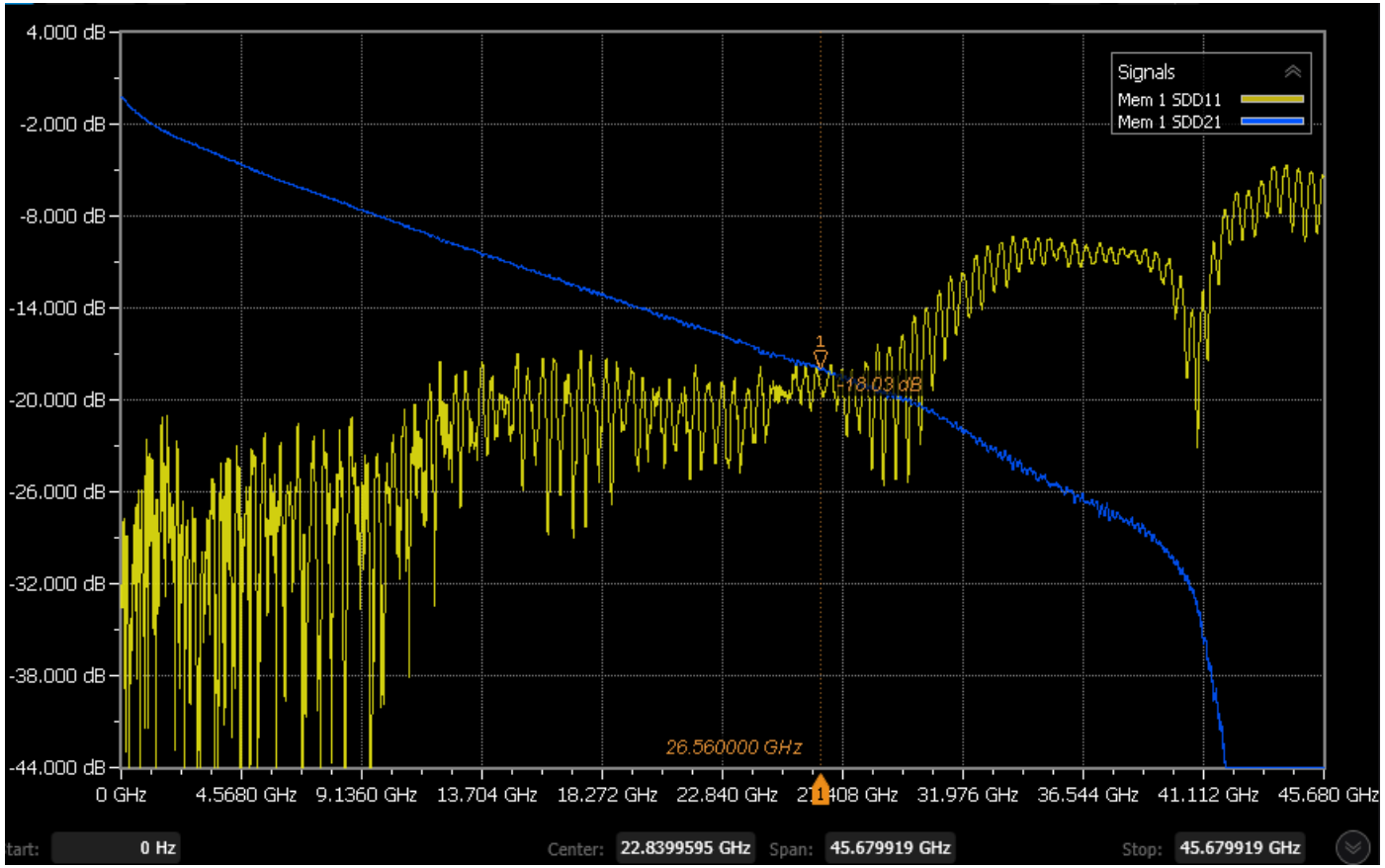
P1a. Minimum voltage can be lower for low loss

or floating load.
M4 Section 17.3.1.7

Parameters	Reference to Table 23-13	comments
Transition time	within spec	
J4u	within spec	include 50mUI sinusoidal jitter @40MHZ
Jrms	within spec	
R_{LM}	within Spec	
SNDR	> 31dB	

Channel Characterization

CISCO M8049A



COM Output (ver 2.93):

- FOM_ILD: 0.1816
- COM: 3.736 dB
- ERL22(dB): 13.2508
- ERL11(dB): 13.2508

Channel Characterization

M L

COM Output (ver 2.93):

- FOM_ILD: 0.1816
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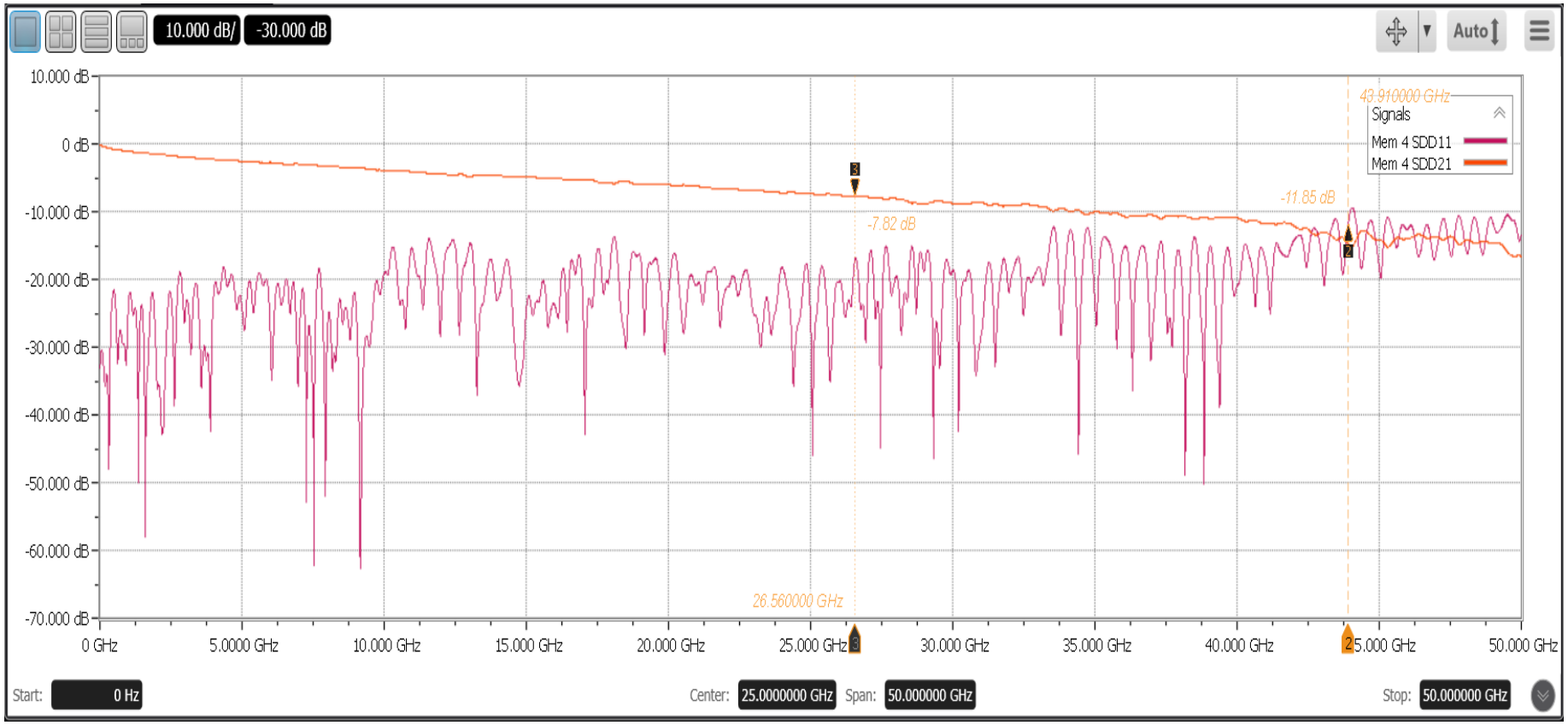
Channel Characterization

HOST INPUT NEAR-END TEST



COM Output (ver 2.93):

- FOM_ILD: 0.0742
- COM(dB): 6.0293
- ERL22(dB): 13.5598
- ERL11(dB): 12.5234