Eye specification in PAM4 C2M

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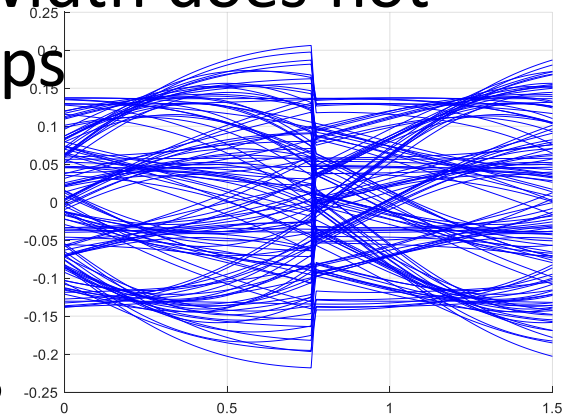
Introduction

- Baselines sun_3ck_04b_0319 and sun_3ck_01b_1119 contain entries for eye width, eye height and vertical eye closure (VEC)
- Eye width is controlled by eye symmetry mask width (ESMW)
  - Limits of 0.22, 0.265 and 0.2 UI were proposed but not adopted
- Use of eye width and ESMW specs is documented in OIF CEI and 120E
  - Not fully presented in the draft, although in baselines

Basics

- C2M eye limits are intended to protect the C2M input from bad signals
- For PAM4, eye width and ESMW method works with a DFE reference receiver just as without
  - The figure shows why: PAM4 eye width does not depend on exact timing of DFE steps



- **A signal is not a channel**
- Look to optical specs for examples of signal specifications
  - Note that optical receivers add significant noise, so optical specs focus on vertical opening not jitter

Objectives of eye specs

Objectives

- Provide input with a signal that it can make right decisions on
  - Adequate vertical eye opening (absolute and relative) across a reasonable time window
    - Avoid needing super-fast circuits or CDRs as good as test equipment
- Provide input with a signal that it can recover a decent clock from
  - Not too much jitter = not too little eye width

Non-objectives

- Educating the reader
- Distinguishing between channel-induced impairments and driver-induced impairments
- Diagnosing, measuring or de-embedding to the driver silicon

History lesson

- C2M VEC and ESMW amount to an eye mask

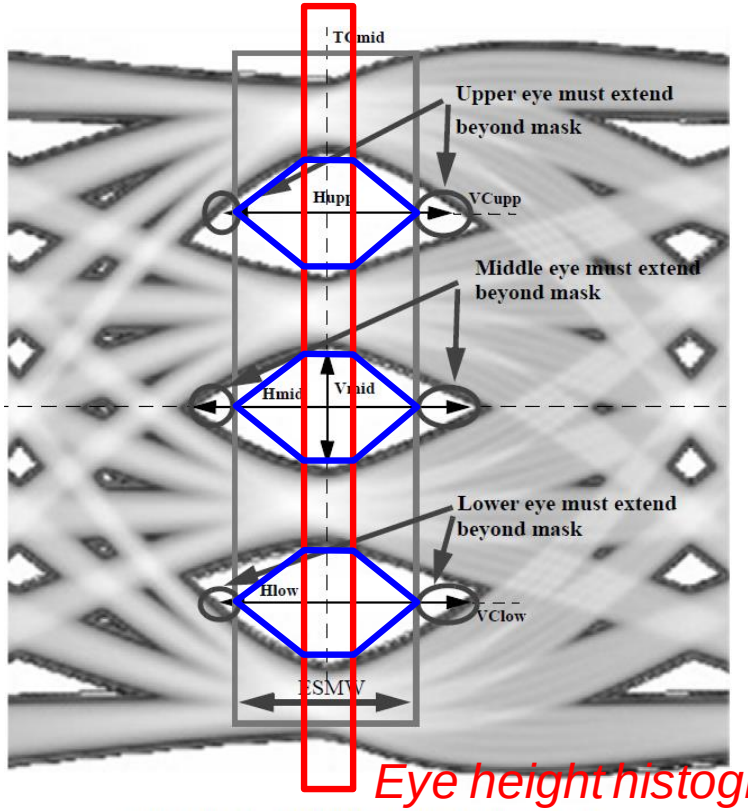


Figure 120E–14—PAM4 upper, middle, and lower eye mask

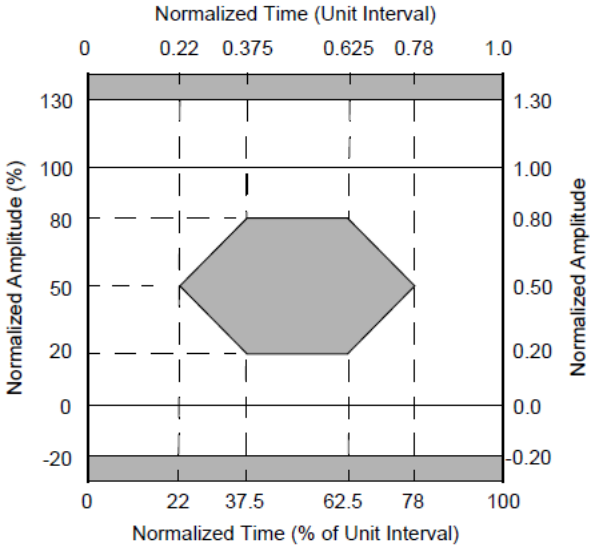


Figure 38–2—Transmitter eye mask definition

Eye height histogram 0.05 UI wide is unusually narrow

- Need something like this to leave room for receiver jitter

Gigabit Ethernet eye mask

- At TP2: good region could be narrower at the receiver
- 6 sided mask
- ESMW 0.78 – 0.22 = 0.56 UI
  - Protects CR part of CDR
- Good region in middle of eye = 0.25 UI wide
  - Protects DR part of CDR

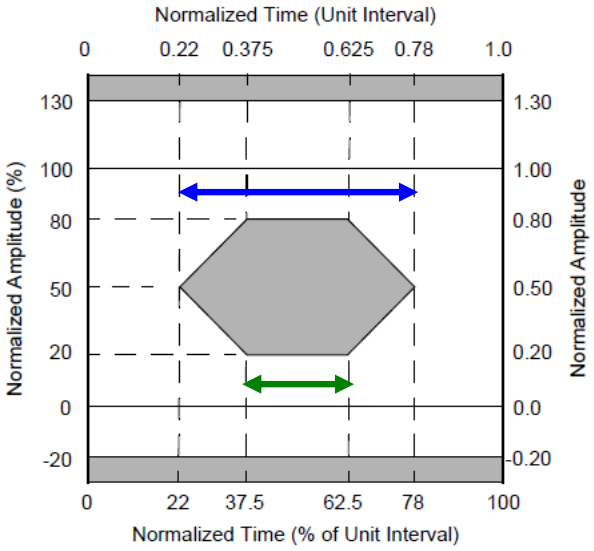


Figure 38–2—Transmitter eye mask definition

10 Gigabit Ethernet eye mask and TDP

- Eye mask at TP2
- 10 sided mask
- ESMW 1 – 2*0.235 = 0.53 UI
  - Protects CR part of CDR
- Good region in middle of eye is
  1 – 2*0.45 = 0.1 UI wide
  - Protects DR part of CDR
- Transition region within 1 – 2*0.395 = 0.21 UI wide
  - Protects receiver from a combination
  - Mask edges are more parallel to actual waveforms where they may encroach, so more definite pass/fail signal in reasonable measurement time
- TDP defined at TP3 (after channel)
- Worse of +/- 0.05 UI, so 0.1 UI wide

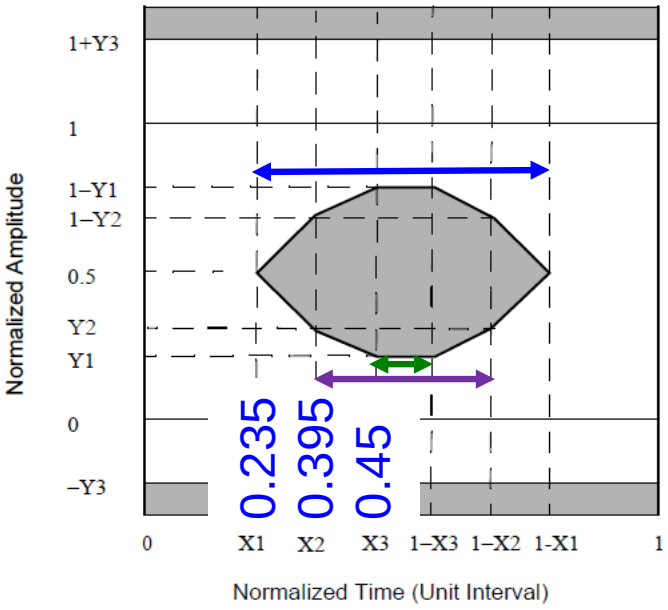


Figure 52–8—Transmitter eye mask definition

25 Gigabit Ethernet TDEC

- Two histogram windows, centres 0.2 UI apart, each 0.04 UI wide
- Total 0.24 UI wide

- As the signal is averaged across each histogram window, it can encroach on the outer sides of the windows

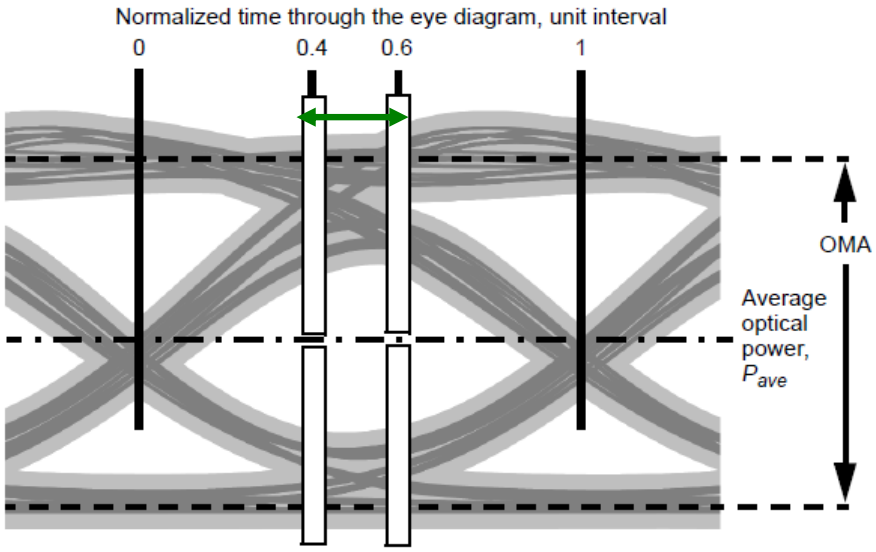


Figure 95–4—Illustration of the TDEC measurement

50 Gigabit Ethernet TDECQ

- Two histogram windows, centres 0.1 UI apart, each 0.04 UI wide
- Total 0.14 UI wide

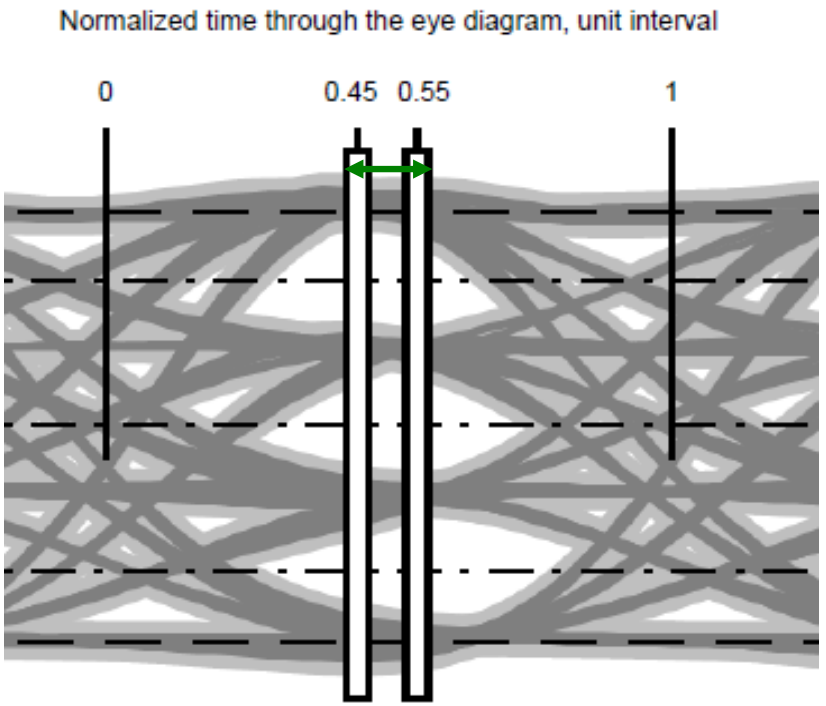


Figure 121–5—Illustration of the TDECQ

- In PAM4:
- On the one hand, even a clean eye has a few tenths of a UI of pattern-dependent jitter
  - Although electrical eyes won't have the inter-sub-eye skew shown here
- On the other hand, because of this unavoidable extra jitter on the signal, the receiver's recovered clock can't be expected to be as clean as for PAM2
- So the eye middle or histograms need to be wider, and signal jitter should be capped

CEI-nG-VSR-PAM4 and C2M

- VEC histogram and EW = mask
- ESMW ensures there is an open eye on both sides of the decision time
- Averaging across a single histogram gives more opportunity to encroach on one or two corners
- Histogram width (0.05 UI) is unusually narrow
  - Comment 41 suggests doubling this to 0.1 UI
  - But this would still be narrower than other eye mask / TDEC / TDECQ central regions

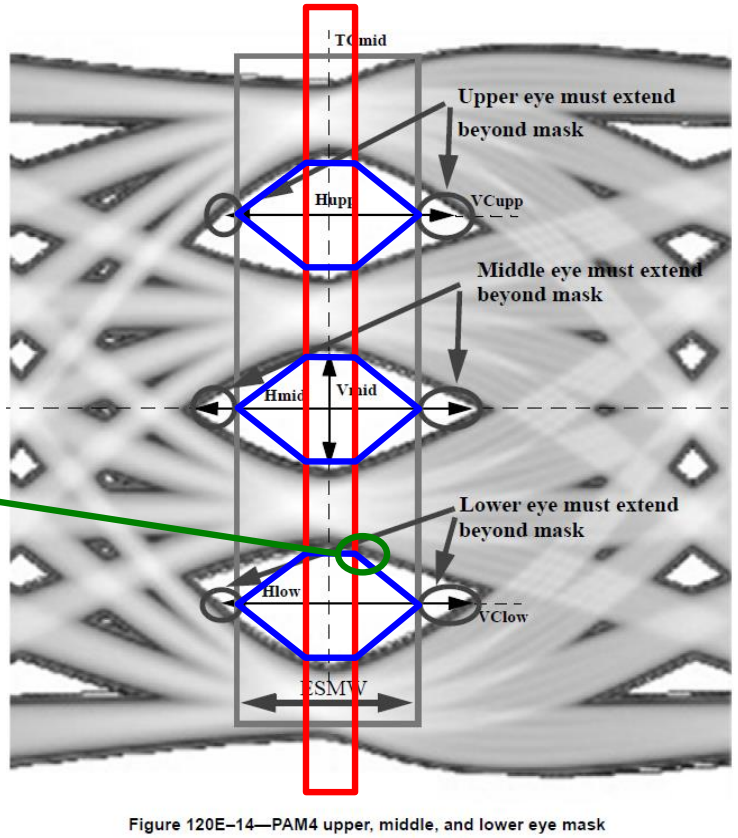
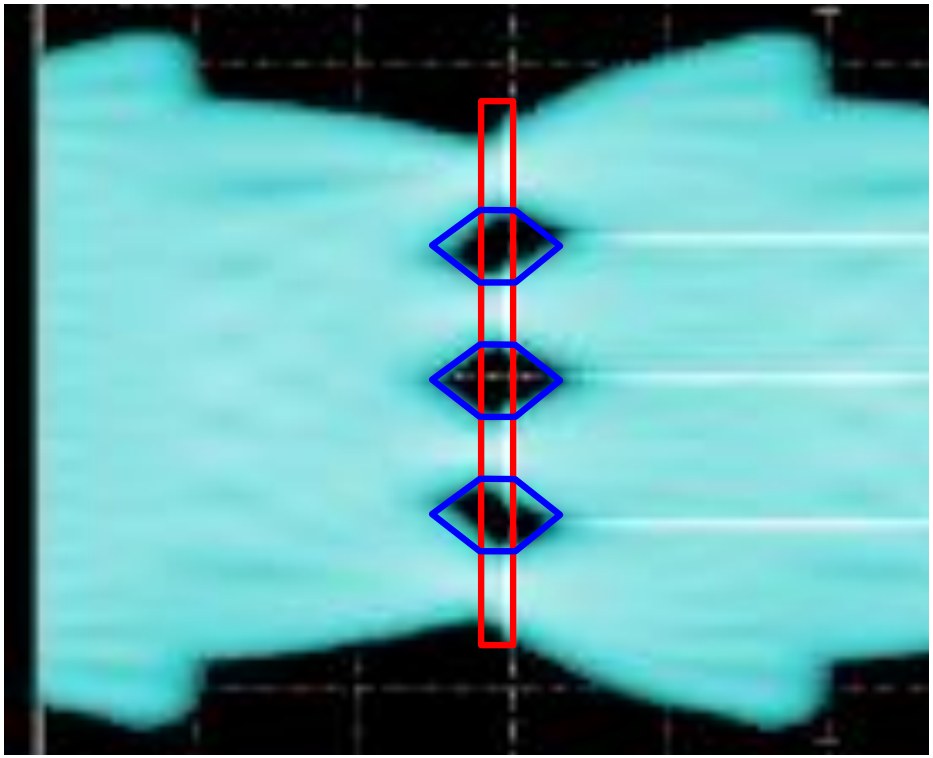


Figure 120E–14—PAM4 upper, middle, and lower eye mask

100G C2M in practice

- DFE steps happen in the middle of the jitter distribution
- Eye width / ESMW is determined by "asymmetric" edges (0 to 2, 1 to 3 and so on), which are measured correctly with or without DFE steps
- If all the signal's impairments and receiver noise were already in the measurement, any vertical eye opening would be enough
- But we would still need some eye width for receiver's jitter



From louchet_3ck_adhoc_01a_092320.pdf

Can we infer one from the other?

- If the eye is adequately open at say +/-0.07 UI, will it have adequately low jitter at the slicing level?
- If all eyes had the same slew time, and/or we made the VEC spec stringent enough to achieve the desired signal jitter limit on the fastest signals, it should
- But we don’t know if the first one is true and if the second one is desirable

Conclusion

- VEC with reasonable histogram width + eye width / ESMW = 6-sided mask
- 10-sided mask would improve measurement accuracy / time
- Reasonable width for receiver is between 0.1 and 0.2 UI, e.g. 0.14 UI as in TDECQ
- Control of jitter in the received signal is still necessary
- Keep eye width / ESMW method or use a mask