The Logic to Keep TP0a

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Overview

- Virtual TP0v test point
- Virtual computation method
- Current vs proposed test fixture loss
- Typical high end PCB loss
- Use of multi-coax for DUT board
- Summary.

TP0v Was Introduced in D1.3

- **See proposal from Liav and Mellitz [mellitz_3ck_adhoc_02_061020]**

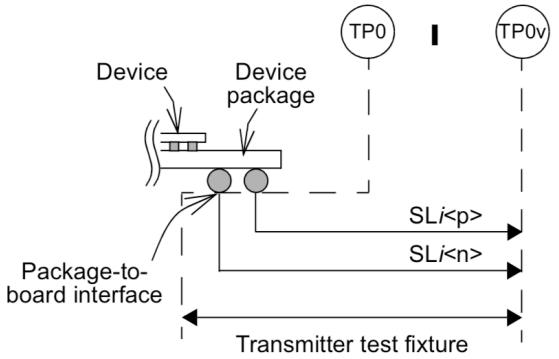
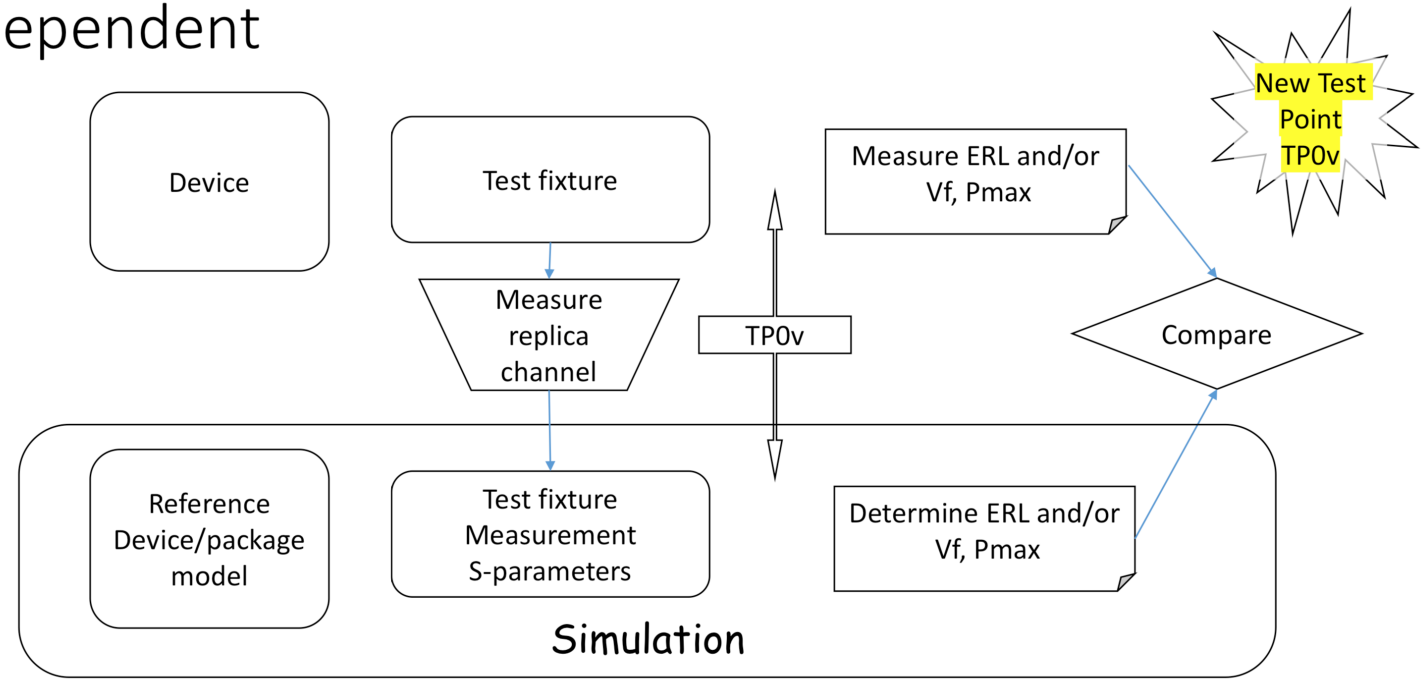


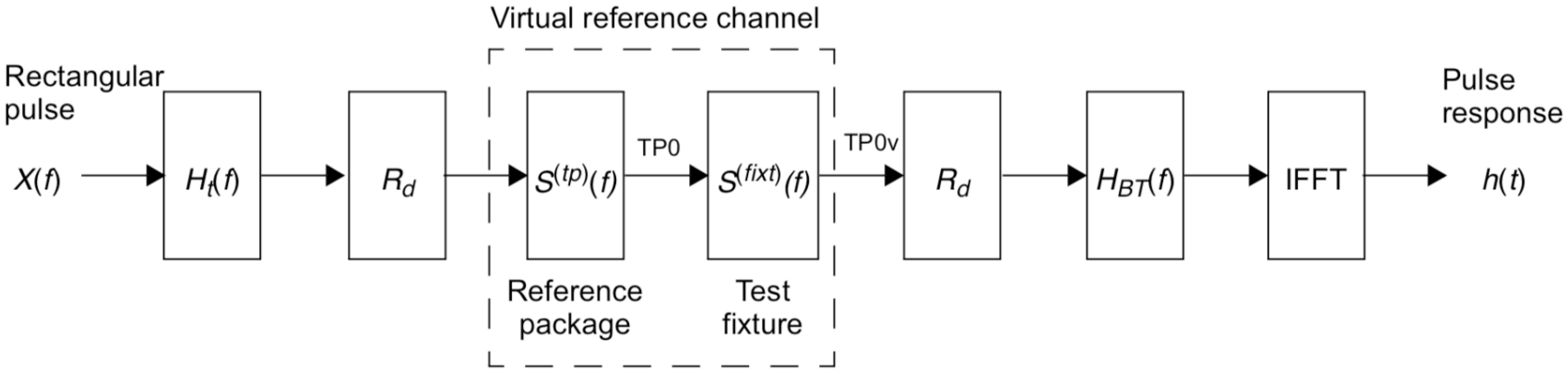
Figure 163–3—Transmitter test fixture and test points

Basic concept is to let the test fixture by user dependent



Method to Compute TP0v

- **TP0v is computed for longest package trace cascaded with test fixture**
  - Simulated value of Vf, ERL, and Vpeaks are compared with measured parameters
    - The difference between simulated and measured parameters are the normative delta limits
  - The normative specifications are dERL, dV, and dVpeak.

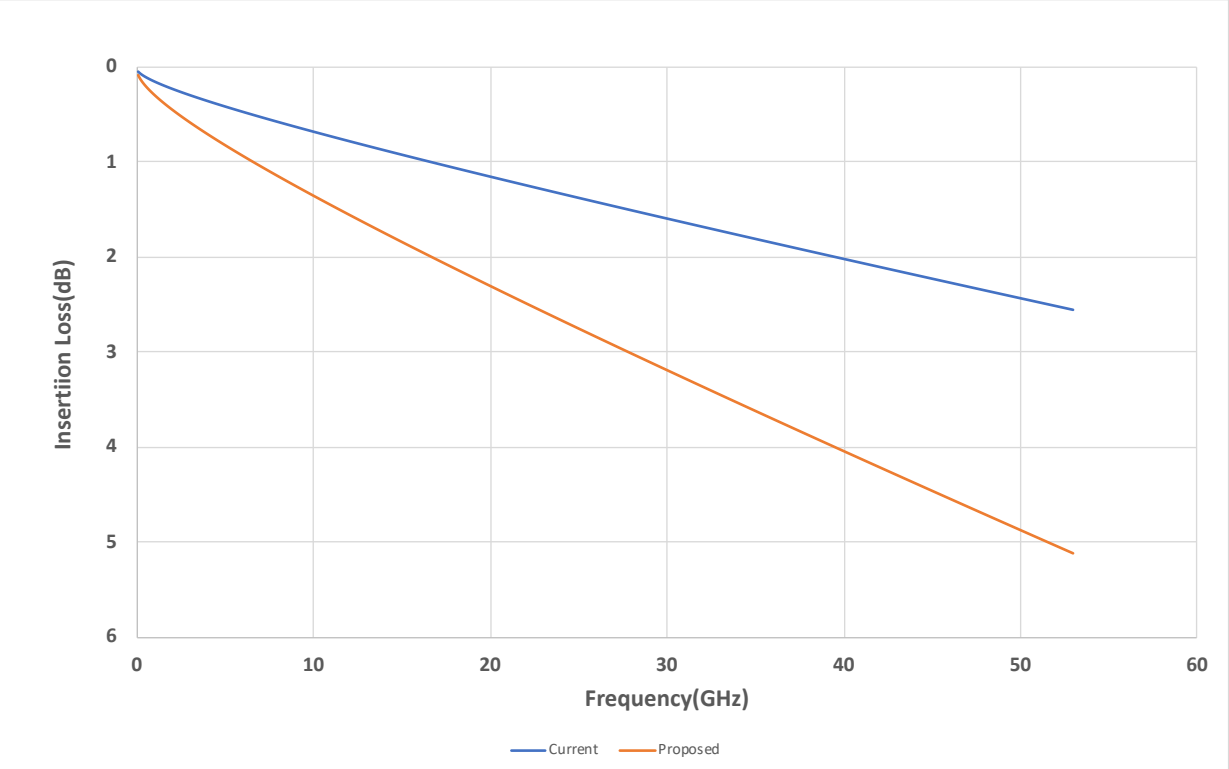


NOTE—The transmitter reference package uses the maximum length specified by the referring subclause.

Figure 163A–2—Configuration for transmitter reference steady-state voltage, pulse peak and ERL

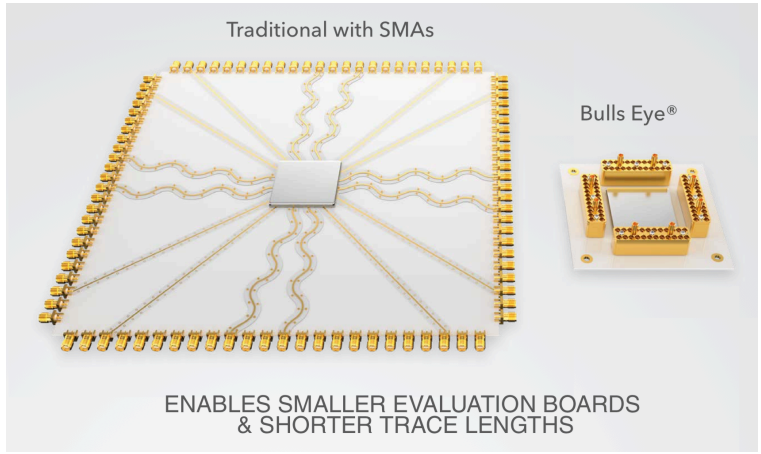
Current and Purposed Test Fixture Loss

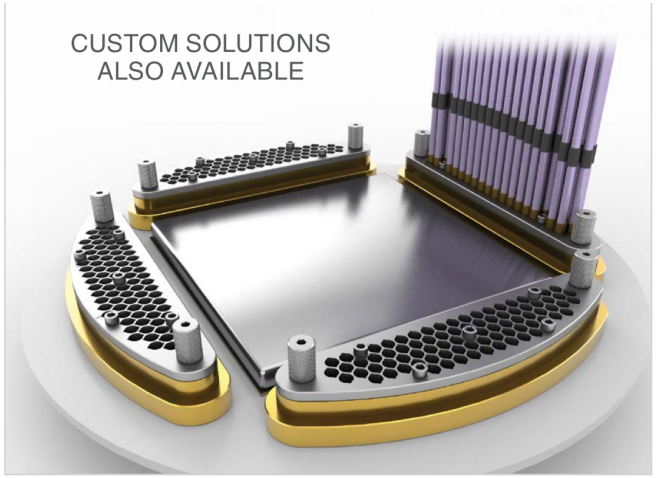
- **Recommend doubling the nominal loss from 1.4 dB to 2.8 dB 163.9.2.2 and use it also for transmit test fixture 163.9.2.1.1**
  - Proposed TX and RX test fixture loss=0.074+0.2104xsqrt(f)+0.0674xf
  - Mated test fixture MCB and HCB their respective losses were also increased to allow reasonable construction



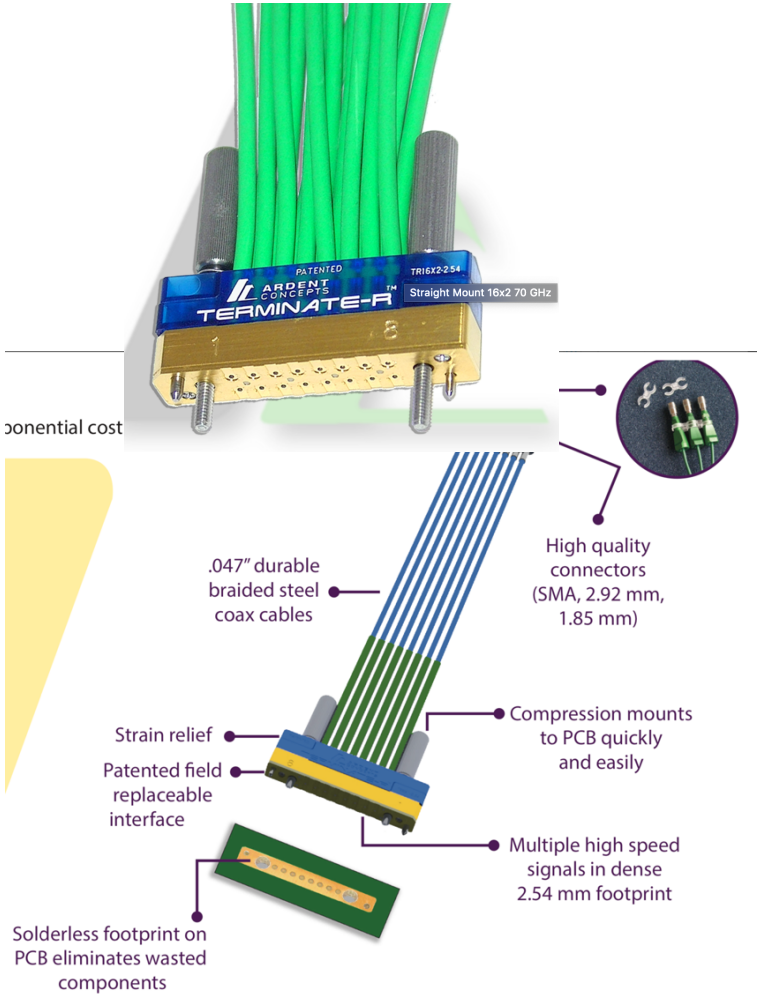
Example of High-Density Multi-Coax with 70 GHz BW

Samtec Bulls Eye





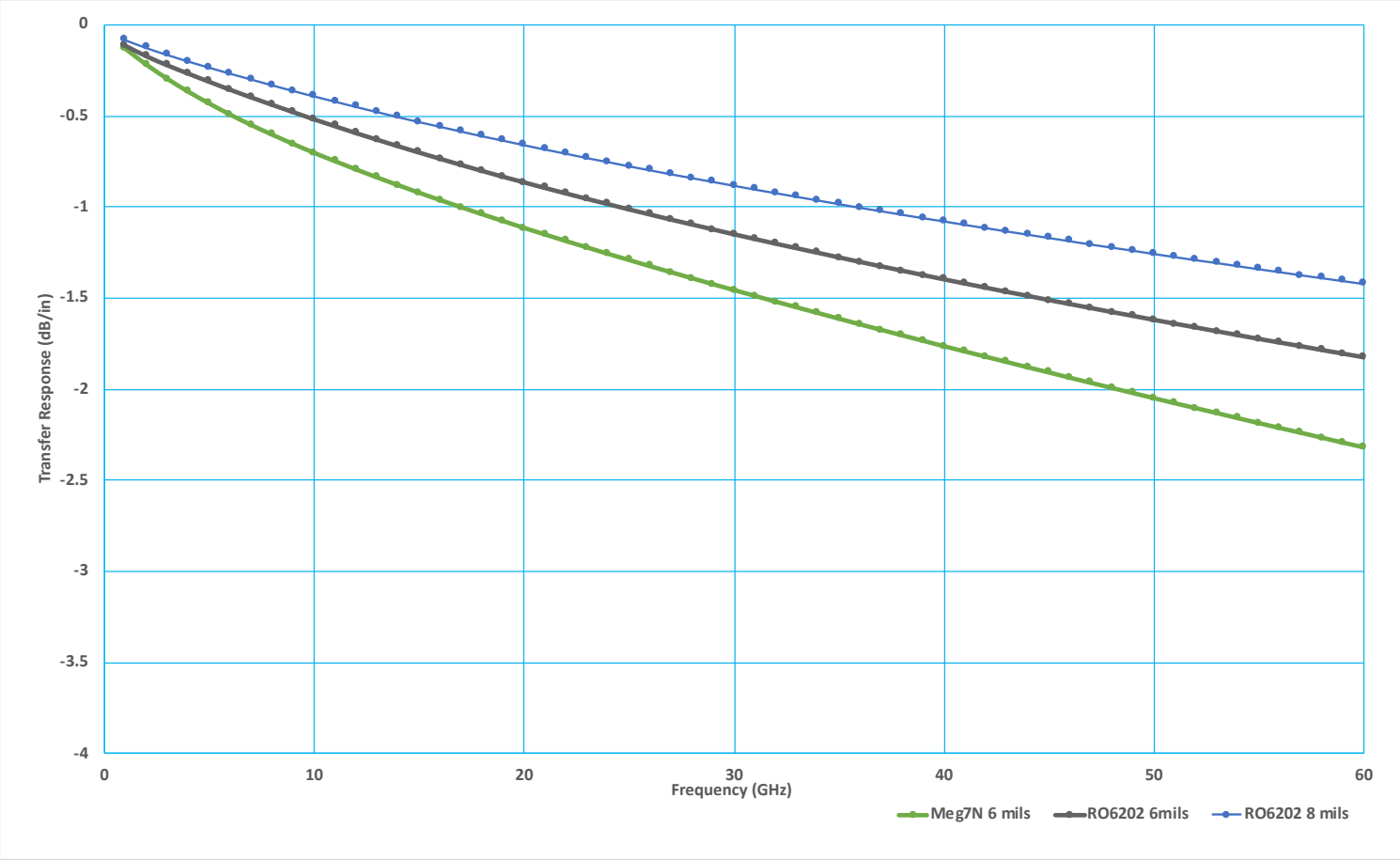
Ardent Terminator



Huber+Shuner MXPM70

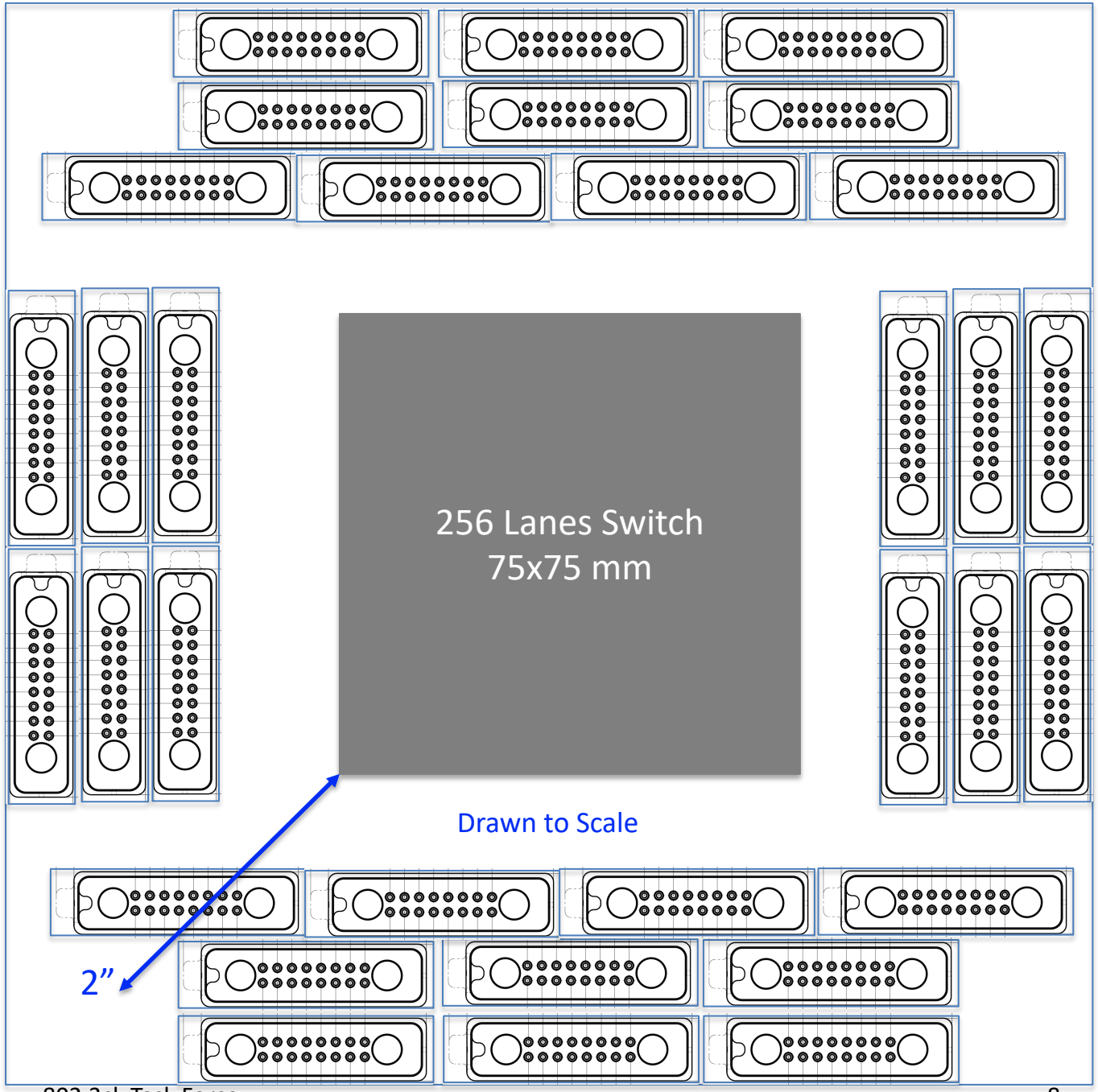
Typical High-End PCB Losses

- **PCB losses for Megtron 7N (6 mils trace) and Rogers 6202 (6 and 8 mils traces)**
  - It reasonable to assume high quality test board will have a construction with loss in 0.8-1.0 dB/in at 26.5 More conventional glass weave material such as TUC 933 and 943 have similar DF to RO6202.



Example 256 Lanes Switch Test Board

- **Can one breakout 256 lane switch with just 2”?**
  - Uses 32 2x8 multi-coax connectors on on top of the board and 32 on the bottom side
  - Alternatively one could use 2x16 multi-coax or custom multi-coax offered by some of the suppliers
  - One could also breakout out 512 lanes switch if needed using custom multi-coax connectors using both side of the board.



Summary

- **As illustrated multi-coax offer the required density and 70 GHz BW for direct implementation of TP0a**
  - Similar to MCB/HCB loss TP0a channel loss should be increased
  - Recommend to increased TP0a channel loss from 1.4 dB to 2.8 dB which allow 2-3” long PCB trace
- **TP0v virtual test point rely on cascaded package model vs an actual DUT board that likely will be using the same multi-coax construction**
  - Cascading DUT channel with reference IEEE package may result in unintended spurious response
  - It is assumed that ERL will improve with increased trace loss and Vf/Vpeak degrades where dERL, dVf, and dVpeak are introduced
  - There has not been any measured vs simulated verification of test method given the frequency
  - The dERL, dVf, and dVpeak may not be fully linear with increase or decrease of test board loss
- **Use of virtual test point TP5v will be significantly even more challenging**
- **TP0a/TP5a are implementable by increasing loss to 2.8 dB and provides reliable direct measurement**
- **TP0v method with further study and if proven reliable can be an informative method to account when test fixture loss deviate >+/- 0.4 dB from 2.8 dB**
  - But normative parameters should be based on 2.8 dB.