Medium Delay and CR ERL

Comments #113, #120

Amphenol Corporation

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Supporters

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Relevant Comments

#113, #120

Cl **162** *SC* **162.11.3** *P* **158** *L* **9** # 113

Kocsis, Sam — Amphenol

Comment Type **TR** *Comment Status* **X**

CR ERL parameter N is "3500"

SuggestedRemedy

Change to "5100", see background/consensus presentation

Proposed Response *Response Status* **O**

Cl **162** *SC* **162.5** *P* **137** *L* **19** # 120

Kocsis, Sam — Amphenol

Comment Type **TR** *Comment Status* **X**

one-way delay no more than "14ns"

SuggestedRemedy

one-way delay no more than "16ns", for consistency with ERL parameter values

Proposed Response *Response Status* **O**

- Presenting resolution of these comments together since each result impacts the other

Medium Delay for CR and KR

From D1p3

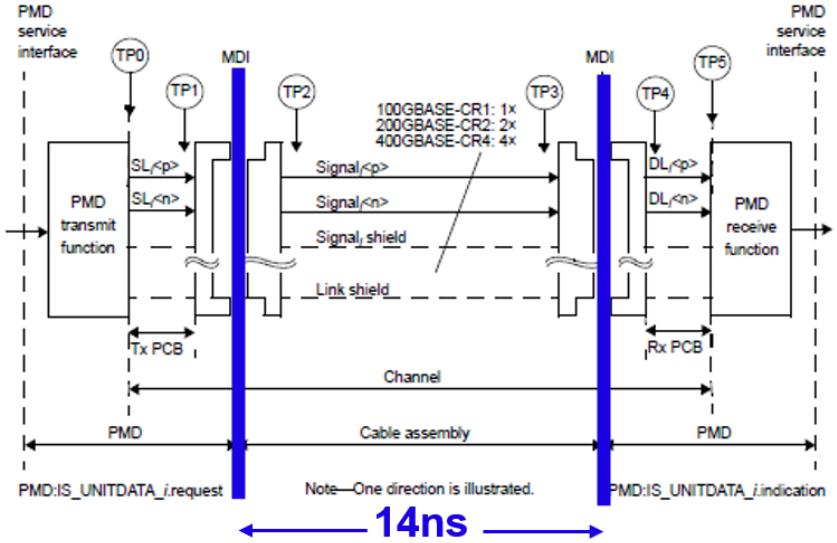

Figure 162–2—100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

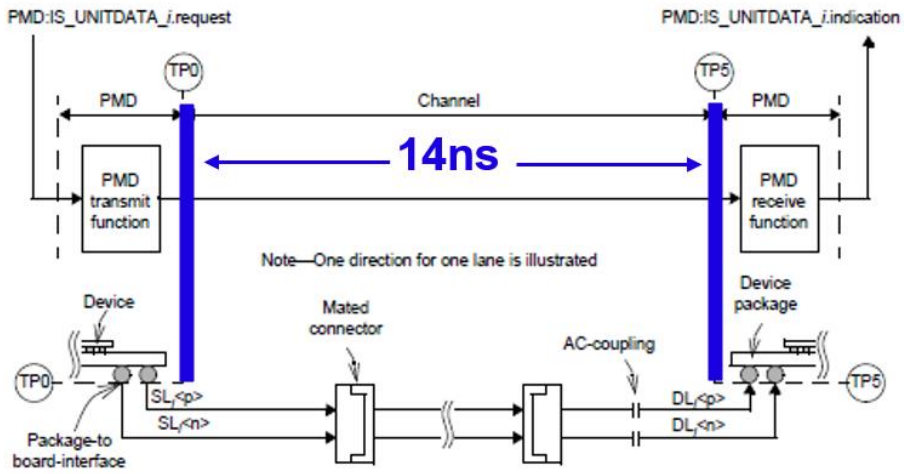

Figure 163–2—100GBASE-KR1, 200GBASE-KR2 or 400GBASE-KR4 link

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Measured Data

From 3ck contributed TP1-TP4 channels

- Two datasets available
  - Tracy_0719 – OSFP 2m Cables
  - Matoglu_0320 – OSFP 2m Cables
- All contributed channels have TP1-TP4 delay < 11ns
  - Estimated breakdown ->

3ck (TP1-TP4) One-Way Delay (below units are Seconds)							
		PCB (MCB)	Connector + Paddlecard	Cable (Er=2.0)	Connector + Paddlecard	PCB (MCB)	Total
Er	2.9	2.60E-10	1.00E-10	9.428E-09	1.00E-10	2.60E-10	1.01E-08
Er	3	2.64E-10	2.00E-10	9.428E-09	2.00E-10	2.64E-10	1.04E-08
Er	3.1	2.68E-10	2.00E-10	9.428E-09	2.00E-10	2.68E-10	1.04E-08
Er	3.2	2.73E-10	2.00E-10	9.428E-09	2.00E-10	2.73E-10	1.04E-08
Er	3.3	2.77E-10	2.00E-10	9.428E-09	2.00E-10	2.77E-10	1.04E-08
Er	3.4	2.81E-10	2.00E-10	9.428E-09	2.00E-10	2.81E-10	1.04E-08
Er	3.5	2.85E-10	2.00E-10	9.428E-09	2.00E-10	2.85E-10	1.04E-08

		PCB (MCB)	Connector + Paddlecard	Cable	Connector + Paddlecard	PCB (MCB)	Total
Er	1.8	2.65E-10	2.00E-10	8.944E-09	2.00E-10	2.65E-10	9.87E-09
Er	1.9	2.65E-10	2.00E-10	9.189E-09	2.00E-10	2.65E-10	1.01E-08
Er	2	2.65E-10	2.00E-10	9.428E-09	2.00E-10	2.65E-10	1.04E-08
Er	2.1	2.65E-10	2.00E-10	9.661E-09	2.00E-10	2.65E-10	1.06E-08
Er	2.2	2.65E-10	2.00E-10	9.888E-09	2.00E-10	2.65E-10	1.08E-08
Er	2.3	2.65E-10	2.00E-10	1.011E-08	2.00E-10	2.65E-10	1.10E-08
Er	2.4	2.65E-10	2.00E-10	1.033E-08	2.00E-10	2.65E-10	1.13E-08
Er	2.5	2.65E-10	2.00E-10	1.054E-08	2.00E-10	2.65E-10	1.15E-08

Based on contributed measurements (TP1-TP4) the one-way delay for a 2m cable is very unlikely to exceed a 14ns maximum delay

Comparing 3cd to 3ck

Channel Assumptions

3ck (TP0-TP5) One-Way Delay (below units are Seconds)							
		PCB (Host)	Connector + Paddlecard	Cable (Er=2.0)	Connector + Paddlecard	PCB (Host)	Total
Er	2.9	1.42E-09	2.00E-10	9.428E-09	2.00E-10	1.42E-09	1.27E-08
Er	3	1.44E-09	2.00E-10	9.428E-09	2.00E-10	1.44E-09	1.27E-08
Er	3.1	1.47E-09	2.00E-10	9.428E-09	2.00E-10	1.47E-09	1.28E-08
Er	3.2	1.49E-09	2.00E-10	9.428E-09	2.00E-10	1.49E-09	1.28E-08
Er	3.3	1.51E-09	2.00E-10	9.428E-09	2.00E-10	1.51E-09	1.29E-08
Er	3.4	1.54E-09	2.00E-10	9.428E-09	2.00E-10	1.54E-09	1.29E-08
Er	3.5	1.56E-09	2.00E-10	9.428E-09	2.00E-10	1.56E-09	1.29E-08

		PCB (Host)	Connector + Paddlecard	Cable (Er=2.3)	Connector + Paddlecard	PCB (Host)	Total
Er	2.9	1.42E-09	2.00E-10	1.011E-08	2.00E-10	1.42E-09	1.33E-08
Er	3	1.44E-09	2.00E-10	1.011E-08	2.00E-10	1.44E-09	1.34E-08
Er	3.1	1.47E-09	2.00E-10	1.011E-08	2.00E-10	1.47E-09	1.34E-08
Er	3.2	1.49E-09	2.00E-10	1.011E-08	2.00E-10	1.49E-09	1.35E-08
Er	3.3	1.51E-09	2.00E-10	1.011E-08	2.00E-10	1.51E-09	1.35E-08
Er	3.4	1.54E-09	2.00E-10	1.011E-08	2.00E-10	1.54E-09	1.36E-08
Er	3.5	1.56E-09	2.00E-10	1.011E-08	2.00E-10	1.56E-09	1.36E-08

3cd (TP0-TP5) One-Way Delay (below units are Seconds)							
		PCB (Host)	Connector + Paddlecard	Cable (Er=2.0)	Connector + Paddlecard	PCB (Host)	Total
Er	2.9	1.42E-09	2.00E-10	1.414E-08	2.00E-10	1.42E-09	1.74E-08
Er	3	1.44E-09	2.00E-10	1.414E-08	2.00E-10	1.44E-09	1.74E-08
Er	3.1	1.47E-09	2.00E-10	1.414E-08	2.00E-10	1.47E-09	1.75E-08
Er	3.2	1.49E-09	2.00E-10	1.414E-08	2.00E-10	1.49E-09	1.75E-08
Er	3.3	1.51E-09	2.00E-10	1.414E-08	2.00E-10	1.51E-09	1.76E-08
Er	3.4	1.54E-09	2.00E-10	1.414E-08	2.00E-10	1.54E-09	1.76E-08
Er	3.5	1.56E-09	2.00E-10	1.414E-08	2.00E-10	1.56E-09	1.77E-08

		PCB (Host)	Connector + Paddlecard	Cable (Er=2.3)	Connector + Paddlecard	PCB (Host)	Total
Er	2.9	1.42E-09	2.00E-10	1.517E-08	2.00E-10	1.42E-09	1.84E-08
Er	3	1.44E-09	2.00E-10	1.517E-08	2.00E-10	1.44E-09	1.85E-08
Er	3.1	1.47E-09	2.00E-10	1.517E-08	2.00E-10	1.47E-09	1.85E-08
Er	3.2	1.49E-09	2.00E-10	1.517E-08	2.00E-10	1.49E-09	1.85E-08
Er	3.3	1.51E-09	2.00E-10	1.517E-08	2.00E-10	1.51E-09	1.86E-08
Er	3.4	1.54E-09	2.00E-10	1.517E-08	2.00E-10	1.54E-09	1.86E-08
Er	3.5	1.56E-09	2.00E-10	1.517E-08	2.00E-10	1.56E-09	1.87E-08

- Spec for 3cd “one-way delay thru medium” was 20ns
- POR for 3ck is 14ns
  - The delay attributed to the cable moving from 3m to 2m is ~5ns
  - **A more appropriate maximum delay for 3ck may be 15-16ns**

Medium Delay
Defining the specification

- Based on contributed measurements (TP1-TP4) the one-way delay for a 2m cable is very unlikely to exceed a 14ns maximum delay
- Setting the maximum delay will limit the maximum copper cable length for future single-lane 100Gb/s PHY applications
  - Current objectives are to support “at least 2m”
- You *could* go up to 4m and still be under 20ns

3ck (TP2-TP3) One-Way Delay (below units are Seconds)							
		PCB (Host)	Connector + Paddlecard	Cable (2m)	Connector + Paddlecard	PCB (Host)	Total
Er	1.8	0.00E+00	0.00E+00	8.944E-09	0.00E+00	0.00E+00	8.94E-09
Er	1.9	0.00E+00	0.00E+00	9.189E-09	0.00E+00	0.00E+00	9.19E-09
Er	2	0.00E+00	0.00E+00	9.428E-09	0.00E+00	0.00E+00	9.43E-09
Er	2.1	0.00E+00	0.00E+00	9.661E-09	0.00E+00	0.00E+00	9.66E-09
Er	2.2	0.00E+00	0.00E+00	9.888E-09	0.00E+00	0.00E+00	9.89E-09
Er	2.3	0.00E+00	0.00E+00	1.011E-08	0.00E+00	0.00E+00	1.01E-08
Er	2.4	0.00E+00	0.00E+00	1.033E-08	0.00E+00	0.00E+00	1.03E-08

		PCB (Host)	Connector + Paddlecard	Cable (3m)	Connector + Paddlecard	PCB (Host)	Total
Er	1.8	0.00E+00	0.00E+00	1.342E-08	0.00E+00	0.00E+00	1.34E-08
Er	1.9	0.00E+00	0.00E+00	1.378E-08	0.00E+00	0.00E+00	1.38E-08
Er	2	0.00E+00	0.00E+00	1.414E-08	0.00E+00	0.00E+00	1.41E-08
Er	2.1	0.00E+00	0.00E+00	1.449E-08	0.00E+00	0.00E+00	1.45E-08
Er	2.2	0.00E+00	0.00E+00	1.483E-08	0.00E+00	0.00E+00	1.48E-08
Er	2.3	0.00E+00	0.00E+00	1.517E-08	0.00E+00	0.00E+00	1.52E-08
Er	2.4	0.00E+00	0.00E+00	1.549E-08	0.00E+00	0.00E+00	1.55E-08

		PCB (Host)	Connector + Paddlecard	Cable (4m)	Connector + Paddlecard	PCB (Host)	Total
Er	1.8	0.00E+00	0.00E+00	1.789E-08	0.00E+00	0.00E+00	1.79E-08
Er	1.9	0.00E+00	0.00E+00	1.838E-08	0.00E+00	0.00E+00	1.84E-08
Er	2	0.00E+00	0.00E+00	1.886E-08	0.00E+00	0.00E+00	1.89E-08
Er	2.1	0.00E+00	0.00E+00	1.932E-08	0.00E+00	0.00E+00	1.93E-08
Er	2.2	0.00E+00	0.00E+00	1.978E-08	0.00E+00	0.00E+00	1.98E-08
Er	2.3	0.00E+00	0.00E+00	2.022E-08	0.00E+00	0.00E+00	2.02E-08
Er	2.4	0.00E+00	0.00E+00	2.066E-08	0.00E+00	0.00E+00	2.07E-08

Impact of Medium Delay

…with respect to CR Compliance Measurements

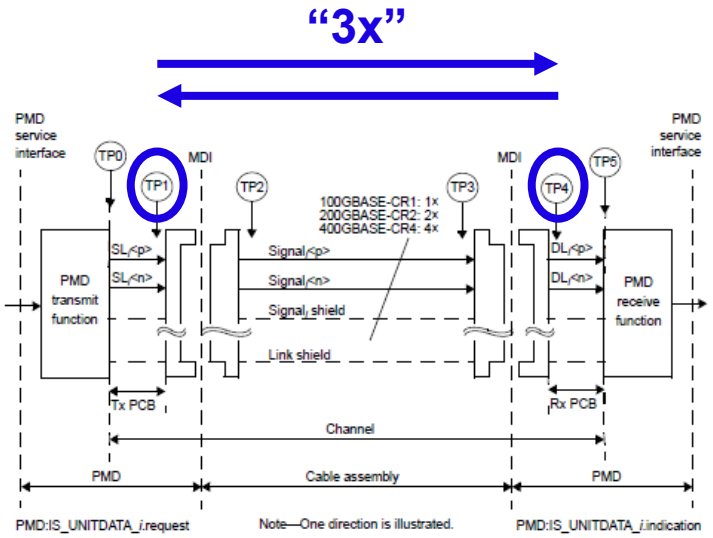

Figure 162–2—100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

Table 162–15—Cable assembly ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	TBD	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	7000	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI

- Request for ERL calculation to define the length of the reflection signal as 3x the round-trip flight time (mellitz_3ck_01b_0320)
- N = fb * "3x" round-trip delay
- f_step = ("3x" round-trip delay)$^{-1}$

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Impact of Medium Delay Value

…with respect to CR Compliance Measurements

- One-way delay (TP1-TP4) is largely determined by the cable (medium delay)
- If one-way medium delay 16ns, then…
  - …TP1-TP4 delay is ~16ns
    - … then f_step for CR compliance can be 10MHz
    - … then a practical setting for N would be 5100

Calculation of Frequency Step-Size				
TP1-TP4 One-Way Delay (seconds)	f_step (Hz)	"3x" Round Trip Delay (seconds)	fb (Hz)	N
9.00E-09	1.85E+07	5.40E-08	5.31E+10	2869
1.00E-08	1.67E+07	6.00E-08	5.31E+10	3188
1.10E-08	1.52E+07	6.60E-08	5.31E+10	3506
1.20E-08	1.39E+07	7.20E-08	5.31E+10	3825
1.30E-08	1.28E+07	7.80E-08	5.31E+10	4144
1.40E-08	1.19E+07	8.40E-08	5.31E+10	4463
1.50E-08	1.11E+07	9.00E-08	5.31E+10	4781
1.60E-08	1.04E+07	9.60E-08	5.31E+10	5100
1.70E-08	9.80E+06	1.02E-07	5.31E+10	5419
1.80E-08	9.26E+06	1.08E-07	5.31E+10	5738
1.90E-08	8.77E+06	1.14E-07	5.31E+10	6056
2.00E-08	8.33E+06	1.20E-07	5.31E+10	6375
2.10E-08	7.94E+06	1.26E-07	5.31E+10	6694
2.20E-08	7.58E+06	1.32E-07	5.31E+10	7013

Medium Delay for CR

Proposal Resolution

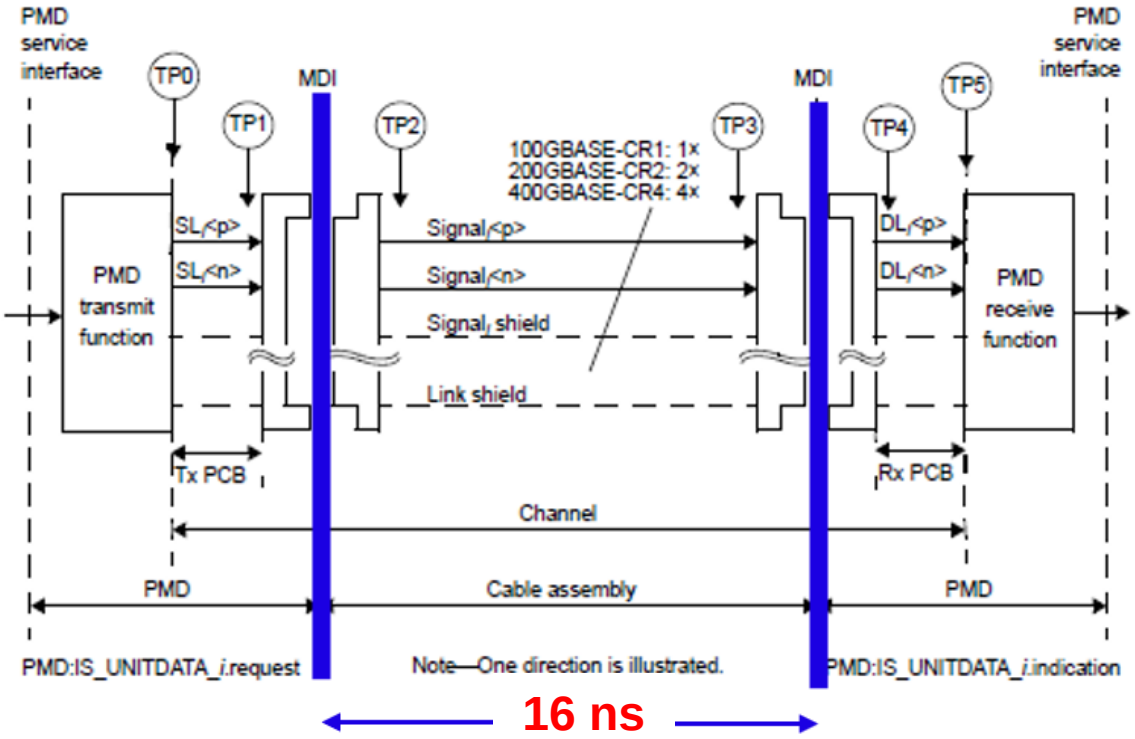

Figure 162–2—100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

ERL Compliance Parameters

Proposed Resolution

Table 162–17—Cable assembly ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.01	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	5100	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI
Twice the propagation delay associated with the test fixture	T_{fx}	0.2[a]	ns
Tukey window flag	tw	1	—

[a]The specified T_{fx} value represents twice the transmission line delay which sufficiently mitigates the test point and transmission line return loss.

- Set N based on the “3x round trip delay” of the max one delay
- Other parameters would remain unchanged from D1p3
  - Note difference in T_fx from D1p2