TRANSMITTER EQUALIZATION DEFINITION IN RECEIVER TESTS

Supporting comments 70 and 231

Adee Ran, Intel

The comments

Cl 163 SC 163.9.3.3 P 181 L 34 # 70

Ran, Adee Intel

Comment Type T *Comment Status* D *RITT*

The exception that "transmitter equalization is configured by management..." is taekn from the AUI-C2C (Annex 120D) which does not have a training protocol.

This clause is for the KR PMD that does have a training protocol defined, so this exception is out of place. The procedure in Annex 93C should be used as is.

SuggestedRemedy

Delete the sendence "with the exception that transmitter equalization is configured by management (see 120D.3.2.3) to the settings that provide the lowest FEC symbol error ratio".

Proposed Response *Response Status* W

PROPOSED ACCEPT.

Cl 163 SC 163.9.3.3 P 181 L 35 # 231

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *RITT*

This isn't right: "transmitter equalization is configured by management (see 120D.3.2.3) to the settings that provide the lowest FEC symbol error ratio". It's the receiver's responsibility to choose an adequate transmitter equalization setting. Further, the transmitter could be a test instrument that doesn't do 802.3 management. What has 120D.3.2.3 got to do with it? Was this text copied from a C2C clause?

SuggestedRemedy

Correct the text. The transmitter equalization is what the receiver asks for after it's had a chance to train, or a default if it doesn't ask for anything in particular.

Same for 163.9.3.4 Receiver jitter tolerance.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve the issue with 163.9.3.3 using the response to comment #70.
For 163.9.3.4, insert an exception as follows:
"a) The transmitter coefficients are set according to the procedure in 93C.2."
For task force review.

Text in question (1)

163.9.3.3 Receiver interference tolerance

Receiver interference tolerance is defined by the procedure in Annex 93C with the exception that transmitter equalization is configured by management (see 120D.3.2.3) to the settings that provide the lowest FEC symbol error ratio.

- It is identical (almost) the C2C test definition in Annex 120D… but the PMD test definition in clause 137 is also based on 120D:

137.9.3 Receiver characteristics

Receiver electrical characteristics are specified at TP5a. The receiver shall meet the specifications given in Table 120D–5 with the following exceptions:

a) PCS FEC symbol error ratio (max) values in Table 120D–6 and Table 120D–7 are all 10^{-3}. For 50GBASE-KR and 100GBASE-KR2, RS-FEC symbol error ratio is used instead of PCS FEC symbol error ratio.
b) Insertion loss at 13.2813 GHz values for Test 1 are 14.5 (min) and 15.5 (max).
c) Insertion loss at 13.2813 GHz values for Test 2 are 29.5 (min) and 30.5 (max).
d) RSS_DFE4 value for Test 1 is 0.05.
e) Receiver jitter tolerance (see 120D.3.2.2) is tested using the test channel used for receiver interference tolerance Test 2 (see item c).
f) The differential input return loss (min) requirements are replaced by the receiver ERL specification in 137.9.3.1.

- The exception in 120D-5 (highlighted above) is not excluded, so it also holds in clause 137!
- Apparently, an oversight in 802.3cd – the test procedure in Annex 93C is defined for PMDs which include a PMD management function (link training). Annex 120D does not include this function, so it adds the exception, but it was not needed for clause 137. It should not be carried over to this project – the exception should be removed.
- Comment #70 addresses this change (and the proposed response is fine).

Text in question (2)

163.9.3.4 Receiver jitter tolerance

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 162–15. The test setup shown in Figure 93–12, or its equivalent, is used. The test channel meets the insertion loss requirement for Test 2 in Table 163–10. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0v. The test procedure is the same as the one described in 120D.3.2.1, with the following exceptions:

a) No broadband noise is added.

b) The test channel COM, calculated per items d) through g) in 120D.3.2.1, is at least 3 dB.

c) For the COM parameter calibration described in 120D.3.2.1 item e), the test channel transmitter J_{RMS} and J3u values are measured with the jitter frequency and amplitude set according to Case E from Table 162–15.

d) As an alternative to using the scrambled idle test pattern and measuring FEC symbol error ratio it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10. Note that this requirement can be somewhat more stringent than using the scrambled idle test pattern and measuring FEC symbol error ratio, and therefore failing this test requirement with the PRBS31Q pattern does not necessarily imply a failure of the jitter tolerance test.

- As comment #231 notes, the test procedure in 120D.3.2.1 does not address link training.
- The problem here:
  - There is no RJT procedure in Annex 93C that can be referred to.
  - The RJT procedures in 93.8.2.4 and in 111.8.3.2 are too specific to the respective PMDs (e.g. in terms of BER requirements); They also specify only two jitter frequencies.
- A suitable procedure definition is proposed in the next slide.

Proposal

- Apply the following changes to 163.9.3.4 to make it refer to the RIT procedure in this clause (163.9.3.3) and to Annex 93C, instead of 120D.3.2.1 – thus including link training:

163.9.3.4 Receiver jitter tolerance

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 162–15. The test setup shown in Figure 93–12 , or its equivalent, is used. The test channel meets the insertion loss requirement for Test 2 in Table 163–10. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0v. The test procedure is the same as the one described in ~~120D.3.2.1~~163.9.3.3, with the following exceptions:

a) No broadband noise is added.

b) The test channel COM, calculated per items ~~d) through g) in 120D.3.2.1~~ 3) through 7) in 93C.2, is at least 3 dB.

c) For the COM parameter calibration described in ~~120D.3.2.1 item c)~~ 93C.2 item 7), the test channel transmitter J_{RMS} and J3u values are measured with the jitter frequency and amplitude set according to Case E from Table 162–15.

d) As an alternative to using the scrambled idle test pattern and measuring FEC symbol error ratio it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10. Note that this requirement can be somewhat more stringent than using the scrambled idle test pattern and measuring FEC symbol error ratio, and therefore failing this test requirement with the PRBS31Q pattern does not necessarily imply a failure of the jitter tolerance test.

The receiver under test shall meet the FEC symbol error ratio requirements for each case in Table 162–15.

Proposed response to comment #231

ACCEPT IN PRINCIPLE.

Implement the changes highlighted in slide 5 of https://www.ieee802.org/3/ck/public/20_10/ran_3ck_03_1020.pdf.