ERL Proposal for C2M

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Outlines

- Background
- ERL analysis of IEEE C2M channels
- Proposal

Background

- Supporting material for the following comments
  - #99 – Host input ERL
  - #90 – Host output ERL
- Previously, ERL of C2M were discussed in the following contributions
  - sun_3ck_01b_0919.pdf, sun_3ck_02_1119.pdf, wu_3ck_01a_1119.pdf, mellitz_3ck_02a_1119.pdf
- However, they were all based on previous ERL parameters
  - There were new ERL parameters in 802.3ck D1p3
- Re-do ERL analysis of 19 C2M channels (host-to-module) in wu_3ck_01a_1119.pdf based on D1p3 parameters & propose ERL spec
  - Propose ERL (min) = 8.5 dB in Table 120G-1 & 120G-5

Channel and Device/Package Parameters

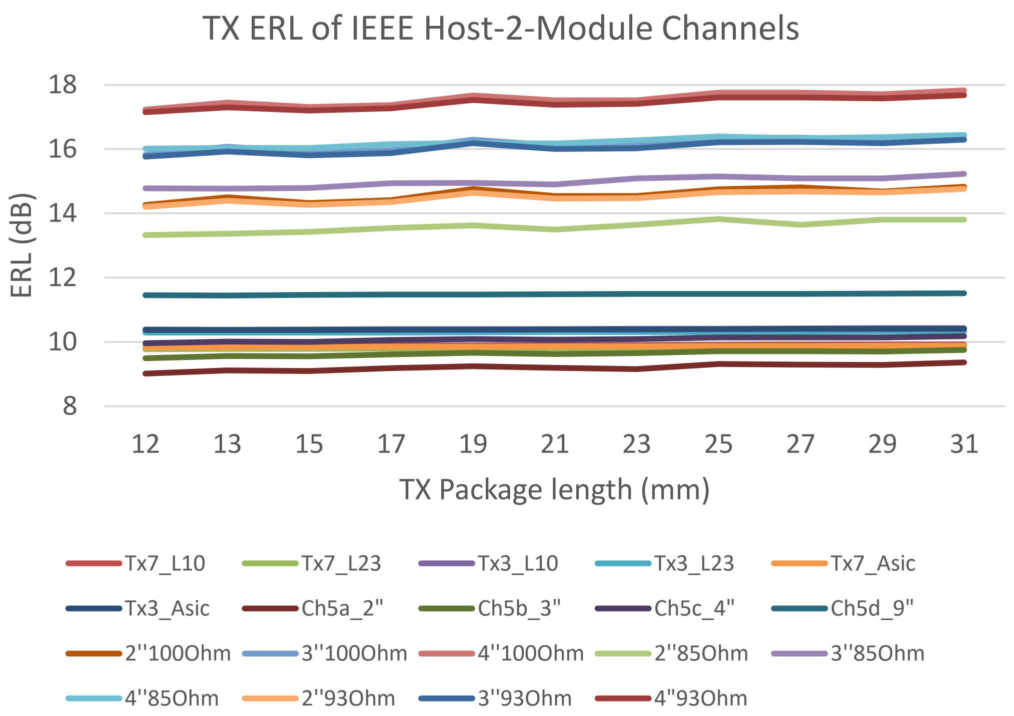
- Channel list
  - 19 IEEE C2M host-to-module channels
  - Detailed list in the appendix
- Package Parameters
  - Sweep host TX package trace length, z_p1 (TX) = [12, 13:2:31], total 11 cases
- COM parameter settings in the appendix
  - COM 2.95
- ERL parameters by D1p3
- Total 19*11 = 209 cases

ERL Sensitivity Analysis over 19 C2M Channels

Contribution	Zip files	Channel	SxP Files	Zp (mm)										
				12	13	15	17	19	21	23	25	27	29	31
lim_3ck_01a_0319	lim_3ck_01_0319_c2m.zip	Tx7_L10	112G_16dB_(QSFPDD+module card)_TX7_L10	9.87	9.87	9.88	9.89	9.89	9.90	9.90	9.91	9.92	9.92	9.92
		Tx7_L23	112G_16dB_(QSFPDD+module card)_TX7_L23	9.77	9.78	9.78	9.79	9.80	9.80	9.81	9.81	9.81	9.82	9.83
		Tx3_L10	112G_16dB_(QSFPDD+module card)_TX3_L10	10.39	10.38	10.39	10.40	10.40	10.40	10.41	10.41	10.42	10.43	10.43
		Tx3_L23	112G_16dB_(QSFPDD+module card)_TX3_L23	10.29	10.29	10.29	10.29	10.30	10.31	10.31	10.31	10.32	10.33	10.33
		Tx7_Asic	112G_16dB_(QSFPDD+module card)_TX7_Asic	9.83	9.83	9.84	9.85	9.85	9.86	9.86	9.87	9.87	9.88	9.88
		Tx3_Asic	112G_16dB_(QSFPDD+module card)_TX3_Asic	10.37	10.37	10.37	10.38	10.38	10.39	10.39	10.40	10.41	10.41	10.41
lim_3ck_adhoc_01_	073119 lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace	9.01	9.11	9.09	9.18	9.24	9.19	9.15	9.31	9.29	9.28	9.36
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace	9.49	9.56	9.55	9.61	9.66	9.62	9.65	9.71	9.71	9.70	9.75
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace	9.96	10.01	10.00	10.06	10.09	10.07	10.09	10.14	10.14	10.14	10.18
		Ch5d_9"	Channel5d_Smaller_Pad_9inch_trace	11.45	11.44	11.46	11.47	11.47	11.48	11.49	11.49	11.49	11.50	11.51
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2''100Ohm	C2M_2p0in_100Ohm_thru1.s4p	14.26	14.50	14.32	14.41	14.76	14.54	14.54	14.75	14.81	14.68	14.83
		3''100Ohm	C2M_3p0in_100Ohm_thru1.s4p	15.82	16.07	15.90	15.96	16.29	16.11	16.11	16.35	16.35	16.29	16.40
		4''100Ohm	C2M_4p0in_100Ohm_thru1.s4p	17.23	17.45	17.31	17.37	17.67	17.52	17.52	17.76	17.76	17.71	17.83
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	2''85Ohm	C2M_2p0in_85Ohm_thru1.s4p	13.33	13.36	13.42	13.54	13.62	13.49	13.64	13.82	13.64	13.80	13.80
		3''85Ohm	C2M_3p0in_85Ohm_thru1.s4p	14.78	14.77	14.79	14.94	14.95	14.90	15.09	15.15	15.09	15.09	15.23
		4''85Ohm	C2M_4p0in_85Ohm_thru1.s4p	16.01	16.03	16.03	16.15	16.19	16.17	16.27	16.39	16.33	16.37	16.44
	akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2''93Ohm	C2M_2p0in_93Ohm_thru1.s4p	14.20	14.39	14.26	14.35	14.64	14.46	14.47	14.66	14.68	14.65	14.76
		3''93Ohm	C2M_3p0in_93Ohm_thru1.s4p	15.76	15.92	15.80	15.87	16.18	16.00	16.02	16.21	16.22	16.18	16.29
		4''93Ohm	C2M_4p0in_93Ohm_thru1.s4p	17.15	17.30	17.20	17.27	17.53	17.38	17.41	17.61	17.61	17.58	17.68

ERL Analysis and Proposal

- ERL varies channel-by-channel
- ERL is not sensitive to TX package length
- Min ERL at Ch5a_2'', Jane Lim's 2 inch short channel
  - 9.01 dB
- If we considered all the channels are valid,
  - we could set ERL (min) = 8.5 dB



Proposals

- Change the value of “Effective return loss (min)” from ‘TBD’ to 8.5 in Table 120G-1 Host output characteristics
- Change the value of “Effective return loss (min)” from ‘TBD’ to 8.5 in Table 120G-5 Host input characteristics

Thank You

C2M Host-to-Module Channels for Analysis

Contribution	Zip files	Channel	SxP Files
lim_3ck_01a_0319	lim_3ck_01_0319_c2m.zip	Tx7_L10	112G_16dB_(QSFPDD+module card)_TX7_L10
		Tx7_L23	112G_16dB_(QSFPDD+module card)_TX7_L23
		Tx3_L10	112G_16dB_(QSFPDD+module card)_TX3_L10
		Tx3_L23	112G_16dB_(QSFPDD+module card)_TX3_L23
		Tx7_Asic	112G_16dB_(QSFPDD+module card)_TX7_Asic
		Tx3_Asic	112G_16dB_(QSFPDD+module card)_TX3_Asic
lim_3ck_adhoc_01_073119	lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace
		Ch5d_9"	Channel5d_Smaller_Pad_9inch_trace
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2"100Ohm	C2M_2p0in_100Ohm_thru1.s4p
		3"100Ohm	C2M_3p0in_100Ohm_thru1.s4p
		4"100Ohm	C2M_4p0in_100Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	2"85Ohm	C2M_2p0in_85Ohm_thru1.s4p
		3"85Ohm	C2M_3p0in_85Ohm_thru1.s4p
		4"85Ohm	C2M_4p0in_85Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2"93Ohm	C2M_2p0in_93Ohm_thru1.s4p
		3"93Ohm	C2M_3p0in_93Ohm_thru1.s4p
		4"93Ohm	C2M_4p0in_93Ohm_thru1.s4p

COM spread sheet – IEEE C2M

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 12; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[12 12; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	vp/vf=.694
A_fe	0.415	V	vp/vf=.694
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.2:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(-3)	[0]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	4	UI	
b_max(1)	**0.4**		**As/dffe1**
b_max(2..N_b)	**[0.15 0.15 0.1]**		**As/dfe2..N_b**
b_min(1)	**0.1**		**As/dffe1**
b_min(2..N_b)	**[-0.15 - 0.15 - 0.05]**		**As/dfe2..N_b**
g_DC	[-13:1:-0]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:0.5:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
G_Qual	[-2 -9 ;-2 -12; -4 -12;-6 -13]	dB	ranges
G2_Qual	[0 -1 -2 -3]	dB	ranges

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{d	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	9	db
EH_min	15	mV
ERL Pass threshold	7	dB
DER_0	0.00001	
T_r	0.0075	ns
FORCE_TR	1	logical
PMD_type	C2M	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0.00E+00	
rho_x	0.618	
fixture delay time	[0 .2e-9]	port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	0.000000041	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN parameters (v2.73+)		
f_f	0.594	Hz f_r specified in first colum
f_n	0.594	GHz
f_2	40	GHz
A_ft	0.6	V
A_nt	0.6	V

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	0 3.8206e-04 9.5909e-05]	
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	407	mm
z_bp (NEXT)	407	mm
z_bp (FEXT)	407	mm
z_bp (RX)	407	mm
C_0	0	nF
C_1	0	nF
Include PCB	0	logical

- ERL22 for **TX ERL**