802.3ck D1.4
Annex 162B – Test Fixtures
RL, ERL and FOM_{ILD} Comments

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Purpose

- Mated Test Fixture RL, ERL and FOM_{ILD} comments.
  - RL Comment #114
    - Remove the mask from the spec
  - ERL comments #112, #105 , #106, #8, and #131
    - > Comment #112 proposes 10 dB
    - > Comment #105, 98#, and #106 propose 9 dB
    - > Comment #8 proposes 14 dB,
    - > Comment #131 proposes 10.3 dB
    - > Comment #42 requests a value
    - > Update PICs.
  - FOM_{ILD} comments #111, #97, #104 and #107
    - > Comments 111, 97 and 104, propose 0.18 dB
    - > Comment 107 proposes 0.18 dB with Tr=9.6 ps
    - > Comment 130 proposes deletion
    - > Comment #41 requests a value
    - > Update PICS if specification is not deleted

Supporters

- Rich Mellitz, Samtec
- Samuel Kocsis, Amphenol
- Adee Ran, Intel
- Yasuo Hidaka

Proposal MTF RL

- **MTF RL Comment #114**
  - **Remove the mask from the spec**
  - **Delete 162B.1.3.3 Mated test fixtures differential return loss**
- **Rationale: With the adoption of a normative return loss requirement (ERL) maintaining information that may not be correlate to the requirement is not meaningful.**

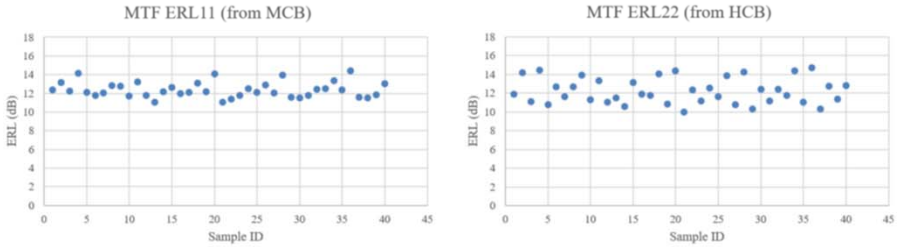
Proposal Mated Test Fixture ERL

- **162B.1.3.2 Mated test fixtures effective return loss (ERL) - P262, L43, TBD = 10.3**
- **162B.1.3.2 Mated test fixtures effective return loss (ERL)**

The values of the mated test fixtures ERL are computed using the procedure in 93A.5 with the parameter values in Table 162B-1 . Parameters that do not appear in Table 162B-1 take values from Table 162–18.

The mated test fixture ERL shall be greater than or equal to TBD dB.

MTF ERL
Updated QSFP-DD800 Data



- 40 new data points collected using are QSFP-DD800, with fixtures that implement the latest MSA changes
- All data points meet previous proposal of 8dB for MTF ERL and would also meet a 9dB requirement
  - [9.8dB , 14.7dB]

Table 162B–1—Mated test fixture ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.01	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	400	UI
Equalizer length associated with reflection signal	N_{bx}	0	UI
Time-gated propagation delay	T_{fx}	0	ns
Tukey window flag	tw	1	—
Target detector error ratio	DER_0	10^{-5}	—

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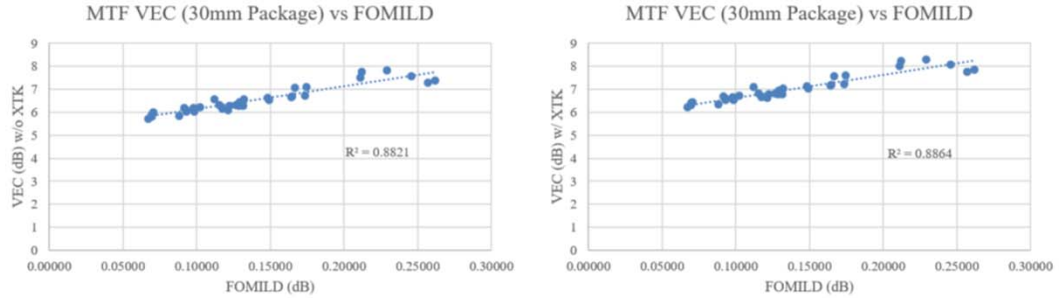
https://www.ieee802.org/3/ck/public/adhoc/jan13_21/kocsis_3ck_adhoc_01_011321.pdf

Proposal Mated Test Fixture FOM_{ILD}

- **162B.1.3.1 – P262, L36, TBD = 0.18, Tr=9.6 ps**
- **Update PICs.**

The FOM_{ILD} is calculated according to 93A.4 with f_b=53.125 GHz, T_t=7.5 ps, and f_r=0.75 × f_b. The fitted insertion loss and insertion loss deviation are computed over the range f_{min}=0.05 GHz to f_{max}=40 GHz. FOM_{ILD} shall be less than (TBD) dB.

MTF FOMILD Requirement
Replacing the TBD



- Adding maximum crosstalk to the MTF results in ~ +0.5dB VEC
- VEC and FOMILD are well correlated and VEC<7.5dB results in and FOMILD<0.187dB
- Recommend setting the MTF FOMILD requirement to 0.18dB for D1p5 release
  - Can be adjusted in future drafts if VEC requirements change or more MTF data becomes available

Slide 11 https://www.ieee802.org/3/ck/public/adhoc/jan13_21/kocsis_3ck_adhoc_01_011321.pdf

Proposal Mated Test Fixture FOM_{ILD}

93A.4 Insertion loss deviation

The insertion loss deviation $ILD(f)$ is the difference between the measured insertion loss $IL(f)$ and the fitted insertion loss $IL_{fitted}(f)$ (see 93A.3) as shown in Equation (93A–55).

$$ILD(f) = IL(f) - IL_{fitted}(f) \quad (93A–55)$$

A figure of merit for a channel that is based on $ILD(f)$ is given by Equation (93A–56). In Equation (93A–56), f_n are the frequencies considered in the computation of the fitted insertion loss and $W(f_n)$ is the weight at each frequency as defined by Equation (93A–57).

$$FOM_{ILD} = \left[\frac{1}{N}\sum_n W(f_n) ILD^2(f_n)\right]^{1/2} \quad (93A–56)$$

$$W(f_n) = \text{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_t)^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (93A–57)$$

The variable f_b is the signaling rate. The 3 dB transmit filter bandwidth f_t is inversely proportional to the 20% to 80% rise and fall time T_t. The constant of proportionality is 0.2365 (e.g., $T_t f_t = 0.2365$; with f_t in Hertz and T_t in seconds). The variable f_r is the 3 dB reference receiver bandwidth.

The values assigned to f_b, T_t, and f_r are defined by the Physical Layer specification that invokes this method.

110B.1.3.7 Mated test fixtures integrated near-end crosstalk noise

Given the disturber near-end crosstalk loss $NEXT_{loss}(f)$ measured over N uniformly spaced frequencies f_n spanning the frequency range 50 MHz to 19 000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated near-end crosstalk noise is determined using Equation (110B–1) and Equation (110B–2).

The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured disturber crosstalk transfer functions. The transmitter and receiver filters

are used in Equation (110B–1) to define a weighting function to the multiple-disturber crosstalk in Equation (110B–2). The sinc function is defined by $\text{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (110B–1).

$$W_{nt}(f_n) = (A_{nt}^2/f_b)\text{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{nt})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (110B–1)$$

where the equation parameters are given in Table 110B–2.

Note that the 3 dB transmit filter bandwidth f_{nt} is inversely proportional to the 20% to 80% rise and fall time T_{nt}. The constant of proportionality is 0.2365 (e.g., $T_{nt} f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 18.75 GHz.

The integrated near-end crosstalk noise σ_{nx} is calculated using Equation (110B–2).

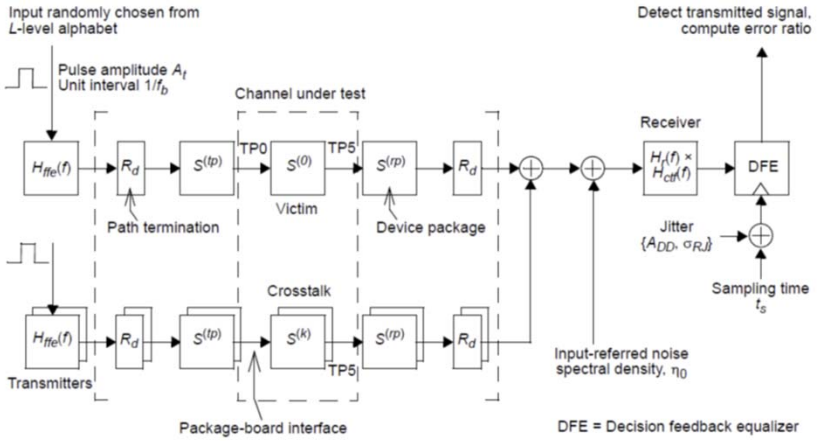
$$\sigma_{nx} = \left[2\Delta f \sum_n W_{nt}(f_n) 10^{-NEXT_{loss}(f_n)/10}\right]^{1/2} \quad (110B–2)$$

where Δf is the uniform frequency step of f_n.

The total integrated near-end crosstalk noise for the mated test fixture is computed using the parameters shown in Table 110B–2.

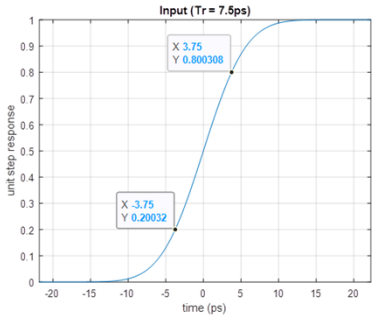
Proposal Mated Test Fixture FOM_{ILD}

- 162B.1.3.1 – P262, L36, TBD = 0.18 dB, Tr=9.6 ps
- Update PICs.

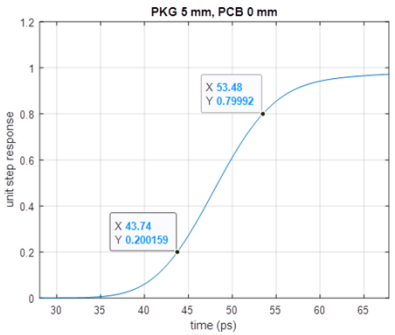


Tr COM = 7.5 ps

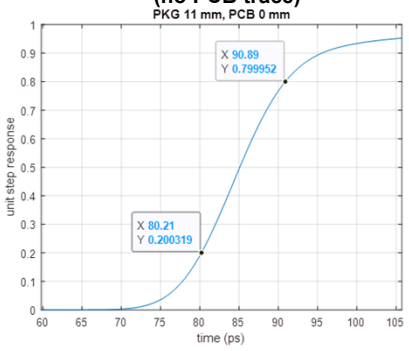
7.5ps input step (Gaussian input pulse)



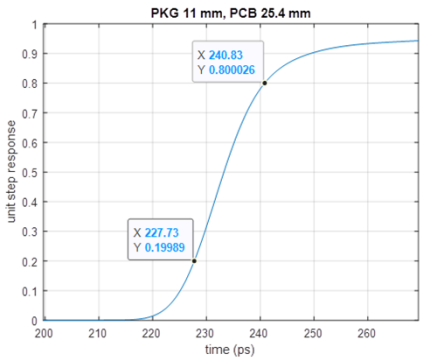
9.74ps after 5mm PKG trace (*no* PCB trace)



10.68ps after 11mm PKG trace (no PCB trace)



13.10ps after 11mm PKG trace and 25.4mm PCB trace



Analysis contributed by Yasuo Hidaka: Using COM device and PKG/PCB model parameters in P802.3ck D1.4.

Supplemental

Adee's comment#131

"The mated test fixture ERL shall be greater than or equal to TBD dB"

We have adopted a minimum of 7.3 dB for a host ERL in Table 162–10 (with parameters in 162.9.3.5). The parameters for MTF are the same, except that "Time-gated propagation delay" is 0 instead of 0.2 ns.

The value 0 was accepted explicitly (comment #122 against D1.3) but the differnece does not seem to be justified, since the MTF includes the test fixture used for host ERL measurement (where the connector is time gated). Different time gating creates difference in the meaning of ERL.

The ERL from a high-quality MTF is the upper bound for any measurement of a DUT which uses any one of the test fixtures. Therefore, it should be significantly higher than 7.3 dB.

It is suggested to divide the budget evenly to allow about the same reflection power from the DUT's internal circuitry as from the mated connectors; if each one is 10.3 dB then their combination (RSS, since reflections are independently distributed) would be 7.3 dB.

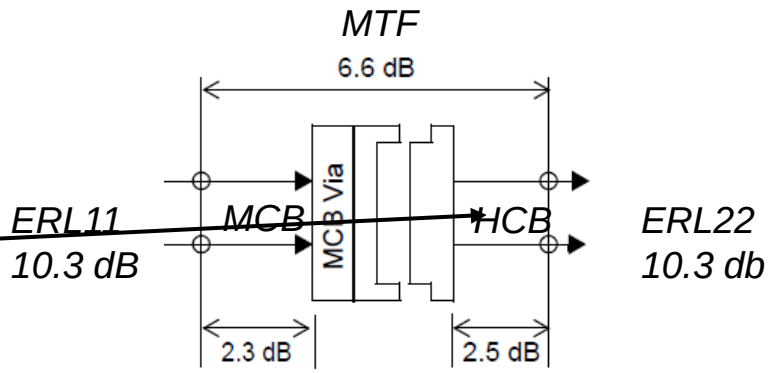
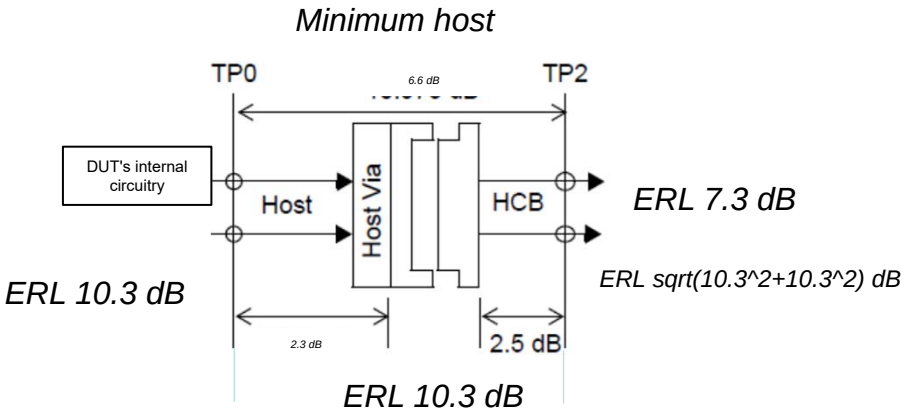


Table 162–10—Summary of transmitter specifications at TP2

Effective return loss, ERL (min)	162.9.3.5	7.3	dB



Test fixture definitions:
MTF = mated test fixture
HCB = host compliance board
MCB = module compliance board

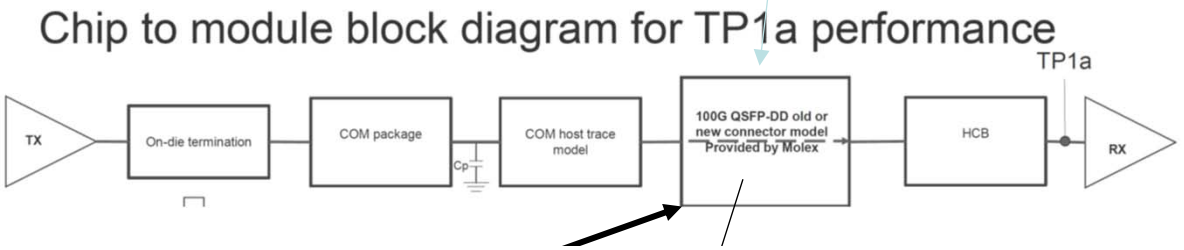
Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance PCBs with allowances for ball grid array (BGA) footprint and host connector footprints is 6.875 dB at 26.56 GHz and the recommended minimum insertion loss allocation for the transmitter or receiver differential controlled impedance PCBs is 2.3 dB at 26.56 GHz.

Mike's comment#8

The ERL of the mated test fixture should be significantly better than the specification for the ERL of the device under test. The ERL of the QSFP-DD improved connector used for channel modeling in e.g Didel_3ck_01_0320. has an ERL of 15.7 dB.

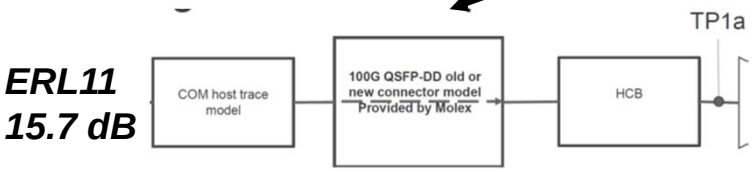
Request MTF ERL of *14* dB

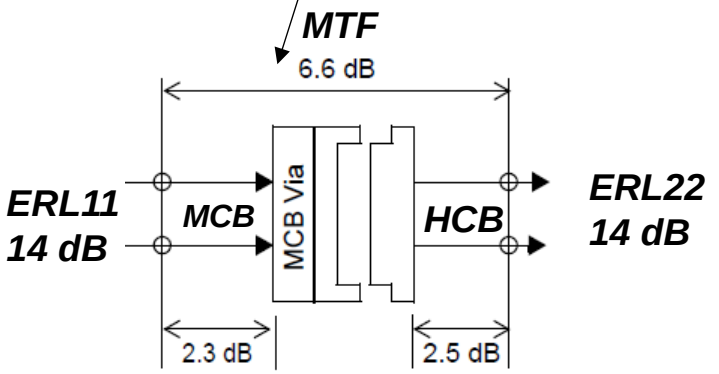
ERL new connector model of 15.7 dB.



dudek_3ck_01_0320.pdf

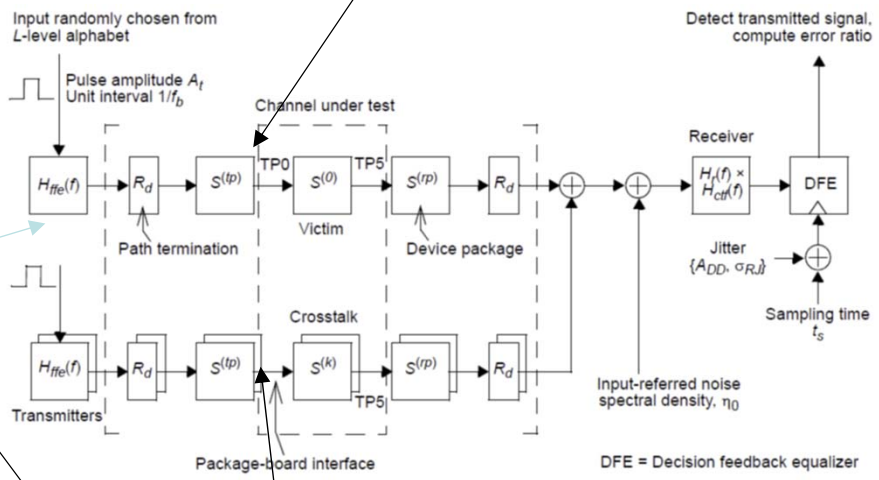
Test fixture definitions:
MTF = mated test fixture
HCB = host compliance board
MCB = module compliance board





Rise time

Tr FOM$_{ILD}$



Tr COM = 7.5 ps

Tr ICN

Proposal

Tr is faster than Tr FOM$_{ILD}$ and Tr ICN

Tr = 7.5ps

Tr FOM$_{ILD}$ and Tr ICN = 9.6 ps

162.11.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 162.11.7.1 and the procedure in 93A.1, where T_r is 7.5 ps for $H_r(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 162D), as described in 162.11.7.2.

$$H_r(f) = \exp(-(\pi f T_r / 1.6832)^2) \qquad (93A–46)$$

94.3.12.1 Test fixture

The test fixture of Figure 94–10 or its equivalent is required for measuring the transmitter specifications described in 94.3.12.

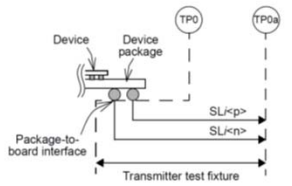
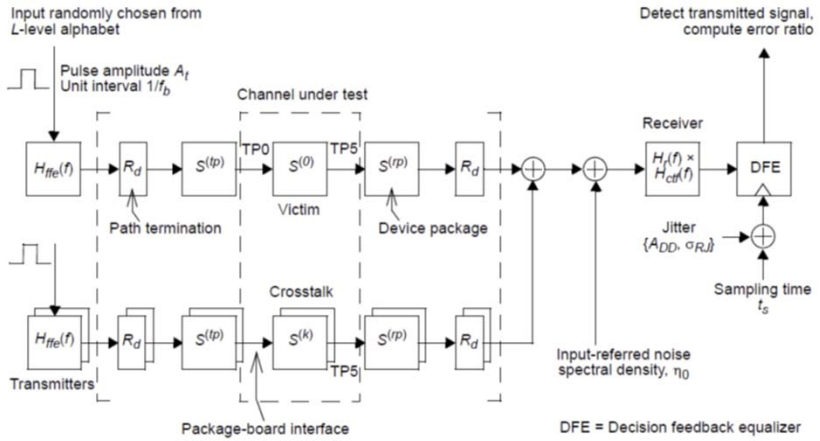


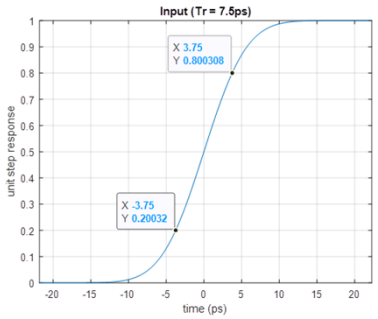
Figure 94–10—Transmitter test fixture and test points

Rise time

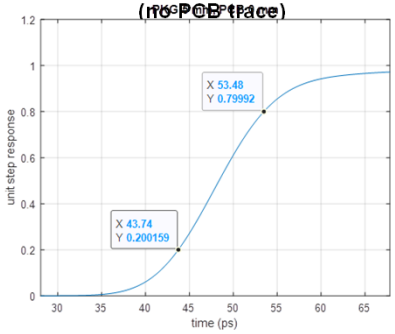
Tr COM = 7.5 ps



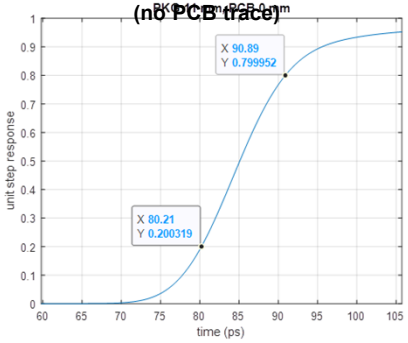
7.5ps input step (Gaussian input pulse)



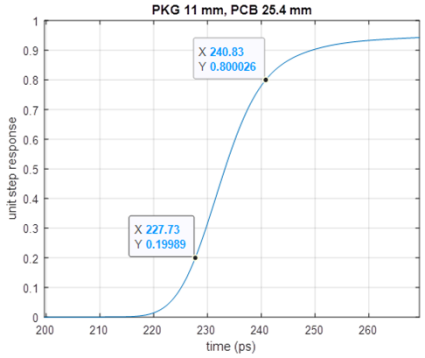
9.74ps after 5mm PKG trace (no PCB trace)



10.68ps after 11mm PKG trace (no PCB trace)



13.10ps after 11mm PKG trace and 25.4mm PCB trace



Analysis contributed by Yasuo Hidaka: Using COM device and PKG/PCB model parameters in P802.3ck D1.4.

Rise time

Rise time – 12G.3.1.4 supplemental

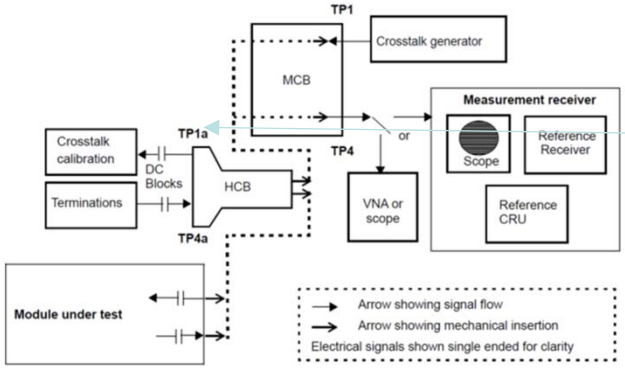


Figure 120G–7—Example module output test configuration

Table 120G–1—Host output characteristics at TP1a

Transition time (min, 20% to 80%)	120G.3.1.4	7.5	ps

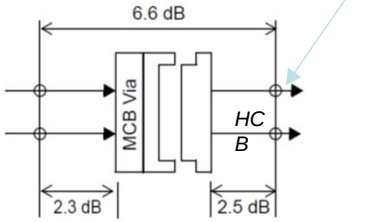


Table 120G–3—Module output characteristics (at TP4)

Transition time (min, 20% to 80%)	120G.3.1.4	7.5	ps

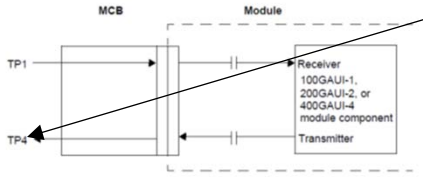


Figure 120G–4—Module compliance points

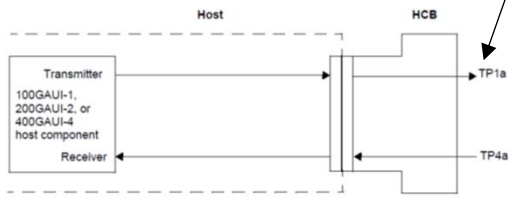


Figure 120G–3—Host compliance points