Clause 163/163B Comment Resolution

Phil Sun

Credo Semiconductor

Comments Overview

Clause	Topic	Comments	Notes
163,	RX RLCD	[121, 26]	
163	Channel ILCD	[122, 27]	
163/120F	Channel RLCD (CC)	139	
163	Channel IL	144	
163B	TP0v/TP5v example	[132, 44, 45], 82	

Comment [121, 26]: RX RLCD

Cl **163** *SC* **163.9.3** *P* **187** *L* **41** # 121

Ran, Adee Intel

Comment Type **TR** *Comment Status* **D** *RX RLCD*

(addressing TBD)
Rx Differential to common-mode (conversion) input return loss refers to 93.8.1.4 with value TBD. This subclause uses equation (93-5) to define the limit.

The conversion loss specifications may need more work, but for the purpose of technical completeness, it is suggested to use a piecewise-linear equation similar to (93-5).
Boundary lines are suggested to match the ones used in OIF CEI-112G-LR for the 53.125 GHz signaling frequency.

As an alternative consider removing this specification (the Rx owns its performance).

SuggestedRemedy

Add a new subclause for Rx differential to common mode return loss with the equation:

RLdc(f) ≥ 25-20*(f/fb) for 0.05 ≤ f ≤ fb/2
RLdc(f) ≥ 15 for fb/2 < f ≤ 40
where f is the frequency in GHz and fb=53.125.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Add a new subclause for RLCD
RLcd(f) = 25-20*(f/fb) for 0.05 <= f <= fb/2
RLcd(f) = 15 for fb/2 < f <= 40
where f is the frequency in GHz and fb=53.125.
Update PICS
Implement with editorial license.

Cl **163** *SC* **163.9.3** *P* **187** *L* **41** # 26

Brown, Matt Huawei

Comment Type **T** *Comment Status* **D** *RX RLCD*

In Table 163-8, the specified value for receiver differential to common-mode return loss is TBD

SuggestedRemedy

Provide a value or equation and update PICS.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using response to comment #121

Table 163–8—Summary of receiver specifications at TP5v

Parameter	Reference	Value	Units
Difference effective return loss, *dERL* (min)	163.9.3.2	-3	dB
Differential to common-mode input return loss	93.8.1.4	TBD	dB
Interference tolerance	163.9.3.3	Table 163–9	—
Jitter tolerance	163.9.3.4	Table 162–15	—

Comment [122, 27]: channel ILCD

Cl **163** *SC* **163.10.4** *P* **192** *L* **44** # 122

Ran, Adee Intel

Comment Type **TR** *Comment Status* **D** *channel ILDC*

(addressing TBD)
For the KR PHY, the channel "differential to common-mode conversion loss of TP0 and TP5" is TBD.

For the CR PHY this parameter is specified in 162.11.5 as "The difference between the cable assembly differential to common-mode conversion loss and the cable assembly insertion loss" with equation (162-10).

For the purpose of technical completeness, a similar equation can be used for KR.

SuggestedRemedy

Rewrite this subclause based on 162.11.5, substituting "TP0 to TP5 channel" for "cable assembly" with editorial license.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **163** *SC* **163.10.4** *P* **192** *L* **44** # 27

Brown, Matt Huawei

Comment Type **T** *Comment Status* **D** *channel ILDC*

The specified value for channel differential to common-mode conversion loss is TBD.

SuggestedRemedy

Provide a value or equation and update PICS.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #122

163.10.4 Channel differential to common-mode conversion loss

The differential to common-mode conversion loss of TP0 and TP5 shall meet the requirement of TBD.

162.11.5 Differential to common-mode conversion loss

The difference between the ~~cable assembly~~ differential to common-mode conversion loss and the cable assembly insertion loss shall meet Equation (162–10) illustrated in Figure 162–6.

$$Conversion\_loss(f) - IL(f) \geq \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases} \quad (162\text{–}10)$$

where

$Conversion\_loss(f)$	is the cable assembly differential to common-mode conversion loss at frequency f in dB
$IL(f)$	is the cable assembly insertion loss at frequency f in dB
f	is the frequency in GHz

Comment [139]: channel RLCD

Cl **163** *SC* **163.10** *P* **190** *L* **28** # 139

Ran, Adee Intel

Comment Type **T** *Comment Status* **D** *channel RLCD (CC)*

There is no specification for RLDC for the KR channel.

Without such specification, a channel can cause a strong common mode reflection signal that will be fed into the Tx - and since Tx RLCD/RLCC are not defined either, a differential or common mode signal can be reflected back without control.

The conversion loss specifications may need more work, but for the purpose of technical completeness, the channel RLDC from 162.11.4 can be used.

Also in missing 120F.

SuggestedRemedy

Add a new subclause for channel differential to common mode return loss, based on 162.11.4 with the same limits, with editorial license.

Apply similarly in 120F.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy.
For task force discussion.
[Editor's note: CC 163, 120F]

162.11.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet Equation (162–9).

$$Return\_loss(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases} \quad (162\text{–}9)$$

where

Return_Loss(f) is the cable assembly differential to common-mode return loss at frequency *f* in dB

f is the frequency in GHz

The cable assembly differential to common-mode return loss is illustrated in Figure 162–5.

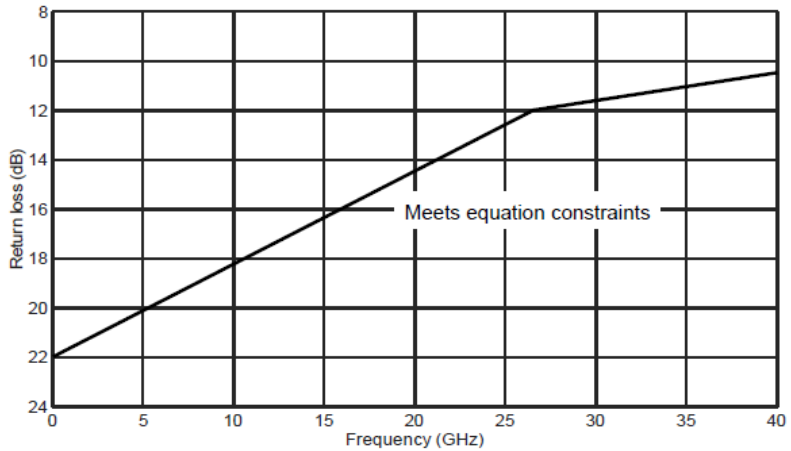

Figure 162–5—Differential to common-mode cable assembly return loss

Comment [144]: channel IL curve

Cl **163** *SC* **163.10.2** *P* **192** *L* **28** # 144

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *channel IL*

The limit at 40 GHz (not 45 as in the figure) excludes some acceptable channels.

SuggestedRemedy

Replace the straight part of the limit with one that curves down. (with an f^2 term). Correct the fmax in Figure 163-5.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The was an error in creating the figure that should be corrected.
Change figure 163-5 so curve ends at 40 GHz to match the equation.
The suggested remedy has not provided sufficient details to change the insertion loss curve. Also, the change is not required for technical completeness.

163.10.2 Channel insertion loss

The maximum recommended insertion loss of the channel is given by Equation (163–3).

$$IL(f) \le \begin{cases} 0.693 + 2.161\sqrt{f} + 0.607f & 0.01 \le f \le 26.5625 \\ -19.12 + 1.773f & 26.5625 < f \le 40 \end{cases} \quad (163\text{–}3)$$

where

$IL(f)$ is the insertion loss in dB at frequency f
f is the frequency in GHz

The insertion loss limit is illustrated by Figure 163–5.

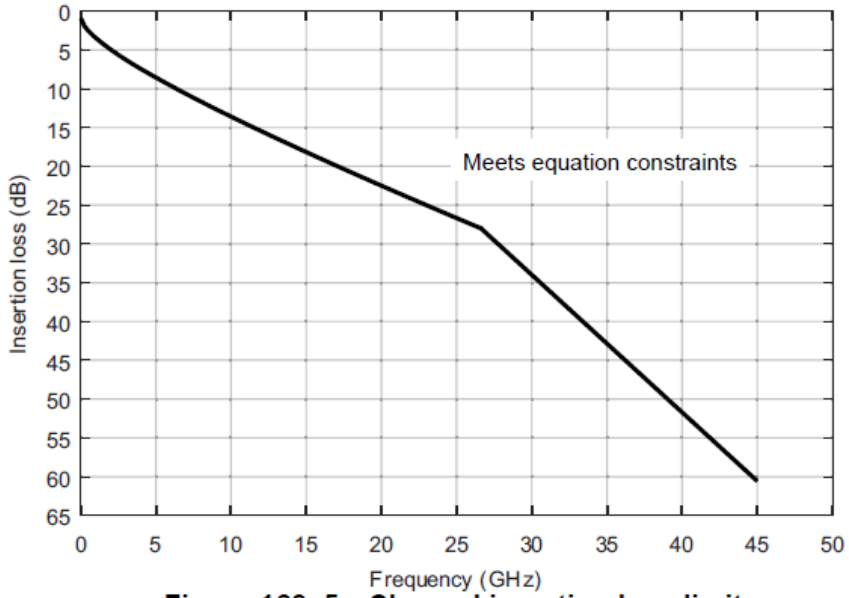

Figure 163–5—Channel insertion loss limit

Comment [132, 44, 45]: TP0v test fixture model

Cl **163B** *SC* **163B.2** *P* **290** *L* **16** # 132

Ran, Adee Intel

Comment Type **TR** *Comment Status* **D** *TP0v/TP5v example*

(addressing TBD)
The example test fixture is defined only by the magnitude of its insertion loss. Therefore it is impossible for a reader to calculate reference values at TP0a, and this example does not help.

The lack of full channel information also prevents calculation of consensus values to replace the TBDs in Table 163B–1.

It is suggested to replace the definition to a full s-parameters model based on the equations in 162.11.7.1.1 with the same z_p, creating an IL of 4.33 dB at 26.56 GHz. This will enable calculation of the reference values.

Alternatively, use a smaller value for z_p to create an IL of 2.8 dB.

SuggestedRemedy

Replace the text of this paragraph with text referring to 162.11.7.1.1 and equation 162-12 and update the reference values (currently TBD) accordingly.

A presentation with a more detailed proposal is planned.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
This comment proposes a technical change to the draft that does not address technical completeness.
Although this Annex is informative, this subclause is incomplete as written.
Phase information is missing for the existing test fixture specification. The suggested remedy does not provide sufficient details for implementation.
However, the comment mentions that a presentation may be provided.

162.11.7.1.1 Channel signal path

The scattering parameters of the channel signal path from TP0 to TP5 are calculated using Equation (162–14). The transmitter and receiver PCB signal paths are denoted as $S^{(HOSPT)}$ and $S^{(HOSPR)}$, and are calculated using Equation (162–12) and Equation (162–13), respectively. The PCB transmission line scattering parameters are denoted as $S^{(l)}$ and are calculated from Equation (93A–13) and Equation (93A–14) using z_p = 110.3 mm in length and the parameter values given in Table 162–19, representing an insertion loss of 4.33 dB at 26.56 GHz on each PCB. The scattering parameters for the PCB via capacitances, $S^{(c0)}$ and $S^{(c1)}$, are calculated using Equation (93A–8) and the values in Table 162–19.

$$S^{(HOSPT)} = \text{cascade}(S^{(c0)}, S^{(l)}, S^{(c1)}) \quad (162\text{–}12)$$

$$S^{(HOSPR)} = \text{cascade}(S^{(c1)}, S^{(l)}, S^{(c0)}) \quad (162\text{–}13)$$

$$SCHS_p^{(k)} = \text{cascade}(S^{(HOSPT)}, S^{(CASP)}, S^{(HOSPR)}) \quad (162\text{–}14)$$

where

$SCHS_p^{(k)}$	is the channel signal path
$S^{(HOSPT)}$	is the host transmitter PCB signal path
$S^{(HOSPR)}$	is the host receiver PCB signal path
$S^{(CASP)}$	is the cable assembly signal path (TP1 to TP4)
k	is equal to zero

Comment [132, 44, 45]: TP0v test fixture model

Cl **163B** *SC* **163B.2** *P* **291** *L* **18** # 44

Brown, Matt — Huawei

Comment Type **T** *Comment Status* **D** *TP0v/TP5v example*

For the example test fixture, the reference value in Table 163B-1 for transmitter steady-state voltage is TBD.

SuggestedRemedy

Provide a value.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
This comment proposes a technical change to the draft that does not address technical completeness.
Resolve using the response to comment #132.

Cl **163B** *SC* **163B.2** *P* **291** *L* **20** # 45

Brown, Matt — Huawei

Comment Type **T** *Comment Status* **D** *TP0v/TP5v example*

For the example test fixture, the reference value for transmitter linear fit pulse peak voltage is TBD.

SuggestedRemedy

Provide a value.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
This comment proposes a technical change to the draft that does not address technical completeness.
Resolve using the response to comment #132.

Table 163B–1—Summary of transmitter reference values at TP0a

Parameter	Reference	Value	Units
Effective return loss, ERL	163.9.2.3	15.5	dB
Transmitter steady-state voltage, v_f	162.9.3.1.2	TBD	V
Transmitter linear fit pulse peak, v_{peak}	162.9.3.1.2	TBD	V

Comment [82]: TP0v test fixture model

Cl **163B** *SC* **163B.2** *P* **290** *L* **23** # 82

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type **TR** *Comment Status* **D** *TP0v/TP5v example*

Example TP0V should be better defined

SuggestedRemedy

See ghiasi_3ck_02_0121
The DUT trace is constructed from 2 mm section of PCB trace with 102 Ohms (via model), followed by 66.8 mm 92.5 Ohms strip line, followed by 2 mm section of PCB trace with 102 ohms (via model) the total loss of this model at 26.55 GHz is 2.8 dB. The PCB model is per table 93-12. The equation for the loss =0.006+0.25*SQRT(f)+0.057*f, where f is in GHz.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
This comment proposes a technical change to the draft that does not address technical completeness.
This suggested remedy provides more accurate IL than equation 163B-1. Phase information is still missing for the test fixture.
Pending review of the following presentation and task force review.
https://www.ieee802.org/3/ck/public/21_01/ghiasi_3ck_02_0121.pdf
Resolve with comment #132.

$$IL(f) = 0.074 + 0.2104\sqrt{f} + 0.0674f \qquad 0.05 \le f \le 53.125 \qquad \text{(163B–1)}$$