Package to Board Linkage capacitance – Cp Extraction/Simulation Follow-up

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Package to board linkage “Ball area” capacitance

Extraction/Simulation follow-up

Reminder – Recap / Main points:

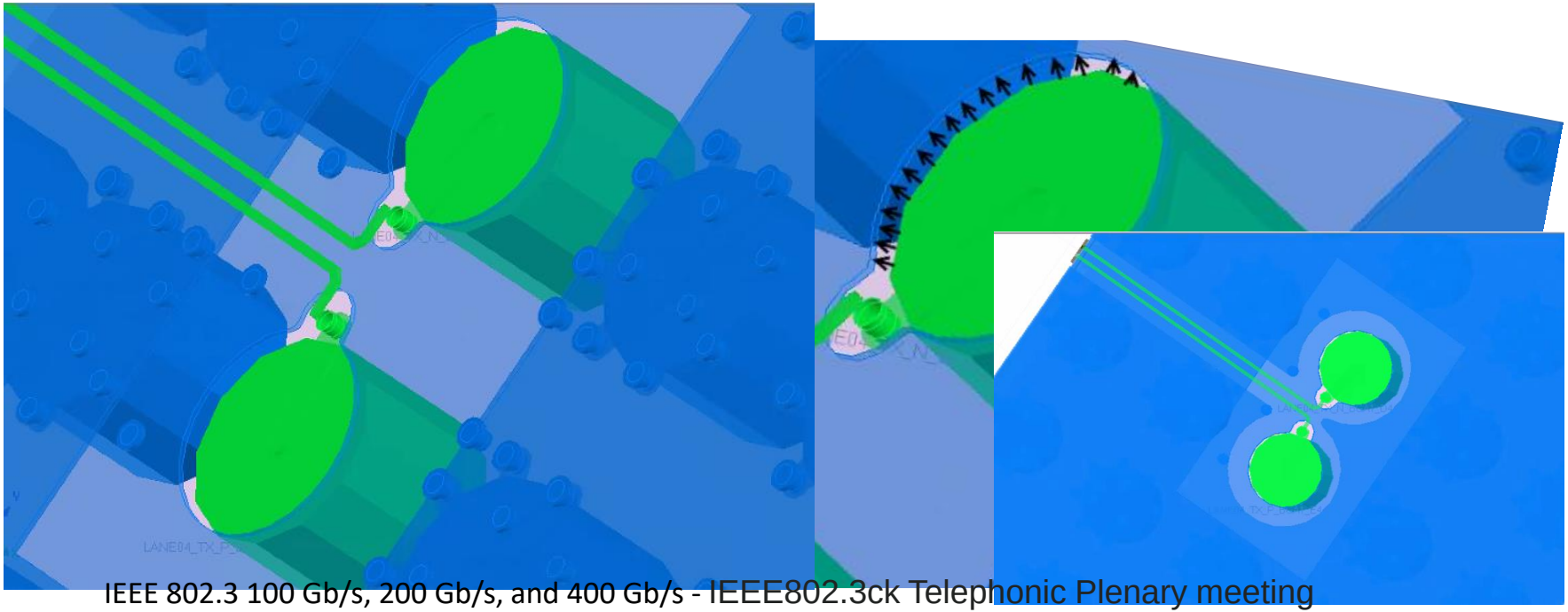
- Ad hoc slides (integrated from slide 8 and on as a reminder) claimed:
  - The appropriate manner to evaluate Cp is by looking at its reflective effect, rather than calculate the capacitance of the mechanical structure –
  - A short background recap of the methodology originally used to corelate the package model effect and with it the ball discontinuity effect will also be presented for further emphasis

- The impedance drop due to 87fF Cp is reasonable, while driving a whole package by a 7.5psec t_r TDR – Will be further emphasized by correlating a ball extraction (with as little a package as possible) by itself

Extraction/Simulation follow-up

Ball Fringing Capacitance Effect

- What would be the effective capacitive reflective effect of a ball (after assembly) (in Green) with the exact same size void (No overlap) formed on the GND (blue) layer 30µ above it?

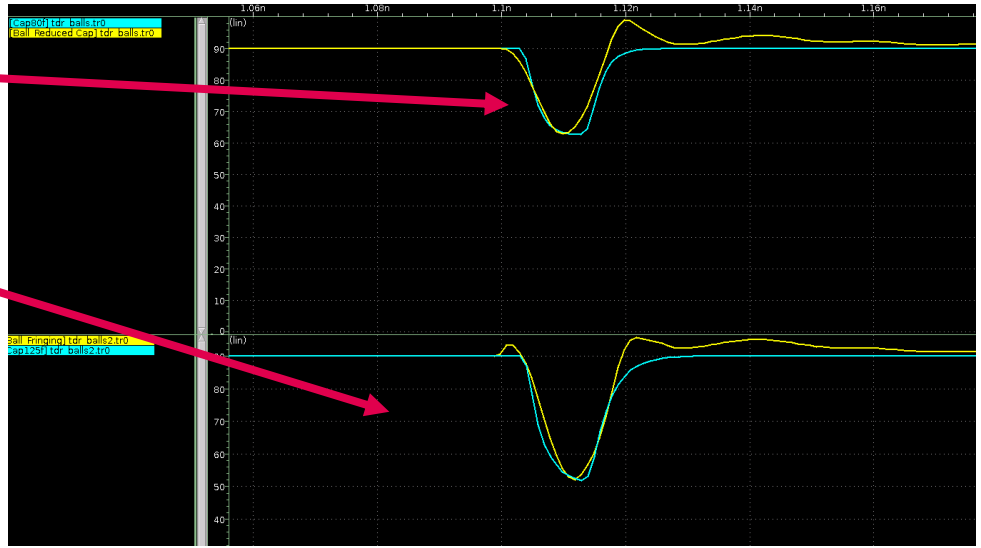


Package to board linkage “Ball area” capacitance

Extraction/Simulation follow-up

Follow-up – TDR of a ball by itself

- Effective capacitance of a ball while utilizing methodologies to lower ball area capacitance ≈ 80fF prior to manufacturing tolerances – Correlates to 802.3ck Cp
- Fringing effect of a ball with the exact same diameter void placed above it ≈ 125fF - Correlates to Cp of 802.3bj



Extraction/Simulation follow-up

Extraction / Simulation Follow-up Summary

- The fringing capacitance by itself correlates to 802.3bj Cp value
- Some valid packaging applications may require mechanical implications on ball area which are likely to be translated to higher capacitance
- Methods were used to lower ball-area capacitance and the discontinuity of the resulting structure was correlated to 80fF (before applying manufacturing tolerance)
- We have verified that former values of Cp indeed corelate to as basic as possible models

➔Cp value of 87fF is reasonable and should not be changed

Background – Package Synthesis Model Process Overview

Steps: 1, 2, 3	Step: 4	Step: 5	Step: 6	Step 7	Step 8
"Original" S4P Model	**TDR, PTDR, IL, RL, PR Plots**	**First draft" synthesized" circuit model**	**Identity delay, loss, and Z_0 T-line segments**	**Adjust T-line and circuit parameters for good TDR, PTDR, , IL and RL**	**Compare with COM**

1. Start from measured or simulated multiport s-parameter not including the die load
   - One set of ports will be the die connect to the package referenced to die reference plane
   - The other side will be the BGA (if applicable) ball with port referenced to the PCB or carrier's reference plane
   - Must have sufficient bandwidth, causality, passivity, and stability for time domain analysis at the prescribed baud rate.
2. Identify a die circuit model to use for synthesis.
3. Identify then extract a 4 port victim set of s-parameters
4. Acquire IL and RL vs Frequency plots, Pulse response (PR) plots, TDR plots PTDR plots
5. Estimate an target for the synthesized circuit.
   - TDR plots
   - This step requires some engineering experience a judgement
6. Identify transmission line segments and make estimates for loss, delay and Z_0.
7. Iterate through comparison between the synthesis models and the original s-parameter model
   - Adjust circuit and T-line parameter to get a acceptable overlays of the pulse response, TDR, PTDR, IL and RL
8. Finally use both models to do COM simulations
   - If results are close enough, say 0.05 dB you are done

Thank You!

Agenda

January 2021 Ad Hoc Slides here-on

1. Package imperfections and inclusion in the reference model
2. Package to board linkage “Ball area” capacitance
3. Cp TDR Results
4. Summary

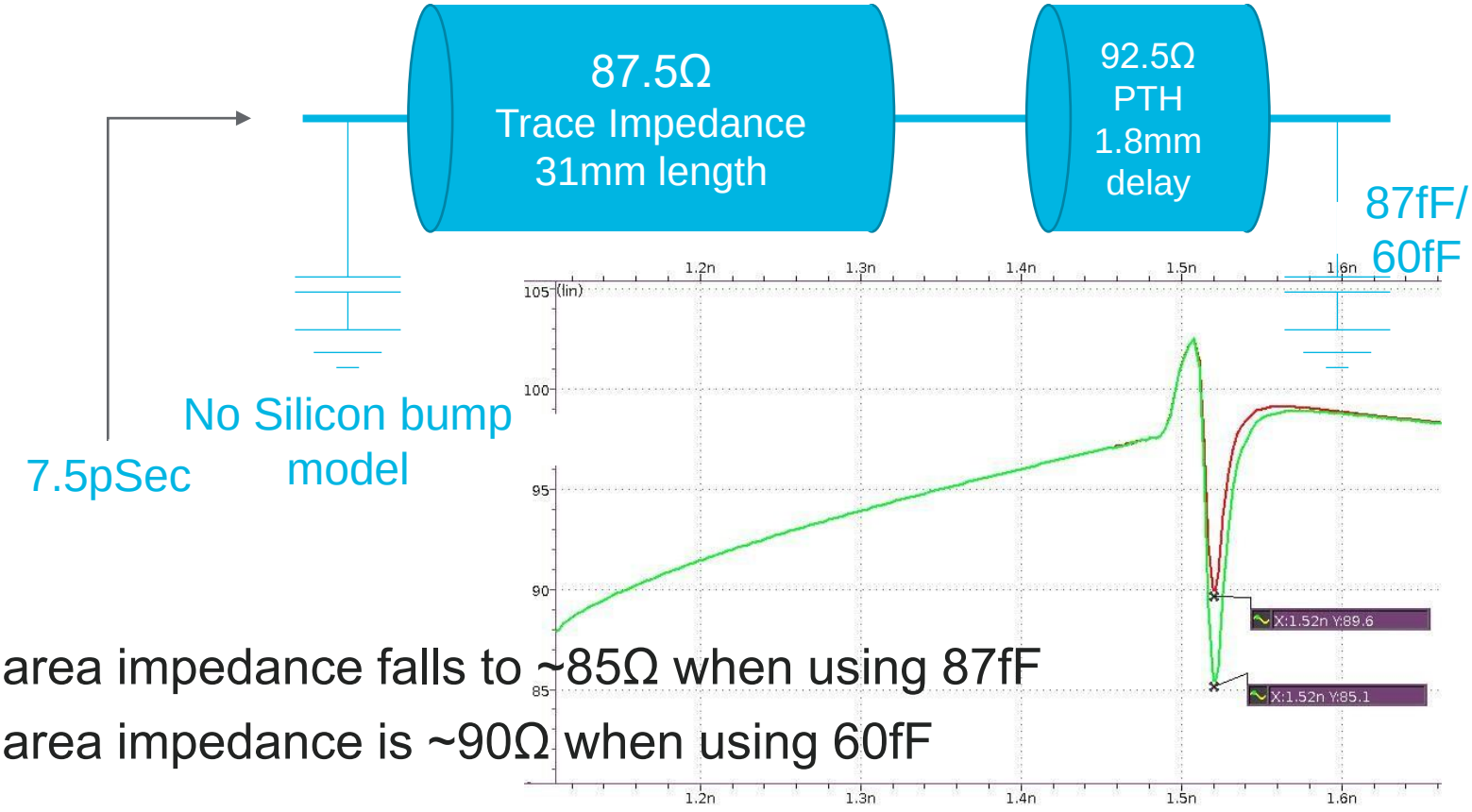
Package imperfections and inclusion in the reference model

- Loss – Included, may fall short of max, or long of min loss
- Length – Two reference lengths – may fall short of max, or long of min length, may not introduce worst re-reflections given specific interconnects
- Bump area discontinuity – model included to represent silicon “T-Coil” and bump discontinuity
- Trace + PTH impedances – Models are included to represent impedances of the trace and the PTH with delay relative length – Manufacturing tolerances are not represented and package vias were optimized to bring best COM result, one PTH location close to the ball
- Package cross lane Far-end/Near-end Crosstalk – Not included
- Ball-area discontinuity – Next Slide

Package to board linkage “Ball area” capacitance

- Device package including 100Gbps lanes vary in size and type
  - Various types and sizes can have different ball-area characteristic impedance discontinuity.
    - Implementation requirements vary, mechanical requirements vary, manufacturing tolerance vary
- Package to board linkage capacitance is used to emulate reference package ball area discontinuity and is called Cp
  - A more complicated model was avoided thanks to ball-area dimensions relative to wavelength. For better accuracy can increase complexity – no need
  - Correlation to extractions (No board pad – coax port on ball) was provided in https://www.ieee802.org/3/ck/public/19_01/benartsi_3ck_01_0119.pdf
- The usage of Cp is in the time domain in COM and TP0v simulations
  - Discontinuity in time domain is best estimated by time domain reflectometry

Cp TDR using COM rise-time (7.5psec)



- Ball area impedance falls to ~85Ω when using 87fF
- Ball area impedance is ~90Ω when using 60fF

Summary

- The reference package model does not incorporate multiple manufacturing related and design related items – 3dB COM
- Loss and reflections are a major contributor to the reference package model imperfections
- The reference package model is used for simulation in the time-domain, thus one should look at its effect in time domain reflectometry
- It was demonstrated that 87fF introduce a reasonable discontinuity – not best case, for sure not worst case

Thank you!