Annex 120G (C2M) Comment Resolution

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IEEE P802.3ck Task Force
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EH/VEC Method
Comment 47

Cl 120G SC 120G.5.2 P 253 L 27 # 47

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR *Comment Status* D *EH/VEC method*

The new C2M test procedure no longer require eye opening measurement with introduction of timing window tx=+/- 50 mUI, given the amount f change it will be very confusing for the reader to follow the procedure!

SuggestedRemedy

Please include a figure and full procedure in CL120G instead of referencing 120E

Proposed Response *Response Status* W

PROPOSED REJECT.
The methodology in this subclause leverages the methodology already documented in 802.3-2018 Annex 120E. There are only a small number of clear exceptions. Replicating the entire methodology is not warranted. Also, it is helpful to refer to existing test methodology familiar to test implementers. The relationship between TCmid (in Figure 120E-13) and Ts can be easily inferred from the exception {the CDF of the signal voltage is accumulated over the time interval ts ± 0.05 UI instead of "within 0.025 UI of time TCmid}.

g) Compute an eye diagram from $y_{Tx}(k)$, including the effect of Gaussian noise with variance calculated in the previous step, but taking into account that some noise from the measurement instrument is already in $y_{Tx}(k)$.

h) Compute Vmid, Vupp, Vlow, VCmid, VCupp, VClow from the eye diagram using 120E.4.2 steps 4) through 6) with the exception that the CDF of the signal voltage is accumulated over the time interval t_5 ± 0.05 UI instead of "within 0.025 UI of time TCmid".

i) The eye height is the minimum of Vmid, Vupp, and Vlow.

j) Compute the vertical eye closure using Equation (120E–4) and the values computed in step h) with the exception that VM3, VM2, VM1, and VM0 are the average values over the time interval t_5 ± 0.05 UI instead of "within 0.025 UI of time TCmid".

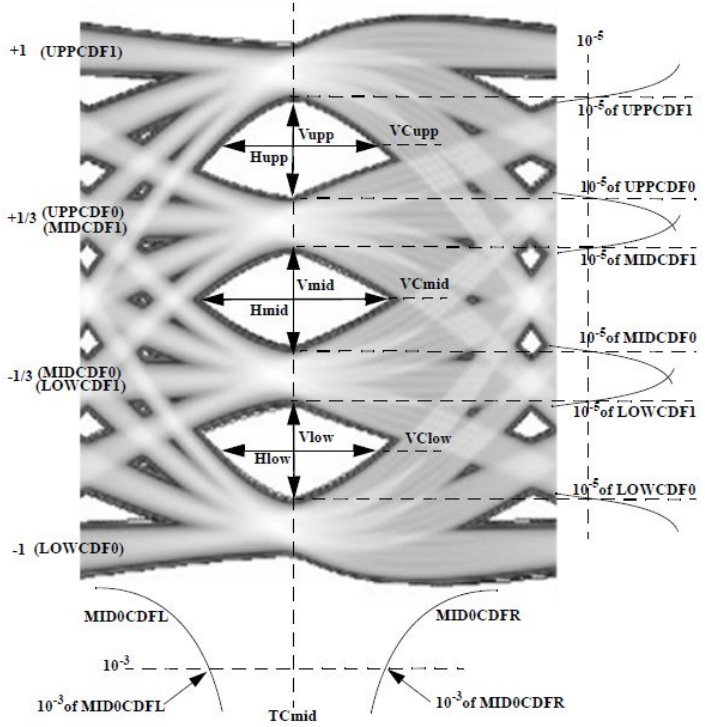


Figure 120E–13—PAM4 eye measurements

EH/VEC Method
Comment 180

Cl 120G	SC 120G.5.2	P 253	L 23	# 180

Dawe, Piers — Nvidia

Comment Type TR *Comment Status* D *EH/VEC method*

This draft has a primitive rectangular eye mask (H = either EHmin or EA/VECmax), although it is described as a histogram. It's an inefficient/inaccurate way of measuring a signal quality vertically and provides weak and uncertain protection against too much jitter. This is worse with the higher VEC limit in the latest draft that allows worse and more varied signals, and is a particular concern for very short host channels (see Mike Dudek's work) that can have faster edges than higher loss ones.

SuggestedRemedy

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = k +/-H/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-1/16, ts+/-3/32, V = k +/-H/2, k +/-H*0.4, k. k is VCmid, VCupp or VClow.
In case it's not clear, H is either EHmin or Eye Amplitude * 10^(-VECmax/20).
This simple scalable method can remain as the EH and VEC limits are revised. Scopes have been measuring with 10-sided masks for many years, it's not more difficult than a rectangular mask.

Proposed Response *Response Status* W

PROPOSED REJECT.
The currently methodology was chosen over an eye mask method like that being proposed in this comment.
See slide 3 of the following presentation was reviewed by the task force:
https://www.ieee802.org/3/ck/public/21_01/brown_3ck_04_0121.pdf
The comment does not provide sufficient justification to support the proposed changes.

g) Compute an eye diagram from $y_{rx}(k)$, including the effect of Gaussian noise with variance calculated in the previous step, but taking into account that some noise from the measurement instrument is already in $y_{rx}(k)$.

h) Compute Vmid, Vupp, Vlow, VCmid, VCupp, VClow from the eye diagram using 120E.4.2 steps 4) through 6) with the exception that the CDF of the signal voltage is accumulated over the time interval $t_z \pm 0.05$ UI instead of "within 0.025 UI of time TCmid".

i) The eye height is the minimum of Vmid, Vupp, and Vlow.

j) Compute the vertical eye closure using Equation (120E–4) and the values computed in step h) with the exception that VM3, VM2, VM1, and VM0 are the average values over the time interval $t_z \pm 0.05$ UI instead of "within 0.025 UI of time TCmid".

Slide 4 in
https://www.ieee802.org/3/ck/public/21_01/brown_3ck_04_0121.pdf

Comments 154
Annex 120G EO Method

Cl 120G	SC 120G.5.2	P 246	L 23	# 154

Dawe, Piers — Nvidia

Comment Type TR *Comment Status* D *EO method*

Of all the options in dawe_3ck_01a_1020, this draft has the most primitive (rectangular eye mask) although it is described as a histogram. It's an inefficient/inaccurate way of measuring a signal and provides weak and uncertain protection against too much jitter. This will get worse if we relax the VEC limits, and is a particular concern for very short host channels (see Mike Dudek's work).

SuggestedRemedy

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = +/-Hmin/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-0.07, ts+/-0.1, V = +/-Hmin/2, +/-Hmin*0.4, +/-0.
(In case it's not clear, Hmin, already specified, is the greater of EH and Eye Amplitude - VEC. There will be discussion about changing those limits from other comments, but this is a simple scalable method that can remain as the EH and VEC limits are revised.)

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment proposes a technical change to the draft that does not address technical completeness.
The comment does not provide sufficient evidence to support the proposed changes.

Draft 1.4 fully specifies the eye height and vertical eye closure.
Supporting presentations for the current methodology show that necessary eye width is enforced by these specifications.
https://www.ieee802.org/3/ck/public/20_10/healey_3ck_01a_1020.pdf
https://www.ieee802.org/3/ck/public/20_10/healey_3ck_02_1020.pdf

Broad support for this methodology was demonstrated by D1.3 Straw Polls #9 and #12.
https://www.ieee802.org/3/ck/public/20_10/minutes_3ck_1020_final_unapproved.pdf

Straw Poll #9:
I support the EW/ESMW direction of (Chicago rules):
A: Keep ESMW and eye width
B: Replace EH, ESMW, and eye width with an eye mask as proposed in dawe_3ck_01_1020
C: Remove ESMW and eye width and redefine EH and VEC as proposed in healey_3ck_01a_1020
D: Remove ESMW and eye width and leave EH and VEC as is
Results: A: 9, B: 10, C: 24, D: 6

Straw Poll #12:
I would support replacing ESMW and EW with the following option from healey_3ck_02_1020
A. "Alt. 2" with TBD = 50 mUI
B. "Alt. 1" with TBD1 = 25 mUI and TBD2 = 25 mUI
C. "Alt. 1" with TBD1 = 50 mUI and TBD2 = 20 mUI
D. "Alt. 2" with TBD = 70 mUI
A: 18, B: 8, C: 4, D: 9

Reference receiver CTLE, fix peak gain Comments 127

Straw Poll #1:
For the reference CTLE of Annex 120G (choose one):

A. I would support the proposed change if it does not degrade VEC/EH compared to the current parameters.
B. I would support the proposed change if it improves VEC/EH compared to the current parameters, and change the max VEC / min EH accordingly.
C. I am interested in the proposed change but some modifications are required.
D. I would not support the proposed change (even with modifications).
E. I need more information.
F. I don't have an opinion.

Results: A: 3 , B: 3 , C: 3 , D: 12 , E: 10 , F: 8

April 21 ad hoc straw poll >>>>

Related presentation:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ran_3ck_adhoc_01_042121.pdf

Cl **120G** *SC* **120G.5.2** *P* **252** *L* **32** # 127

Ran, Adee — Cisco

Comment Type **T** *Comment Status* **D** *RR CTLE*

The reference receiver parameters fz, fp1, fp2, and gDC create CTLE transfer functions that are not necessarily passive (up to 0 dB across the spectrum) for all combinations.

This is different from the reference receiver used in the previous C2M specification (Annex 120E). Although 120E uses different equation and parameters, the resulting CTLE combinations always have combinations of the parameters Z1 and G that create 0 dB gain at the peaking frequency.

(The reference receiver CTLE in 120E is essentially similar to the one used in the COM method in all CR/KR specifications, in that the peaking is created by varying the zero while keeping the poles constant, with the zero being equal to fp1 for zero peaking; 120E has an addition of a flat gain G to create 0 dB maximum gain; this gain has no effect on COM, but does affect the eye height).

There was no indication or claim that the CTLE in this annex has better performance or better matches real designs than a CTLE similar to Annex 120E (with different peaking frequency). In fact, with the addition of a DFE to the reference receiver, a CTLE similar to the one in Annex 120F (C2C) may be more adequate, as the equalization at Nyquist frequency can utilize the DFE.

It is suggested to modify the reference receiver transfer functions to be similar to those of 120E. This requires a minor change in the definition of the CTLE in Annex 93A (COM).

SuggestedRemedy

Bring 93A.1.4.3 (Receiver equalizer) into the draft, and change Equation 93A–22 to include an additional factor G. Add a description of G below the equation:

"where G is a gain factor, whose value depends of the variable norm_ctle as follows:

- If norm_ctle is 1, G is set based on g_DC, f_z, g_DC2, f_LF, f_p1, and fp2, such that the maximum of H_ctf(f) across f is equal to 1.
- If norm_ctle is 0 or is not provided by the clause that invokes this method, G is set to 1."

In Table 120G–12, change the values of f_z and f_p1 to f_b/2.5, change the value of f_p2 to f_b, and add the parameter norm_ctle with value 1.

A presentation with the effect of the proposed change will be provided.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient evidence to make the proposed changes.
All of the simulations and related specifications thus far have been based upon the current CTLE pole-zero and gain parameters. Any changes to these parameters would require all related specifications to be revisited.

Table 120G–12—Eye opening reference receiver parameter values

Parameter	Symbol	Value	Units
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Continuous time filter, DC gain for TP1a Range for $g_{DC2} = 0$ Range for $-1 \le g_{DC2} < 0$ Range for $-2 \le g_{DC2} < -1$ Range for $-3 \le g_{DC2} < -2$ Step size	g_{DC}	 −2 to −9 −2 to −12 −4 to −12 −6 to −13 1.0	dB
Continuous time filter, DC gain 2 for TP1a Minimum value Maximum value Step size	g_{DC2}	 −3 0 0.5	dB
Continuous time filter, DC gain for TP4 near-end Minimum value Maximum value Step size	g_{DC}	 −5 −2 1.0	dB
Continuous time filter, DC gain 2 for TP4 near-end Minimum value Maximum value Step size	g_{DC2}	 −2 0 0.5	dB
Continuous time filter, DC gain for TP4 far-end Minimum value Maximum value Step size	g_{DC}	 −9 −3 1.0	dB
Continuous time filter, DC gain 2 for TP4 far-end Minimum value Maximum value Step size	g_{DC2}	 −3 −1 0.5	dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	12.58	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	20 28	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	$f_b / 40$	GHz

Reference receiver CTLE, value adjustments
Comments 44, 178, 179, 183

Cl **120G** SC **120G.5.2** P **252** L **16** # 44

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type **TR** *Comment Status* **D** *RR CTLE*

gDC max value may result in very large VEC > 20 dB when module are tuned in the middle of range if plugged into min loss host.

SuggestedRemedy

Suggest reducing gDC from -2 to -1 and see ghiasi_3ck_01_0421

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the task force at a previous ad hoc meeting:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf
For task force discussion

Cl **120G** SC **120G.5.2** P **252** L **25** # 178

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **D** *RR CTLE*

As a lot of the channel for TP4 far-end is known exactly, one would expect that a known subset of gDC, gDC2 combinations would be the only candidates to try. As for TP1a, I believe the strongest gDC and gDC2 should add to a constant.

SuggestedRemedy

For Continuous time filter, DC gain for TP4 far-end (gDC), change to a set of limits that depend on gDC2 in the same style as for TP1a, with the strongest gDC and gDC2 adding to a constant. The allowed values should be a subset of those for TP1a.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support any changes and the suggested remedy does not provide sufficient detail to implement.

Cl **120G** SC **120G.5.2** P **252** L **12** # 179

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **D** *RR CTLE*

By allowing stronger gDC with stronger gDC2, we can have up to 12 dB of peaking for gCD2 = -1 but up to 16 dB for gDC2 = -3 - yet we don't expect the maximum channel loss to vary like that.

SuggestedRemedy

For TP1a, change the second -12 to -11, and -13 to -10 (so the strongest "CTLE peaking" is 13).

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification for the proposed change. It is not clear that the current specifications are harmful nor is there evidence that the proposed changes won't be harmful. The CTLE peaking provides equalization for the combination of ball to ball channel as well as the routing within the packages which may exceed 20 dB.

Cl **120G** SC **120G.5.2** P **252** L **16** # 183

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **D** *RR CTLE*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes.

SuggestedRemedy

Create separate limits for TP4 short and long output modes.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient justification to support any changes and the suggested remedy does not provide sufficient detail to implement.

Table 120G–12—Eye opening reference receiver parameter values

Parameter	Symbol	Value	Units
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Continuous time filter, DC gain for TP1a Range for $g_{DC2} = 0$ Range for $-1 \le g_{DC2} < 0$ Range for $-2 \le g_{DC2} < -1$ Range for $-3 \le g_{DC2} < -2$ Step size	g_{DC}	 –2 to –9 –2 to –12 –4 to –12 –6 to –13 1.0	dB
Continuous time filter, DC gain 2 for TP1a Minimum value Maximum value Step size	g_{DC2}	 –3 0 0.5	dB
Continuous time filter, DC gain for TP4 near-end Minimum value Maximum value Step size	g_{DC}	 –5 –2 1.0	dB
Continuous time filter, DC gain 2 for TP4 near-end Minimum value Maximum value Step size	g_{DC2}	 –2 0 0.5	dB
Continuous time filter, DC gain for TP4 far-end Minimum value Maximum value Step size	g_{DC}	 –9 –3 1.0	dB
Continuous time filter, DC gain 2 for TP4 far-end Minimum value Maximum value Step size	g_{DC2}	 –3 –1 0.5	dB

Host/Module output AC CM noise value Comment 118

Cl 120G *SC* 120G.3.1 *P* 237 *L* 13 # 118

Ran, Adee Cisco

Comment Type T *Comment Status* D *AC CM noise*

Host output "AC common-mode output voltage (max, RMS)" is specified in Table 120G–1 as 17.5 mV.

This value is tighter than what is allowed for CR transmitter measured at the same point (30 mV) and also tighter than the specification for KR/C2C.

Analysis of the effect of 17.5 mV vs. 30 mV has not been provided. Devices with higher AC CM output have been demonstrated to operate with real receivers at acceptable BER on a variety of channels.

Unless evidence is provided that 30 mV is unacceptable with real receivers, the limit should be aligned with the CR specification.

Applies similarly to Module output characteristics in Table 120G–3.

SuggestedRemedy

Change the value for AC common-mode output voltage (max, RMS) from 17.5 to 30, in Table 120G–1 and Table 120G–3.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy.
For task force discussion.
[Editor's note: Line number changed from blank to 13.]

Table 120G–1—Host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
DC common-mode output voltage (max)	120G.5.1	2.8	V
DC common-mode output voltage (min)	120G.5.1	–0.3	V
Single-ended output voltage (max)	120G.5.1	3.3	V
Single-ended output voltage (min)	120G.5.1	–0.4	V
AC common-mode RMS output voltage (max)	120G.5.1	17.5	mV

Table 162–10—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Signaling rate, each (nominal)		53.125 ± 50 ppm[a]	GBd
Unit interval (nominal)		18.82353	ps
Differential pk-pk voltage with Tx disabled (max)[b]	93.8.1.3	30	mV
DC common-mode voltage (max)[b]	93.8.1.3	1.9	V
AC common-mode RMS voltage, v_{cmr} (max)[b]	93.8.1.3	30	mV

Table 163–5—Summary of transmitter specifications at TP0v

Parameter	Reference	Value	Units
Signaling rate		53.125 ± 50 ppm[a]	GBd
Differential pk-pk voltage (max)[b] Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
DC common-mode voltage (max)[b]	93.8.1.3	1.0	V
DC common-mode voltage (min)[b]	93.8.1.3	0.2	V
AC common-mode RMS voltage (max)[b]	93.8.1.3	30	mV

Table 120F–1—Transmitter electrical characteristics at TP0v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
Differential peak-to-peak output voltage[b] (max) Transmitter disabled Transmitter enabled	93.8.1.3	 35 1200	 mV mV
Common-mode voltage[b] (max)	93.8.1.3	1.9	V
Common-mode voltage[b] (min)	93.8.1.3	0	V
AC common-mode output voltage[b] (max, RMS)	93.8.1.3	30	mV

MO differential peak to peak voltage Comments 187, 206

Cl 120G SC 120G.3.2 P 240 L 8 # 206

Healey, Adam Broadcom Inc.

Comment Type TR *Comment Status* D *TP3 DPPV*

The maximum differential peak-to-peak output voltage for the "short" module output mode should be reduced. A lower output amplitude for "short" mode would reduce the input dynamic range that the host receiver needs to support. This was part of the original proposal for multiple module output modes. However, the feature has not yet been included in the standard.

SuggestedRemedy

Change the maximum differential peak-to-peak output voltage to 600 mV for the "short" module output mode.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
For task force discussion.

Cl 120G SC 120G.3.2 P 240 L 8 # 187

Dudek, Mike Marvell

Comment Type TR *Comment Status* D *TP3 DPPV*

The 900mV output amplitude allowed for the module is larger than necessary for a short channel and makes it more difficult for the host receiver to avoid being overloaded.

SuggestedRemedy

Provide two rows for Differential peak-to-peak output voltage (max) one for "long mode" and one for "short mode". Leave the "long mode" at 900mV. Make the "short mode" 600mV

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #206.

Table 120G–3—Module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate, each lane (nominal)		53.125[a]	GBd
AC common-mode output voltage (max, RMS)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max)	120G.5.1	900	mV
Eye height, differential (min)	120G.3.2.2	15	mV
Vertical eye closure (max)	120G.3.2.2	12	dB

Implement similar to the following...

Differential peak-to-peak output voltage (max) Short mode Long mode	120G.5.1	 600 900	 mV mV

The resolution of these comments may help to address comment #171 on the following slide.

MO EH value Comments 171

Cl 120G SC 120G.3.2 P 240 L 9 # 171

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *TP3 EH*

For a reasonably clean module (or test equipment in a host stressed eye test), the driver swing has to be aggressively reduced to deliver only 15 mV at near end, short mode. 120E has 70 mV, and the previous draft had 24 mV. Yet a host designer knows whether the host wants the short or long setting, and can usefully optimise for e.g. different crosstalk or noise or BER if given a reasonable signal strength. There is room to increase this weak signal without overloading the receiver.

SuggestedRemedy

Increase the eye height, short mode, from 15 mV to 18 mV

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
For task force discussion.
Resolve in conjuction with comments #187 and #206 which proposed to decrease the maximum differential peak-to-peak output voltage for short mode.

Table 120G–3—Module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate, each lane (nominal)		53.125[a]	GBd
AC common-mode output voltage (max, RMS)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max)	120G.5.1	900	mV
Eye height, differential (min)	120G.3.2.2	15	mV
Vertical eye closure (max)	120G.3.2.2	12	dB

If #187 and #206 are resolved such that the differential peak-to-peak output voltage (max) is decreased to 600 mV, then this comment might be resolved as (or similar):
REJECT
The resolution of comments #187 and #206 result in the differential peak-to-peak output voltage (max) value reduced from 900 mV to 600 mV.

Module output EH Comment 34

https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf

Cl **120G** *SC* **120G.3.2** *P* **240** *L* **10** # **34**

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type **TR** *Comment Status* **D** *TP4 EH*

Given that now we have AUI-S/L far end eye would be AUI-S min eye opening

SuggestedRemedy

The eye opening with 50 mUI rectangular window for AUI-L is VEO=11 mV, see ghiasi_3ck_01_0121

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Pending task for review slide 9 of the following presentation:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf
In Table 120G-3 create separate rows for EH (min) for short and long setting.
For short setting leave EH (min) at 15 mV.
For long setting set EH (min) to 11 mV.
[Editor's note: Changed page/line from 164/13 to 240/10.]

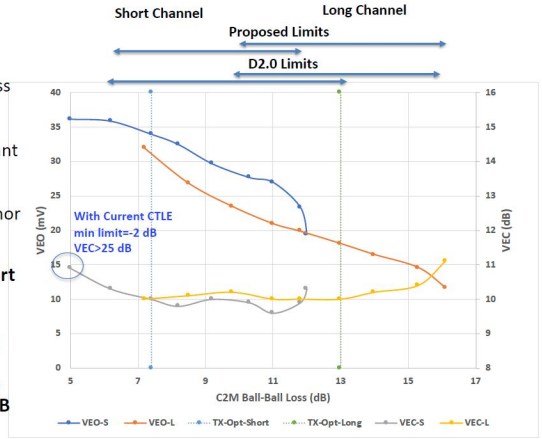
Table 120G–3—Module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate, each lane (nominal)		53.125[a]	GBd
AC common-mode output voltage (max, RMS)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max)	120G.5.1	900	mV
Eye height, differential (min)	120G.3.2.2	15	mV
Vertical eye closure (max)	120G.3.2.2	12	dB
Common-mode to differential return loss (min)	120G.3.1.1	Equation (120G–1)	dB
Effective return loss, ERL (min)	120G.3.2.3	8.5	dB
Differential termination mismatch (max)	120G.3.1.3	10	%
Transition time (min, 20% to 80%)	120G.3.1.4	8.5	ps
DC common-mode voltage (min)[b]	120G.5.1	–350	mV
DC common-mode voltage (max)[a]	120G.5.1	2850	mV

[a]The signaling rate range is derived from the PMD receiver input.
[b]DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

M2C Short and Long Channels

- **Current D2.0 definition of TP4 short and long**
  - Short 0 – 160 mm (6.6 dB) + MTF Loss
  - Long 80 mm (3.1 dB) – 244.7 mm (9.6 dB) + MTF Loss
    - 9.6 dB + 6.6 dB MTF loss exceed max 16 dB
    - 244.7 mm should be reduced to 239.7 mm (9.4 dB)
  - Short channel max loss up to 13.2 results in significant VEC/VEO degrading
    - Propose to reduce short channel max loss to 12 dB
  - Not clear if MTF variations should be accounted or nor with current procedure explicitly specifying added trace
- **Proposed new limit for TP4 short/long adjusting short max loss and accounting for MTF loss**
  - Assumes MTF loss of 6.6 dB
    - Short range will be from 6.6 – 11.8 dB (0 – 132.6 mm)
    - Long range will be from 9.7 – 16 dB (80 – 239.7 mm)
- **If one allow short range to go to as low as 5 dB VEC> 25 dB but this issue is avoided if one adjust for 1.6 dB MTF loss difference otherwise gDC need to be reduced from -2 dB to -1 dB.**



A. Ghiasi — IEEE 802.3ck Task Force — 9

MO test setup
Comment 188

Note: Comment #233 (already closed) requests that the transition time parameters be collected in the stressed eye parameter tables.

Revised proposed response:
REJECT
The host output minimum transition time is specified as 10 ps. With a long trace similar transition time might be possible with appropriate transmitter equalization and/or use of a driver with faster transition time.

Cl 120G *SC* 120G.3.2.2 *P* 241 *L* 13 # 188

Dudek, Mike — Marvell

Comment Type T *Comment Status* D *TP3 XTALK*

It is unlikely that a host that is asking for a "long mode" will have a fast risetime, and therefore the crosstalk will be less, helping the module achieve better VEC and VEO

SuggestedRemedy

Change to "transition time of 10ps with short mode and 15ps with long mode". Also in table 120G-1 Change the existing row to be for "when requesting short mode" and add another row with value 15ps for "transition time (min 20% to 80%) when requesting long mode." and on page 245 line 53 change to "and transition time of 10ps with short mode and 15ps with long mode as measured at TP1a"

Proposed Response *Response Status* W

PROPOSED REJECT.
The justification provided by the comment is not valid. The choice of long or short mode does reflect the insertion loss and therefore (in that regard) the transition time. In long mode with more peaking, the transition time might be smaller.

120G.3.2.2 Module output eye height and vertical eye closure

Figure 120G–7 depicts an example module output eye height and vertical eye closure test configuration. Module output eye height and vertical eye closure are measured at TP4 using compliance boards defined in 120G.5.3. For each module output mode, eye height and vertical eye closure are measured according to the method described in 120G.3.2.2.1 using both the near-end and far-end host channels.

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP1a (without the use of a reference receiver) with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps.

Table 120G–1—Host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
DC common-mode output voltage (max)	120G.5.1	2.8	V
DC common-mode output voltage (min)	120G.5.1	–0.3	V
Single-ended output voltage (max)	120G.5.1	3.3	V
Single-ended output voltage (min)	120G.5.1	–0.4	V
AC common-mode RMS output voltage (max)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	120G.5.1	 35 870	mV
Eye height, differential (min)	120G.3.1.5	10	mV
Vertical eye closure (max)	120G.3.1.5	12	dB
Common-mode to differential return loss (min)	120G.3.1.1	Equation (120G–1)	dB
Effective return loss, ERL (min)	120G.3.1.2	7.3	dB
Differential termination mismatch (max)	120G.3.1.3	10	%
Transition time (min, 20% to 80%)	120G.3.1.4	10	ps

[a]For a PMA in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the signaling rate presented to the PMA input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMA or FEC sublayers.

Comments 41
MO test setup

Cl **120G** *SC* **120G.3.2.2.1** *P* **242** *L* **10** # **41**

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type **TR** *Comment Status* **D** *TP3 host PCB*

Table 120G-5 PCB length are for the reference MCB but based on construction the MCB loss may vary

SuggestedRemedy

Add note to the table that above PCB length assumes an MCB loss of 2.4 dB, please also list the PCB losses in dB instead of every reader trying to calculate
80 mm = 3.1 dB
160 mm = 6.6 dB
244.7 mm = 9.6 dB
To account for any difference in MTF loss from 6.6 dB it would be beter to list the dB value for the trace+MTF and list the PCB lenghts as reference, in that case then
80 mm becomes = 3.1+6.6 = 9.7 dB
160 mm becomes = 6.6+6.6 dB=13.2 dB
244.7 mm 9.6 + 6.6 dB=16.2 dB
Looking at Ghiasi_3ck_01_0421 there are several issues with above limits:
1. Max trace loss need to be reduced from 244.7 mm to 239.7 mm so the max loss is 16 dB
2. Current 160 mm max range for short results in excess VEC propose to reduce 132.6 mm (5.2 dB)
The proposed optimized new limits become:
Short 6.6 - 11.8 dB (inlcude 6.6 dB MTF loss)
Long 9.7 - 16 dB (include 6.6 dB MTF loss)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
[Editor's note: Changed subclause from 120G.3.2.2 to 120G.3.2.2.1.]
The following related presentation was reviewed by the task force at a previous ad hoc meeting:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf
The location of the measurement host PCB is not shown Figure 120G-8, but should be part of the measurement receiver between the MCB and the reference receiver.
It would be helpful to note the assumed MCB insertion loss and the insertion loss associated with each of measurement host PCB lengths listed in Table 120G-5. However, it is not necessary to provide the sum of the two. Specifying host PCB length to finer precision than 1 mm is not necessary.
Change long-far-end PCB length to 240 mm.
Change short-far-end PCB length to 133 mm.
In Figure 120G-7, change "reference receiver" to "host PCB and reference receiver".
In Table 120G-5, add an extra column for host PCB insertion loss.

https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf

120G.3.2.2.1 Near-end and far-end eye measurement methodology

The signal measured at TP4 is first convolved with a host channel. The host channel is the host receiver printed circuit board (PCB) signal path $S^{(HOSPR)}$ defined in 162.11.7.1.1 with the exceptions that the length z_p for each test is provided in Table 120G–5, and C_0 and C_1 are both 0 nF. The eye height and vertical eye closure are measured using the method in 120G.5.2.

Table 120G–5—PCB length for module output measurements

Module output mode	Host channel type	PCB length, z_p (mm)
Short	near-end	0
Short	far-end	160
Long	near-end	80
Long	far-end	244.7

Module output mode	Host channel type	PCB length, z_p (mm)	PCB loss (dB)
Short	near-end	0	0
Short	far-end	~~160~~133	5.2
Long	near-end	80	2.1
Long	far-end	~~244.7~~240	9.4

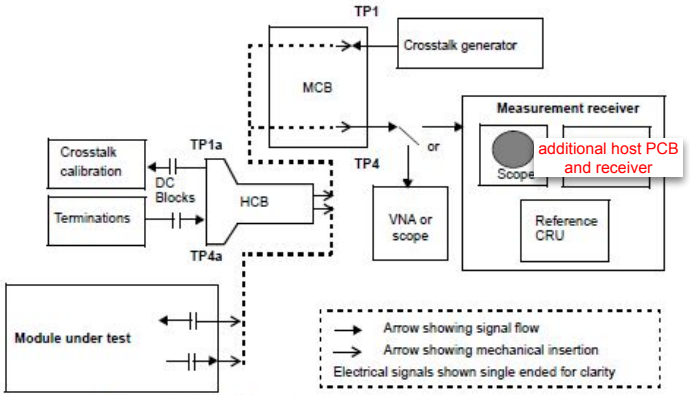


Figure 120G–7—Example module output test configuration

HO EH/VEC Comment 39

Cl 120G SC 120G.3.1 P 237 L 17 # 39

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR *Comment Status* D *TP1 EH/VEC*

VEC limit of 12 dB and VEO limit of 10 mV results in well constructed host to fail, this was not the case prior to adding timing window of +/-50 mUI.

SuggestedRemedy

The agreement was not to shift the burden for host or module when we defined new values for VEC and VEO based on timing window ts=+/- 50 mUI. Unfortuntatly the VEC and VEO limits result in host that passed now will fail.
Propose new limits for VEO=8 mV and VEC=13.5 dB and see ghiasi_3ck_01_0421

Proposed Response *Response Status* W

PROPOSED ACCEPT.
Pending task for review of the following presentation:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf

Table 120G–1—Host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
DC common-mode output voltage (max)	120G.5.1	2.8	V
DC common-mode output voltage (min)	120G.5.1	–0.3	V
Single-ended output voltage (max)	120G.5.1	3.3	V
Single-ended output voltage (min)	120G.5.1	–0.4	V
AC common-mode RMS output voltage (max)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	120G.5.1	 35 870	mV
Eye height, differential (min)	120G.3.1.5	10	mV
Vertical eye closure (max)	120G.3.1.5	12	dB

Comments 140 (part 1)
HI/MI SIT ERL test point

Cl **120G** *SC* **120G.3.4.1.1** *P* **248** *L* **17** # **140**

Hidaka, Yasuo — Credo Semiconductor, Inc.

Comment Type **T** *Comment Status* **D** *ERL TP*

It says "The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2."
120G.3.1.2 measures the host output ERL at TP1a rather than TP1.
Hence, the ERL of the test system is measured at TP1a, not at TP1.

SuggestedRemedy

Change
"The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2."

to

"The return loss of the test system at TP1 meets the ERL specification given in 120G.3.1.2 when measured at TP1a."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Also, in Figure 120G-10 and figure 120G-9, the connections of the HCB and module under test to the MCB are incorrect.
Implement the suggested remedy.
In Figure 120G-9 connect the dashed line from the HCB TP1a path to the MCB TP1 path and connect the module under test input path to the MCB TP4 path.
In Figure 120G-10 connect the dashed line from the MCB TP4 path to the HCB TP4a path and connect the host under test input path to the HCB TP1a path.

The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 120G–9. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification in Table 120F–1. The target pattern generator 20% to 80% transition time at the input to the test channel in the module stressed input test is 9 ps. The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2.

Comments 140 (part 2)
HI/MI SIT ERL test point

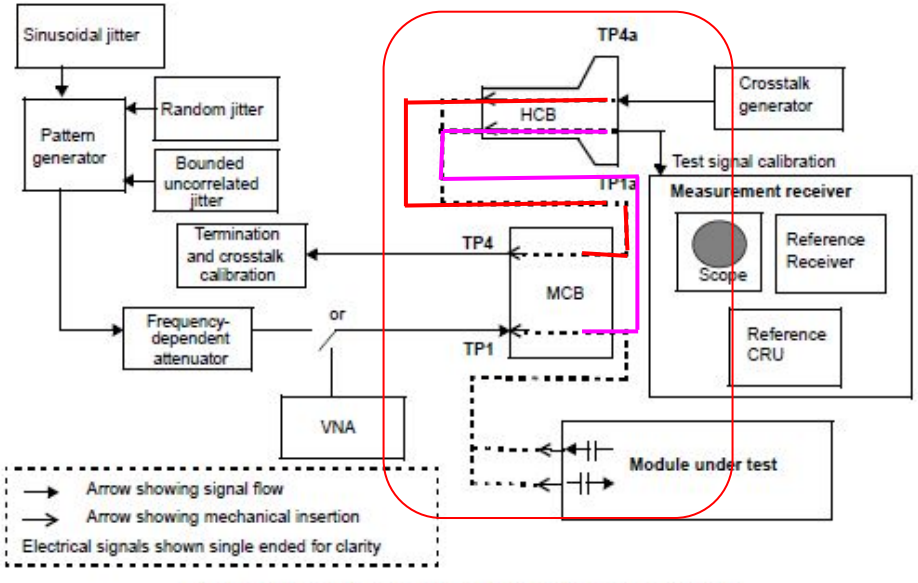


Figure 120G–10—Example module stressed input test

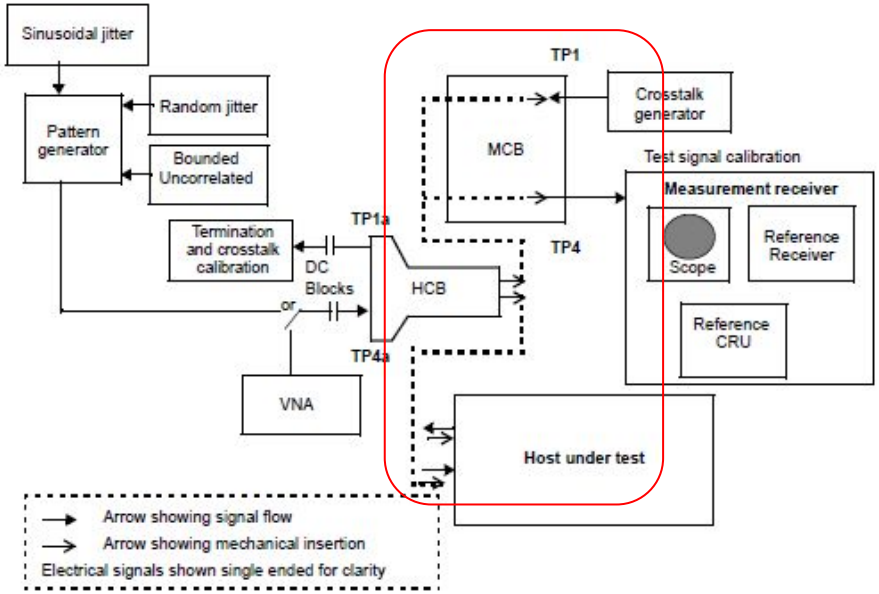


Figure 120G–9—Example host stressed input test

Comments 28, 30, 29, 31 (part 1)
HI/MI SIT jitter calibration

Cl **120G** *SC* **120G.3.3.3** *P* **244** *L* **45** # **28**

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **D** *host input jitter*

Reports of high VEC measurements were reported in calvin_3ck_02_1020 suggest 50 nUI of Sj is a strong factor. The value of Sj seems to be inherited from older specification. Hence there does not seem to be a tie between Tx jitter measured and Rx jitter injected.

SuggestedRemedy

Based on extrapolation from J3u in 162 and 163 add to table 120G-6
Jitter (max)
Jrms = 0.23 UI refer to 120F.3.1.3
J4u = 0.129 UI refer to 120F.3.1.3
Even-odd jitter, pk-pk = 0.023 UI refer to 120F.3.1.3

Proposed Response *Response Status* **W**

PROPOSED REJECT.
[Editor's note: Change subclause, page, and line from 120G.3.3/243/24 to 120G.3.3.3/244/45.]
The commenter intended to refer to Table 120G-8 "Host stressed input parameters".
The following reflects the intent of the comment.
Comment #30 proposes related updates to text referring to Table 120G-8.
Comment #29 proposes similar updates for module input.
Add the following jitter parameters to Table 120G-8:
Jrms = 0.23 UI (target) refer to 120F.3.1.3
J4u = 0.129 UI (target) refer to 120F.3.1.3
Even-odd jitter, pk-pk (max) = 0.023 UI refer to 120F.3.1.3
Including these jitter parameters to Table 120G-8 could be interpreted as being the intended end result of the calibration rather than a starting point per the methodology that references these parameters.
The comment does not provide sufficient evidence for the suggested changes.
Resolve in conjuction with comments #29 and #30.
For task force discussion.

Cl **120G** *SC* **120G.3.3.3.1** *P* **245** *L* **49** # **30**

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **D** *host input jitter*

There is more than a few dB VEC difference between simulations using the COM computation script using 0.025 UI of Add and measurements using 50 mUI of Sj for a 16 dB channel. The measured VEC with 50 mUI of Sj approaches 15.7 dB,
The actual jitter injected during the a receiver compliance test may introduce a degree of instrument and test set up jitter uncertainty or amplification at the receiver test point.

SuggestedRemedy

Change p245 line 49
Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum JRMS and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1.
To
Random jitter and bounded uncorrelated jitter are added such that the input to the host approximates the output jitter profile given by maximum JRMS and maximum J4u, and complies with the even-odd jitter specification, in Table 120G-6.
Other solutions are possible like lowering injected Sj to 20 mUI.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The intent of this comment is to update the text relating to the parameters proposed in comment #28.
Resolve using the response to comment #28.

https://www.ieee802.org/3/ck/public/adhoc/apr28_21/mellitz_3ck_adhoc_01a_042821.pdf

Comments 28, 30, 29, 31 (part 2)
HI/MI SIT jitter calibration

Cl **120G** *SC* **120G.3.4.1** *P* **247** *L* **43** # **29**

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **D** *module input jitter*

Reports of high VEC measurements were reported in calvin_3ck_02_1020 suggest 50 nUI of Sj is a strong factor. The value of Sj seems to be inherited from older specification.
Hence there does not seem to be a tie between Tx jitter measured and Rx jitter injected.

SuggestedRemedy

Based on extrapolation from J3u in 162 and 163 add to table 120G-10
Jitter (max)
Jrms = 0.23 UI refer to 120F.3.1.3
J4u = 0.129 UI refer to 120F.3.1.3
Even-odd jitter, pk-pk = 0.023 UI refer to 120F.3.1.3

Proposed Response *Response Status* **W**

PROPOSED REJECT.
[Editor's note: Changed subclause from 120G.3.2 to 120G.3.4.1 and line from 21 to 43]
The commenter intended to refer to Table 120G-11 "Module stressed input parameters".
Comment #28 proposes similar changes for the host input.
Comment #30 proposes related updates to text referring to Table 120G-11.
Implement the following with editorial license.
Add the following jitter parameters to Table 120G-11:
Jrms (target) = 0.23 UI refer to 120F.3.1.3
J4u (target) = 0.129 UI refer to 120F.3.1.3
Even-odd jitter, pk-pk (max) = 0.023 UI refer to 120F.3.1.3
Including these jitter parameters to Table 120G-1 could be interpreted as being the intended end result of the calibration rather than a starting point per the methodology that references these parameters.
For task force discussion.

Cl **120G** *SC* **120G.3.4.1.1** *P* **248** *L* **12** # **31**

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **D** *module input jitter*

There is more than a few dB VEC difference between simulations using the COM computation script using 0.025 UI of Add and measurements using 50 mUI of Sj for a 16 dB channel. The measured VEC with 50 mUI of Sj approaches 15.7 dB.
The actual jitter injected during the a receiver compliance test may introduce a degree of instrument and test set up jitter uncertainty or amplification at the receiver test point.

SuggestedRemedy

Change p245 line 49
Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum JRMS and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1.
To
Random jitter and bounded uncorrelated jitter are added such that the input to the host approximates the output jitter profile given by maximum JRMS and maximum J4u, and complies with the even-odd jitter specification, in Table 120G-10.
Other solutions are possible like lowering injected Sj to 20 mUI.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The intent of this comment is to update the text relating to the parameters proposed in comment #29.
Resolve using the response to comment #29.

https://www.ieee802.org/3/ck/public/adhoc/apr28_21/mellitz_3ck_adhoc_01a_042821.pdf

Comments 28, 30, 29, 31 (part 3) HI/MI SIT jitter calibration

120G.3.3.3 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 120G.3.3.3.1. The input shall satisfy the input tolerance using the parameters Table 120G–8 for either the module output short or long mode.

Table 120G–8—Host stressed input parameters

Parameter	Value
Applied peak-to-peak sinusoidal jitter	Table 120G–9
Eye height (target)	15 mV
Vertical eye closure (min)	12 dB
Vertical eye closure (max)	12.5 dB

#28 proposes to add newly JRMS, J4u, and EOJ to this table with new values.

Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to ensure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1. The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps as measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with PRBS13Q. The pattern

#30 proposes to update the highlighted sentence to point to Table 120G-8.

120G.3.4.1 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 120G.3.4.1.1. The input shall satisfy the input tolerance with the parameters in Table 120G–11.

Table 120G–11—Module stressed input parameters

Parameter	Value
Applied pk-pk sinusoidal jitter	Table 120G–9
Eye height (target)	10 mV
Vertical eye closure (min)	12 dB
Vertical eye closure (max)	12.5 dB

#29 proposes to add JRMS, J4u, and EOJ to this table with new values.

The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 120G–9. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification in Table 120F–1. The target pattern generator 20% to 80% transition time at the input to the test channel in the module stressed input test is 9 ps. The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2.

#31 proposes to update the highlighted sentence to point to Table 120G-11.

MI SIT
Comment 125

Cl 120G SC 120G.3.4.1.1 P 248 L 44 # 125

Ran, Adee Cisco

Comment Type TR *Comment Status* D *module input SIT*

"For the high loss case, pre-emphasis capability is likely to be required in the pattern generator to meet the TP1a eye height and vertical eye closure specifications."

It is not specified what kind of pre-emphasis the pattern generator should include. In presentations to the task force, there were some assumptions about a CR host transmitter (3 precursors and 1 postcursor); it is reasonable to assume similar capabilities for a C2M host output.

Also, it should be explicitly permissible to use pre-emphasis for both high-loss and low-loss cases.

SuggestedRemedy

Delete "For the high-loss case,"

Add after this sentence: "The pattern generator is expected to be able to apply pre-emphasis equivalent to the Transmit equalizer functional model specified in 162.9.3.1. Pre-emphasis may be set separately for the high-loss and low-loss cases".

Proposed Response *Response Status* W

PROPOSED REJECT.
The intent of the statement is meant as a helpful warning that it may need preemphasis (or as permission to use preemphasis) rather than to specify that preemphasis shall be required and if so how.

For the high loss case, pre-emphasis capability is likely to be required in the pattern generator to meet the TP1a eye height and vertical eye closure specifications.

The change proposed in the suggested remedy would be as follows:

~~For the high-loss case, p~~Pre-emphasis capability is likely to be required in the pattern generator to meet the TP1a eye height and vertical eye closure specifications. The pattern generator is expected to be able to apply preemphasis equivalent to the Transmit equalizer functional model specified in 162.9.3.1. Pre-emphasis may be set separately for the high-loss and low-loss cases.

MI SIT
Comments 126

Cl 120G *SC* 120G.3.4.1.1 *P* 249 *L* 10 # 126

Ran, Adee Cisco

Comment Type TR *Comment Status* D *module input SIT*

Here it is specified that "Random jitter and the pattern generator output levels are adjusted (...) to result in the eye height for all three eyes given in Table 120G–11"

But:

The random jitter level has already been adjusted in a prior step (P248 L15) "such that the output of the pattern generator approximates the output jitter profile given by maximum JRMS and maximum J4u".

Random jitter cannot satisfy both conditions. Adding higher jitter than J4u/JRMS specifications is an overstress (since host output should not have such higher jitter). Unlike low EH, high jitter cannot be compensated by simple Rx circuitry.

Eye height should be adjustable by pattern generator output level (after VEC has been obtained by other means; this is the subject of another comment) but not using random jitter.

SuggestedRemedy

Delete "Random jitter and".

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy.
For task force discussion.

In hindsight, this suggested remedy may not be valid as the text referenced in the comment specifies a starting point.

For the high-loss case, frequency-dependent attenuation is added such that the loss at 26.56 GHz from the output of the pattern generator to TP1a is 18.2 dB. The 18.2 dB loss represents 16 dB channel loss with an additional allowance for host transmitter package loss. Eye height and VEC are then measured at TP1a as described in 120G.5.2. Random jitter and the pattern generator output levels are adjusted (without exceeding the differential peak-to-peak input voltage tolerance specification as shown in Figure 120G–10) to result in the eye height for all three eyes given in Table 120G–11 using the reference receiver with the setting that minimizes the vertical eye closure. The CTLE setting, g_{DC}+g_{DC2}, has to be less than or equal to –13 dB.

The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 120G–9. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification in Table 120F–1. The target pattern generator 20% to 80% transition time at the input to the test channel in the module stressed input test is 9 ps. The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2.

MI SIT
Comment 224

Cl **120G** *SC* **120G.3.4.1.1** *P* **249** *L* **8** # 224

Wu, Mau-Lin — MediaTek Inc.

Comment Type **TR** *Comment Status* **D** *module input SIT*

The frequency-dependent attenuation added from output of the pattern generator to TP1a is 18.2 dB, which is 16 dB channl loss with 2.2 dB for host transmitter package loss. However, 2.2 dB is too small a value for host transmitter package loss with 31 mm package trace length.

SuggestedRemedy

By leveraging what adopted in OIF CEI-112G-VSR-PAM4, propose to adopt the 19.5 dB value to replace 18.2 dB, where 3.5 dB representing host transmitter package loss is reasonable.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The comment does not provide sufficient evidence to make the proposed change. The referenced OIF document specifies signaling rate up to 58 GBd rather than 53.125 GBd specified in Annex 120G.

For the high-loss case, frequency-dependent attenuation is added such that the loss at 26.56 GHz from the output of the pattern generator to TP1a is 18.2 dB. The 18.2 dB loss represents 16 dB channel loss with an additional allowance for host transmitter package loss. Eye height and VEC are then measured at TP1a as described in 120G.5.2. Random jitter and the pattern generator output levels are adjusted (without exceeding the differential peak-to-peak input voltage tolerance specification as shown in Figure 120G–10) to result in the eye height for all three eyes given in Table 120G–11 using the reference receiver with the setting that minimizes the vertical eye closure. The CTLE setting, $g_{DC}+g_{DC2}$, has to be less than or equal to –13 dB.

HI/MI SIT additive noise (part 1)
Comment 119, 123

Cl **120G** *SC* **120G.3.3.3.1** *P* **244** *L* **53** # 119

Ran, Adee — Cisco

Comment Type **TR** *Comment Status* **D** *TP4 additive noise*

In the host input stressed eye calibration procedure, "The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern".

This signal does not necessarily represent a real module output, in which the EH and VEC can also be affected by additive noise (which is quite different from jitter in its effect on a receiver). Stressing the host with a high level of bounded uncorrelated jitter (which is not fully specified, and may create different stress for different DUTs) does not test its ability to operate with a noisy module.

Adjusting the VEC using additive noise, as done in the CR/KR/C2C tolerance tests, should at least be allowed instead of using "bounded uncorrelated jitter"; it may be preferable in some setups. For the time being, it is suggested as an alternative.

SuggestedRemedy

Add a wideband noise source to the diagram in Figure 120G–9, between the pattern generator and the HCB.

Add a description of the noise source to the text, with reference to 93C.1 (where noise source specification is defined) and setting f_NSD1 to 1 GHz, as in 163.9.3.4.

Add that calibrating the noise source level is an alternative method to adding BUJ for calibrating the EH and VEC.

Editorial license is suggested, but if necessary for accepting the comment I can provide candidate text before comment resolution.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Comment #123 proposes a similar change to the module stressed input configuration.
Additive amplitude noise is not the same as BUJ and so it is not an inter-changeable alternative.
The suggested remedy is not sufficiently complete to implement.
Refer to Clause 162 comment #207 which proposes to specify the characteristics of the additive noise.

Cl **120G** *SC* **120G.3.4.1.1** *P* **248** *L* **1** # 123

Ran, Adee — Cisco

Comment Type **TR** *Comment Status* **D** *TP2 additive noise*

In the module input stressed eye calibration procedure, "The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation".

This signal does not necessarily represent a real host output, in which the EH and VEC can also be affected by additive noise (which is quite different from jitter in its effect on a receiver). Stressing the module with a high level of bounded uncorrelated jitter (which is not fully specified, and may create different stress for different DUTs) does not test its ability to operate with a noisy host.

Note that in a host transmitter it is often easier to control clock jitter than to reduce additive noise coupling from multiple sources in an ASIC.

Adjusting the VEC using additive noise, as done in the CR/KR/C2C tolerance tests, should at least be allowed instead of using "bounded uncorrelated jitter"; it may be preferable in some setups. For the time being, it is suggested as an alternative.

SuggestedRemedy

Add a wideband noise source to the diagram in Figure 120G–10, between the pattern generator and the frequency-dependent attenuator.

Add a description of the noise source to the text, with reference to 93C.1 (where noise source specification is defined) and setting f_NSD1 to 1 GHz, as in 163.9.3.4.

Add that calibrating the noise source level is an alternative method to adding BUJ for calibrating the EH and VEC.

Editorial license is suggested, but if necessary for accepting the comment I can provide candidate text before comment resolution.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
Resolve using the response to comment #119.

HI/MI SIT additive noise (part 2)
Comment 119, 123

120G.3.3.3.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 120G–9. The stressed signal is applied at TP4a and is calibrated at TP4. A reference clock recovery unit (CRU) with a corner frequency of 4 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using the PRBS13Q Pattern (see 120.5.11.2.1). The reference receiver is specified in 120G.5.2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern. Sinusoidal jitter is applied with frequency and peak-to-peak amplitude according to each case in Table 120G–9.

120G.3.4.1.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 120G–10. The stressed signal is applied at TP1 and is calibrated at TP1a. A reference CRU with a corner frequency of 4 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using a PRBS13Q pattern.

Eye height vertical eye closure are measured according to the method described in 120G.5.2.

The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 120G–9. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification in Table 120F–1. The target pattern generator 20% to 80% transition time at the input to the test channel in the module stressed input test is 9 ps. The ERL of the test system as measured at TP1 meets the specification given in 120G.3.1.2.

HI/MI SIT CM noise
Comment 121, 124

Cl 120G SC 120G.3.4.1.1 P 248 L 1 # 124

Ran, Adee Cisco

Comment Type TR *Comment Status* D *TP2 SIT CM noise*

The module stressed eye does not include any common-mode noise, even though a host output is allowed to have some common-mode AC content.

In a real system, the common-mode AC content of the host can degrade the module's (electrical) receiver performance, via the module's allowed termination mismatch or by circuit sensitivity. This will not be detected in the module test without common-mode content, and may not be addressed in design - but it can cause compliant modules to fail with real hosts.

For uncorrelated common mode noise, a sinusoidal source should be used. However, for the host output it is likely that common-mode content is generated by conversion from a differential signal and is therefore correlated to it. In this test, it is suggested that p/n skew is the preferred way to create the allowed common-mode RMS level.

SuggestedRemedy

In another comment I am suggesting to add a wideband noise source to the diagram in Figure 120G–10, between the pattern generator and the frequency-dependent attenuator.

For adding correlated common-mode noise, a skew between the p and n components of the frequency-dependent attenuator should be added and calibrated to create the allowed common-mode RMS level. Alternatively, a sinusoidal common-mode signal can be added, at any frequency up to the Nyquist frequency.

Add the necessary text for calibrating the common mode output at TP1a.

Editorial license is suggested, but if necessary for accepting the comment I can provide candidate text before comment resolution.

Proposed Response *Response Status* W

PROPOSED REJECT.
Resolve using the response to comment #121.

Cl 120G SC 120G.3.3.3.1 P 245 L 42 # 121

Ran, Adee Cisco

Comment Type TR *Comment Status* D *TP4 SIT CM noise*

The host stressed eye does not include any common-mode noise, even though a module output is allowed to have some common-mode AC content.

In a real system, the common-mode AC content of the module can be converted to differential noise at the host's receiver, via the S21DC of the host input channel, which is not specified at all. This will not be detected in the host test without common-mode content, and may not be addressed in host channel design - but it can cause compliant hosts to fail with real modules.

The common mode noise stress should be a sinusoid at any frequency up to the Nyquist frequency, and should be calibrated at TP4 to have the RMS value allowed for the module output in Table 120G–3.

SuggestedRemedy

In another comment I am suggesting to add a wideband noise source to the diagram in Figure 120G–9, between the pattern generator and the HCB.

If the other comment is accepted, an addition for this comment would be to make the noise source also have a common mode component. otherwise, add a common mode noise source in the same location instead.

Add the necessary text for calibrating the common mode output at TP4.

Editorial license is suggested, but if necessary for accepting the comment I can provide candidate text before comment resolution.

Proposed Response *Response Status* W

PROPOSED REJECT.
Resolve in conjunction with comment #124.
The comment does not provide sufficient justification for the proposed change. The suggested remedy does not provide sufficient detail to implement. A detailed proposal justifying the nature of the stress signal and details how to generate and apply it are required.

HI SIT calibration
Comment 122

Cl **120G** *SC* **120G.3.4.1.1** *P* **247** *L* **49** # 122

Ran, Adee Cisco

Comment Type **T** *Comment Status* **D** *TP4 SIT calibration*

The instructions for calibrating the module stressed input are unclear and unstructured, and there are missing parts, such as when and how VEC is optimized.

It would be better to write it as procedure separated to steps, as done for example in 120G.5.2, and in other receiver test procedures such as 110.8.4.2.1 through 110.8.4.2.5, or annex 93C.

SuggestedRemedy

A proposal for restructuring will be provided in a presentation.

Proposed Response *Response Status* **W**

PROPOSED REJECT.
The suggested remedy as written does not provide sufficient detail to implement.
Pending task force review of presentation.

120G.3.4.1.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 120G–10. The stressed signal is applied at TP1 and is calibrated at TP1a. A reference CRU with a corner frequency of 4 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using a PRBS13Q pattern.

Eye height vertical eye closure are measured according to the method described in 120G.5.2.

No presentation received.

Module input SIT calibration
Comment 42

Cl 120G SC 120G.3.4.1 P 247 L 17 # 42

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR *Comment Status* D *TP4a SIT EH/VEC*

VEC limit of 12 dB and VEO limit of 10 mV results in well constructed host to fail, this was not the case prior to adding timing window of +/-50 mUI.

SuggestedRemedy

The agreement was not to shift the burden for host or module when we defined new values for VEC and VEO based on timing window ts=+/- 50 mUI. Unfortuntatly the VEC and VEO limits result in host that passed now will fail.
Propose new limits for VEO=8 mV and VEC=13.25 to 13.75 dB and see ghiasi_3ck_01_0421

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
[Editor's note: Changed page from 233 to 247 and subclause from 120G.3.1.5 to 120G.3.4.1]
Pending task for review of the following presentation:
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf

120G.3.4.1 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 120G.3.4.1.1. The input shall satisfy the input tolerance with the parameters in Table 120G–11.

Table 120G–11—Module stressed input parameters

Parameter	Value
Applied pk-pk sinusoidal jitter	Table 120G–9
Eye height (target)	10 mV
Vertical eye closure (min)	12 dB
Vertical eye closure (max)	12.5 dB

https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf

Host input SIT calibration Comment 208

Cl 120G SC 120G.3.3.3.1 P 246 L 13 # 208

Healey, Adam Broadcom Inc.

Comment Type TR *Comment Status* D *TP4 SIT eye opening*

The stressed input signal calibration procedure states that "random jitter and the pattern generator output levels are adjusted (without exceeding the differential peak-to-peak input voltage tolerance specification as shown in Table 120G–7) to result in the eye height for all three eyes given in Table 120G–8 with the setting of the CTLE that minimizes the vertical eye closure." The term "output levels" is ambiguous. It could be interpreted to be "pattern generator output amplitude" or "individual PAM-4 signal levels". This needs to be clarified.

SuggestedRemedy

Change:
"Random jitter and the pattern generator output levels are adjusted (without exceeding the differential peak-to-peak input voltage tolerance specification as shown in Table 120G–7) to result in the eye height for all three eyes given in Table 120G–8 with the setting of the CTLE that minimizes the vertical eye closure."
To:
"Random jitter and the pattern generator differential peak-to-peak output voltage are adjusted so that the height of the smallest eye matches the value in Table 120G-8. The differential peak-to-peak input voltage tolerance given in Table 120G-7 is not exceeded."

Make a similar change to 120G.3.4.1.1 (page 249, line 10).

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
For task force discussion.

may be changed to a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration and the stressed input test. For the case where the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane, so that the symbols on each lane are not correlated. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

The stressed input is calibrated using the methodology in 120G.3.2.2.1 using the far-end host channel specified for the module output mode as requested by the host (see 120G.3.2.2). The eye height and vertical eye closure are set to the target values in Table 120G–8 when measured according to the method in 120G.5.2. Meeting the BER requirement using only one module output mode, as requested by the host, is sufficient.

Random jitter and the pattern generator output levels are adjusted (without exceeding the differential peak-to-peak input voltage tolerance specification as shown in Table 120G–7) to result in the eye height for all three eyes given in Table 120G–8 with the setting of the CTLE that minimizes the vertical eye closure. Pre-emphasis capability is likely to be required in the pattern generator to meet this requirement.

The pattern is then changed to Pattern 5, Pattern 3, or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for the input test which is conducted by inserting the HCB into the host under test. Patterns 3 and 5 are described in Table 124–9.

If the test is performed with pattern 3, the host BER may be calculated using the host's PMA test pattern checker (see 120.5.11.2.2). If the test is performed with pattern 5 or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal, the BER may be calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits. The number of received bits may be estimated based on the test time.

HI SIT calibration Comment 120

Cl 120G SC 120G.3.3.3.1 P 245 L 41 # 120

Ran, Adee Cisco

Comment Type E *Comment Status* D *TP4 SIT wording*

In the host stressed input test procedure there is a "block" paragraph of 18 lines, which contains some 13 sentences, dealing with the bounded uncorrelated jitter (purpose, definition), calibration of jitter (BUJ and random), and crosstalk signal requirements and calibrations, with great detail and no clear list of requirements. This is painful to read (many times).

The paragraph should be broken to shorter paragraphs and possibly a list of requirements, to make it more legible, and separate requirements from informative explanations.

SuggestedRemedy

Rephrase and reformat as necessary.

If required, I can create a detailed proposal, but I trust the editors to be able to improve this paragraph by inspection.

Proposed Response *Response Status* W

PROPOSED ACCEPT.

Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to ensure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1. The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps as measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with PRBS13Q. The pattern may be changed to a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration and the stressed input test. For the case where the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane, so that the symbols on each lane are not correlated. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

The following or similar reformatting might address Adee's concern:

Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum JRMS and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1.

Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. The clock source for the PRBS generator is asynchronous to the pattern generator clock source to ensure non-correlation of the jitter.

The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps as measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with PRBS13Q. The pattern may be changed to a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration and the stressed input test. For the case where the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane, so that the symbols on each lane are not correlated. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

MI RLCD Comment 181

CI 120G SC 120G.3.1.1 P 237 L 36 # 181

Dawe, Piers Nvidia

Comment Type E *Comment Status* D *TP1 RLCD*

In other specs such as CEI-56G-VSR-PAM4 and CEI-56G-VSR-PAM4, the output differential to common-mode return loss is 3 dB better than the input common-mode to differential mode return loss at low frequency, for a good reason, but in this annex they are the same.

SuggestedRemedy

Unless we find a reason not to, offset the specs in the usual way.

Proposed Response *Response Status* W

PROPOSED REJECT.
The comment does not provide sufficient justification for the proposed changes nor does the suggested remedy provide sufficient detail to implement.

120G.3.3.1 Host input differential to common-mode return loss

Differential to common-mode return loss of the host input is shown in Equation (120G–2) and illustrated in Figure 120G–8.

$$RLCD(f) \le \begin{cases} 22 - 20(f/53.125) & 0.01 \le f \le 26.56 \\ 15 - 6(f/53.125) & 26.56 < f \le 53.125 \end{cases} \quad \text{(120G–2)}$$

where

RLCD is the differential to common-mode return loss in dB

f is the frequency in GHz

Table 120G–10—Module input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, each lane (range)		TP1	53.125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	120G.5.1	TP1a	900	mV
Differential to common-mode return loss (min)	120G.3.3.1	TP1	Equation (120G–2)	dB

120G.3.1.1 Host output common-mode to differential return loss

Common-mode to differential return loss of the host output is shown in Equation (120G–1) and illustrated in Figure 120G–5.

$$RLDC(f) \le \begin{cases} 22 - 20(f/53.125) & 0.01 \le f \le 26.56 \\ 15 - 6(f/53.125) & 26.56 < f \le 53.125 \end{cases} \quad \text{(120G–1)}$$

where

RLDC is the common-mode to differential return loss in dB

f is the frequency in GHz

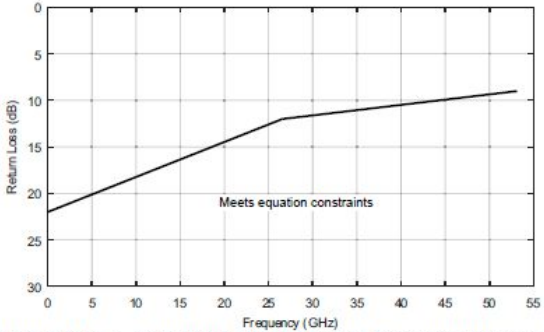


Figure 120G–5—Host output common-mode to differential return loss

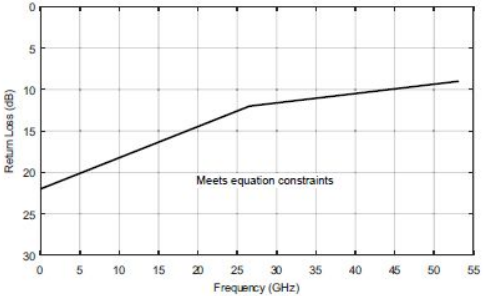


Figure 120G–8—Host input differential to common-mode return loss

Precoding
Comment #234

Cl 120G	*SC* 120G.1	*P* 235	*L* 38	# 234

Dawe, Piers — Nvidia

Comment Type TR *Comment Status* D *precoding*

Up to now, the optical PMD channels have not needed a very strong DFE, and the C2M loss (10 dB for C2M CAUI-4, 10.2 for 200GAUI-4 C2M, 16 for 400GAUI-4) is low enough that CR and KR PMDs don't need a very strong DFE when used as C2M. Therefore, we never have precoding on C2M at 50G/lane - simple. At 100G/lane, links such as active copper cables will benefit from a very strong DFE in the receiver in the cable end that's receiving from a higher loss in the cable. 802.3 enables such active cables via the C2M specs; up until now there was nothing more to say, so they don't get a mention in 802.3. Adding precoding after the signal has been serialised is best avoided, so it should be added in the host, so for the first time, there is something that 802.3 should do specifically about active cables.

SuggestedRemedy

Allow optional precoding abilities in 100G/lane C2M transmitters and receivers in the host. Add MDIO registers to advertise these abilities and to enable them.

Proposed Response *Response Status* W

PROPOSED REJECT.
Precoding if used is added and removed by the PMA at each end of a physical link as necessary. Similarly, an active cable can add precoding at the transmitter at one end and remove the precoding at the other end.
Precoding must be enabled (or disabled) on both Tx and Rx in the same direction; this is coordinated using training for CR/KR or by station management for C2C. This cannot be done with C2M and active cable (end-to end) because neither AN nor link training are available. Applying precoding internally within an active cable is still possible.

Nothing to point to since it is addition of a new feature.

Module output modes
Comments 56, 175, 223

120G.3.2.1 Module output modes

The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and vertical eye closure (max) in Table 120G–3 for both near-end and far-end measurements (see 120G.3.2.2).

One method for configuring the module output mode is to configure the module for a particular host electrical interface. Mapping of the combination of IEEE 802.3 interface type and module output mode to a host electrical interface may be determined from Table 120G–4.

Table 120G–4—Module output mode mapping

IEEE 802.3 interface type	Module output mode	Host electrical interface
100GAUI-1 C2M	short	100GAUI-1-S C2M
100GAUI-1 C2M	long	100GAUI-1-L C2M
200GAUI-2 C2M	short	200GAUI-2-S C2M
200GAUI-2 C2M	long	200GAUI-2-L C2M
400GAUI-4 C2M	short	400GAUI-4-S C2M
400GAUI-4 C2M	long	400GAUI-4-L C2M

Cl 120G *SC* 120G.3.2.1 *P* 240 *L* 27 # 175

Dawe, Piers — Nvidia

Comment Type T *Comment Status* D *wording*

The module output doesn't have to "support" two modes (e.g. receive, co-operate, enable, or similar), it has to actually do them. They are abilities of the module.

SuggestedRemedy

Change "The module output shall support two modes: short and long." to "There are two module output modes: short and long."

Proposed Response *Response Status* W

PROPOSED REJECT.
The proposed changes to wording do not improve the quality of the draft.

Cl 120G *SC* 120G.3.2.1 *P* 240 *L* 27 # 56

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type T *Comment Status* D *wording*

Short and long are not very descriptive

SuggestedRemedy

Please replace short and long with "lower loss hosts" and "higher loss hosts"

Proposed Response *Response Status* W

PROPOSED REJECT.
The interpretation of short and long modes is implicit in the test methodology specified in 120G.3.2.2. The suggested remedy is not generally accurate. Use of a concise label for each mode is helpful.

Cl 120G *SC* 120G.3.2.1 *P* 240 *L* 37 # 223

Wu, Mau-Lin — MediaTek Inc.

Comment Type TR *Comment Status* D *wording*

In Table 120G-4, Module output mode mapping, there are 100GAUI-1-S C2M, 100GAUI-1-L C2M, and etc. defined for "Host electrical interface". However, no definitions of those "Host electrical interface" were found in the whole specification. Based on that, the information provided by this Table may be confusing for the readers.

SuggestedRemedy

We shall either add the definitions of 100GAUI-1-S & 100GAUI-1-L C2M or remove Table 120G-4.

Proposed Response *Response Status* W

PROPOSED REJECT.
Table 120G-4 defines what those labels mean.

Module output modes
Comment 40

Cl 120G SC 120G.3.2.1 P 240 L 37 # 40

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR *Comment Status* D *reference*

Table 120G-4 defines AUI short and long but with proper reference

SuggestedRemedy

Please reference table 120G-5

Proposed Response *Response Status* W

PROPOSED REJECT.
Short and long modes are defined in the first paragraph of 120G.3.2.1. Table 120G-5 provides parameters for the measurement of EH and VEC at the module output when configured for short or long mode.

120G.3.2.1 Module output modes

The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and vertical eye closure (max) in Table 120G–3 for both near-end and far-end measurements (see 120G.3.2.2).

One method for configuring the module output mode is to configure the module for a particular host electrical interface. Mapping of the combination of IEEE 802.3 interface type and module output mode to a host electrical interface may be determined from Table 120G–4.

Table 120G–4—Module output mode mapping

IEEE 802.3 interface type	Module output mode	Host electrical interface
100GAUI-1 C2M	short	100GAUI-1-S C2M
100GAUI-1 C2M	long	100GAUI-1-L C2M
200GAUI-2 C2M	short	200GAUI-2-S C2M
200GAUI-2 C2M	long	200GAUI-2-L C2M
400GAUI-4 C2M	short	400GAUI-4-S C2M
400GAUI-4 C2M	long	400GAUI-4-L C2M

120G.3.2.2.1 Near-end and far-end eye measurement methodology

The signal measured at TP4 is first convolved with a host channel. The host channel is the host receiver printed circuit board (PCB) signal path $S^{(HOSPR)}$ defined in 162.11.7.1.1 with the exceptions that the length z_p for each test is provided in Table 120G–5, and C_0 and C_1 are both 0 nF. The eye height and vertical eye closure are measured using the method in 120G.5.2.

Table 120G–5—PCB length for module output measurements

Module output mode	Host channel type	PCB length, z_p (mm)
Short	near-end	0
Short	far-end	160
Long	near-end	80
Long	far-end	244.7

Terminology Comment 20

Cl 120G SC 120G.3.1.5 P 239 L 8 # 20

Brown, Matt Huawei

Comment Type ER *Comment Status* D *(bucket3)*

An acronym for vertical eye closure (VEC) is defined in the first sentence of 120G.3.1.5. However, the acronym is rarely used in 120G and the full name is normally used. Since this acronym was not defined in 120E, where the base methodology is defined, 120G should continue to use the full name only.

SuggestedRemedy

Delete all instance of the acronym VEC in 120G.
Alternately, where appropriate, replace all instances of "vertical eye closure" with the acronym VEC.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
With editorial license, remove all instances of "VEC" in 120G by either replacing "VEC" with "vertical eye closure" or deleting "VEC" as appropriate.

Revised proposed response:

PROPOSED ACCEPT IN PRINCIPLE.
With editorial license, replace all instances of "vertical eye closure" with "VEC", where appropriate.

120G.3.1.5 Host output eye height and vertical eye closure

Figure 120G–6 depicts an example host output eye height and vertical eye closure (VEC) test configuration. Host output eye height and vertical eye closure are measured at TP1a using compliance boards defined in 120G.5.3. Eye height and vertical eye opening are measured according to the method described in 120G.5.2.

Terminology Comment 14

Cl **120G** *SC* **120G.3.1** *P* **237** *L* **17** # **14**

Brown, Matt — Huawei

Comment Type **ER** *Comment Status* **D** *(bucket3)*

The eye height is defined by the measurement method in 120G.3.1.5 and it is not necessary to qualify it as being "differential". If so, the VEC should also be qualified as "differential".

SuggestedRemedy

Change "Eye height, differential (min)" to "Eye height (min)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Table 120G–1—Host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
DC common-mode output voltage (max)	120G.5.1	2.8	V
DC common-mode output voltage (min)	120G.5.1	–0.3	V
Single-ended output voltage (max)	120G.5.1	3.3	V
Single-ended output voltage (min)	120G.5.1	–0.4	V
AC common-mode RMS output voltage (max)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	120G.5.1	 35 870	mV
Eye height, differential (min)	120G.3.1.5	10	mV
Vertical eye closure (max)	120G.3.1.5	12	dB
Common-mode to differential return loss (min)	120G.3.1.1	Equation (120G–1)	dB
Effective return loss, ERL (min)	120G.3.1.2	7.3	dB
Differential termination mismatch (max)	120G.3.1.3	10	%
Transition time (min, 20% to 80%)	120G.3.1.4	10	ps

[a]For a PMA in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the signaling rate presented to the PMA input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMA or FEC sublayers.