Author's note: This update incorporates the resolution of other comments related to 120G.3.4.1, which have been resolved or are in the initial bucket.

Thanks to Matt Brown and Piers Dawe for reviewing and suggesting important corrections and improvements.

120G.3.4.1 Module stressed input test

The module stressed input tolerance is tested with the setup defined in 120G.3.4.1.1. The test is defined with two stressed signal cases, low-loss and high-loss, which are calibrated separately as described in 120G.3.4.1.2. The test procedure is described in 120G.3.4.1.3.

The module under test shall meet the BER requirement in 120G.1.1:

– for both the high-loss and low-loss cases,
– with all sinusoidal jitter cases in Table 162–15, and
– for any signaling rate in the range given in Table 120G–10.

Commented [AR(1]: Comment #13

Commented [AR(2]: Comment #12 (bucket – proposed response)

120G.3.4.1.1 Module stressed input test setup

The module stressed input test setup is illustrated in Figure 120G–10. The stressed signal is applied at TP1 and is calibrated at TP1a.

The stressed signal includes the following impairments:

– Sinusoidal jitter, random jitter, and bounded uncorrelated jitter

– Frequency-dependent attenuation representing the host channel, which may be implemented with PCB traces. The frequency-dependent attenuation is used only for the high-loss case (see 120G.3.4.1.2).

– Counter-propagating crosstalk signals.

Bounded uncorrelated jitter may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a low-pass filtered pseudo-random pattern. The pattern should be either PRBS7 or PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source. The low-pass filter has 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz.

Commented [AR(3]: Currently "The PRBS pattern length should be between PRBS7 and PRBS9" – incorrect

A crosstalk generator for counter-propagating signals representing the module output is used for calibration of the stress. The counter-propagating signals are asynchronous to the pattern generator. This crosstalk generator is not present in the test, being replaced by the output of the module under test.

The measurement receiver has a reference clock recovery unit (CRU) that acts as a high-pass jitter filter with a 3 dB corner frequency of 4 MHz and slope of 20 dB/decade.

The test system meets the ERL specification given in 120G.3.1.2 when measured at TP1a.

Commented [AR(4]: Comment #131 (editorial change from response: "is used to calibrate the stressed signal using a PRBS13Q pattern" moved to the calibration subclause)

Commented [AR(5]: Comment #140

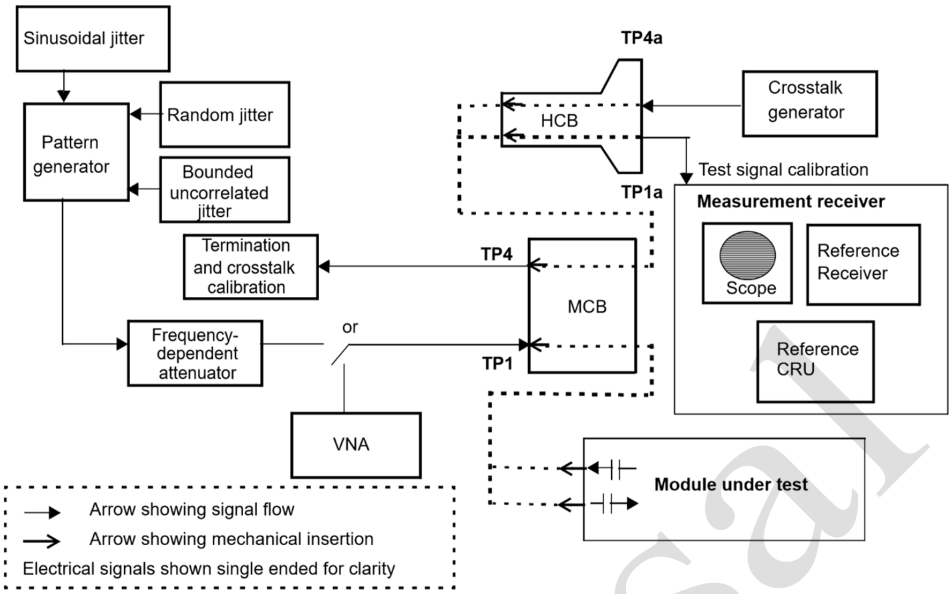

Figure 120G–10—Example module stressed input test setup

120G.3.4.1.2 Module stressed input calibration

The stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (pattern 4; see Table 124–9) with 20% to 80% transition time at the input to the frequency-dependent attenuator as specified in Table 120G–11.

b) Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–15.

c) Random jitter and bounded uncorrelated jitter are added to the sinusoidal jitter such that the jitter profile of the signal at the pattern generator output approximates J_{RMS} (max) and J4u (max) and complies with the even-odd jitter (max) specification in Table 120F–1.

d) The HCB is plugged into the MCB. The counter-propagating crosstalk signals are calibrated to the differential peak-to-peak voltage and transition time specified in Table 120G–11, measured at TP4 (without the use of a reference equalizer). The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (pattern 3), scrambled idle (pattern 5), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

e) For the low-loss signal calibration, the output of the pattern generator is fed directly to the MCB input (TP1). For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the loss at 26.56 GHz from the output of the pattern generator to TP1a is 18.2 dB. This represents 16 dB channel loss with an additional allowance for host transmitter package loss.

f) Eye height and VEC are measured at TP1a as described in 120G.5.2. The pattern generator random jitter and output levels are adjusted so that the height of the smallest eye matches the value in Table 120G-11. The differential peak-to-peak input voltage tolerance given in Table 120G-10 is not exceeded. For the high-loss case, the reference receiver CTLE is limited to settings where gDC+gDC2 is less than or equal to –13 dB. This restriction does not apply for the low-loss case. The resulting vertical eye closure has to be within the limits in Table 120G–11. The pattern generator pre-emphasis and reference receiver setting that minimizes the vertical eye closure is used.

Commented [AR(6]: Comment #13

Commented [AR(7]: Comment #233

Commented [AR(8]: Comment #208 (“Make a similar change to 120G.3.4.1.1”)

Table 120G–11—Module stressed input parameters

Parameter	Value
Pattern generator transition time (target)	9 ps
Applied pk-pk sinusoidal jitter	Table 120G–9
Eye height (target)	10 mV
Vertical eye closure (min)	12 dB
Vertical eye closure (max)	12.5 dB
Crosstalk generator differential pk-pk voltage (target)	870 mV
Crosstalk generator transition time (target)	10 ps

Commented [AR(9]: Moved to the table by comment #233

Commented [AR(10]: Moved to the table by comment #233

120G.3.4.1.2 Module stressed input test procedure

After the stress has been calibrated, the pattern generator is set to generate either PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, with sinusoidal jitter per the selected case in Table 162–15. The HCB is detached from the MCB and the module under test is plugged into the MCB. The module electrical output is enabled on all lanes with any of the patterns above.

Commented [AR(11]: Comment #13

If the test is performed with PRBS31Q, the module BER may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2), if this option is implemented in the module, as the number of bit errors divided by the number of received bits. The module BER is the average of the BER of each of its lanes.

Commented [AR(12]: Clarification of the requirement to match the convention of 83E, 120E

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the module BER may be calculated by placing the module under test into local loopback (see 120.5.9) and feeding the module output into a compliant host or its equivalent. The module BER is then calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

The number of received bits may be estimated based on the test time.

Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results.