# 802.3ck D2.1 Comment Resolution 120G

Matt Brown, Huawei, P802.3ck Editor-In-Chief

# 120G EH/VEC measurement mask/window, part 1
# 39, 106

Cl 120G SC 120G.5.2 P 266 L 25 # 39

Ran, Adee Cisco systems

*Comment Type* TR *Comment Status* D *EO method*

As has been reported in calvin_3ck_adhoc_01_063021, the authors have been "unable to reliably close the calibration loop on TP1a at 12.5dB VEC with precision lab equipment" for insertion loss of 16.4 dB. This suggests that the VEC specification may be unfeasible.

Allowing a higher (worse) VEC for transmitters (host/module outputs) might pass bad receivers with very closed eyes, which will put more burden on receivers (even if the signal in stressed input test does not change, receivers will have to work with transmitters that have the same VEC due to other reasons, e.g. a "rectangular eye" closed by high noise that can't be equalized, rather than ISI).

Instead of lowering the VEC bar for transmitters, we should look at the definition of VEC and make it more suitable to the expected eye shape of good transmitters after processing with the reference receiver (this shape is not rectangular), taking into account the expected behavior of real receivers.

The calculation of VEC and EH from a CDF accumulated over ts ± 0.05 UI gives the same weight to all phases. This makes sense if the receiver's phase is distributed uniformly in this window; it supposedly makes sense it we don't know where the receiver will sample within this region and account for sampling error. But the eye is not independent of the receiver - it is shaped by the receiver's equalization, and in the reference receiver we assume a certain behavior.

A receiver is expected to optimize its equalization (CTLE+DFE or equivalent) at the sampling point ts - this is part of the measurement procedure (currently steps k and l) - which would result in the maximum vertical opening being at ts. We should assume the average sampling phase is then ts; any difference between the optimized phase and the average phase is an implementation penalty that should be covered by the minimum EH.

A real receiver's CDR does not have a uniform phase distribution around its mean; the probability of sampling at either -0.05 UI or +0.05 UI from ts is smaller than the probability of sampling closer to ts. The rare events where the sample is taken far from ts contribute less to the average BER, so they should be weighted down in the calculation of the CDFs. Having equal weights as in the current method is overly pessimistic in both EH and VEC.

It is therefore proposed to apply a weighting function to the sampled data based on the phase.

*SuggestedRemedy*

A detailed proposal will be provided in a presentation.

*Proposed Response* *Response Status* W

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.1 and D2.0 or the unsatisfied negative comments from the initial ballot.

Hence it is not within the scope of the recirculation ballot.

The comment does not provide sufficient justification for any changes and the suggested remedy as written does not provide sufficient detail to implement.
The following presentation analyzed the effect of the currently specified measurement method. A similar analysis is required to make any changes.
Https://www.ieee802.org/3/ck/public/20_10/healey_3ck_01a_1020.pdf
The suggested remedy does not provide sufficient detail to implement.
A related presentation is anticipated.
For task force discussion.

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ran_3ck_01_0721.pdf

# 120G EH/VEC measurement mask/window, part 2
# 39, 106

Cl 120G SC 120G.5.2 P 266 L 23 # 106

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *EO method*

This draft has a primitive rectangular eye mask spec with mask height = max(EHmin, EA/VECmax) and mask width = 0.1 UI, although it is described as a histogram. Measuring a diamond eye with a rectangular mask is an inefficient, inaccurate way of measuring signal quality and provides weak and uncertain protection against too much jitter. Its effective width is less than its actual because of the 1e-5 probability criterion and the inefficient shape.
De-weighting the sides of the histogram/mask would make this worse, equivalent to increasing the target BER by 10x or so. A higher VEC / smaller EH limit with the rectangular mask would allow more jittered and more varied signals, particularly for very short host channels (see Mike Dudek's work) that can have faster edges than higher loss ones. The target BER is not going to change.
We need an eye mask that's more eye shaped, so that a higher proportion of the samples are near the boundary and contribute to the measurement.

*SuggestedRemedy*

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = y +/-H/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-1/16, ts+/-3/32, V = y +/-H/2, k +/-H*0.4, y. y is near VCmid, VCupp or VClow (vertically floating, as in D2.1).
H is max( EHmin, Eye Amplitude * 10^(-VECmax/20) ). Eye Amplitude is AVupp, AVmid or AVlow, as in D2.1.
This simple scalable method can remain as the EH and VEC limits are revised. Scopes have been measuring with 10-sided masks for many years, it's not more difficult than a rectangular mask and gives better results.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.0 comment #127, which was REJECT.ed on the basis of insufficient justification and insufficient analysis to show equivalent or better interoperability. No further justification or implementation detail is provided.
The comment does not provide sufficient evidence to make the proposed changes. All of the simulations and related specifications thus far have been based upon the current CTLE pole-zero and gain parameters. Any changes to these parameters would require all related specifications to be revisited.

Cl 120G SC 120G.5.2 P 253 L 23 # 180

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* R *EH/VEC method*

This draft has a primitive rectangular eye mask (H = either EHmin or EA/VECmax), although it is described as a histogram. It's an inefficient/inaccurate way of measuring a signal quality vertically and provides weak and uncertain protection against too much jitter. This is worse with the higher VEC limit in the latest draft that allows worse and more varied signals, and is a particular concern for very short host channels (see Mike Dudek's work) that can have faster edges than higher loss ones.

*SuggestedRemedy*

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = k +/-H/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-1/16, ts+/-3/32, V = k +/-H/2, k +/-H*0.4, k. k is VCmid, VCupp or VClow.
In case it's not clear, H is either EHmin or Eye Amplitude * 10^(-VECmax/20).
This simple scalable method can remain as the EH and VEC limits are revised. Scopes have been measuring with 10-sided masks for many years, it's not more difficult than a rectangular mask.

*Response* *Response Status* U

REJECT.
The currently methodology was chosen over an eye mask method like that being proposed in this comment.
See slide 3 of the following presentation was reviewed by the task force:
https://www.ieee802.org/3/ck/public/21_01/brown_3ck_04_0121.pdf
The comment does not provide sufficient justification to support the proposed changes.

Comment #180 against D2.0

## Comments 154
## Annex 120G EO Method

Cl 120G SC 120G.5.2 P 246 L 23 # 154

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *EO method*

Of all the options in dawe_3ck_01a_1020, this draft has the most primitive (rectangular eye mask) although it is described as a histogram. It's an inefficient/inaccurate way of measuring a signal and provides weak and uncertain protection against too much jitter. This will get worse if we relax the VEC limits, and is a particular concern for very short host channels (see Mike Dudek's work).

*SuggestedRemedy*

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = +/-Hmin/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-0.07, ts+/-0.1, V = +/-Hmin/2, +/-Hmin*0.4, +/-0.
(In case it's not clear, Hmin, already specified, is the greater of EH and Eye Amplitude - VEC. There will be discussion about changing those limits from other comments, but this is a simple scalable method that can remain as the EH and VEC limits are revised.)

*Proposed Response* *Response Status* W

PROPOSED REJECT.
This comment proposes a technical change to the draft that does not address technical completeness.
The comment does not provide sufficient evidence to support the proposed changes.

Slide 3 in brown_3ck_04_0121

Draft 1.4 fully specifies the eye height and vertical eye closure. Supporting presentations for the current methodology show that necessary eye width is enforced by these specifications.
https://www.ieee802.org/3/ck/public/20_10/healey_3ck_01a_1020.pdf
https://www.ieee802.org/3/ck/public/20_10/healey_3ck_02_1020.pdf

Broad support for this methodology was demonstrated by D1.3 Straw Polls #9 and #12.
https://www.ieee802.org/3/ck/public/20_10/minutes_3ck_1020_final_unapproved.pdf

Straw Poll #9:
I support the EW/ESMW direction of (Chicago rules):
A: Keep ESMW and eye width
B: Replace EH, ESMW, and eye width with an eye mask as proposed in dawe_3ck_01_1020
C: Remove ESMW and eye width and redefine EH and VEC as proposed in healey_3ck_01a_1020
D: Remove ESMW and eye width and leave EH and VEC as is
Results: A: 9, B: 10, C: 24, D: 6

Straw Poll #12:
I would support replacing ESMW and EW with the following option from healey_3ck_02_1020
A. "Alt. 2" with TBD = 50 mUI
B. "Alt. 1" with TBD1 = 25 mUI and TBD2 = 25 mUI
C. "Alt. 1" with TBD1 = 50 mUI and TBD2 = 20 mUI
D. "Alt. 2" with TBD = 70 mUI
A: 18, B: 8, C: 4, D: 9

# 120G EH/VEC measurement mask/window, part 3
# 39, 106

Comment #36

- argues that square measurement window is pessimistic as it puts too much emphasis on the outer edges of the measurement window
- proposes to resolve by weighting the contributions from the window as a function of offset from ts
- proposes weighting function with Gaussian distribution and 0.015 UI standard deviation
- see ran_3ck_01_0720

Comment #109

- restates a similar comment (#180) against D2.0 and provides no extra justification or detail
- proposes that the currently specified square window is inaccurate and does not protect against jitter

Neither comment nor the related presentation provide data showing either the effect on the established VEC and EH limits or the improvement to interoperability.

The presentation healey_3ck_01a_1020, used as justification for the current window method, provided evidence that this method does discriminate against jitter.

# RR g_DC
# 103, 104, 105

Cl 120G SC 120G.5.2 P 265 L 16 # 103

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *RR gdc*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes.

*SuggestedRemedy*

Create separate limits for TP4 short and long output modes, so 4 sets for TP4+, in the style of TP1a.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.0 comment #179, which was REJECT.ed on the basis of insufficient justification and detail. It adds request to provide 4 sets of values in the style used for TP1a but does not provide specific values. No further justification is provided. The comment does not provide sufficient justification for the proposed changes nor does the suggested remedy provide sufficient detail to implement.

Cl 120G SC 120G.5.2 P 265 L 25 # 104

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *RR gdc*

As a lot of the channel for TP4 far-end is known exactly and the max loss to TP4 far end is less than to TP1a, the range of gDC, gDC2 combinations should be a subset of the TP1a ones. As for TP1a, I believe the strongest gDC and gDC2 should add to a constant.

*SuggestedRemedy*

For Continuous time filter, DC gain for TP4 far-end (gDC), change to a set of limits that depend on gDC2 in the same style as for TP1a, with the strongest gDC and gDC2 adding to a constant. The allowed values should be a subset of those for TP1a.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.0 comment #178, which was REJECT.ed on the basis of insufficient justification and detail. No further justification or implementation detail is provided.
The comment does not provide sufficient justification for the proposed changes nor does the suggested remedy provide sufficient detail to implement.

Cl 120G SC 120G.5.2 P 265 L 12 # 105

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *RR gdc*

When gDC2 is -2, we allow no more than -(-12-2) = 14 dB of peaking, yet when gDC2 is -3, we allow -(-13-3) = 16 dB, yet the channel loss should not be higher. This doesn't make sense.

*SuggestedRemedy*

For TP1a, change -12 -12 -13 to -12 -11 -10 or -12 -12 -11 (so the strongest CTLE peaking for the highest two gDC2 categories is the same).

*Proposed Response* *Response Status* W

PROPOSED REJECT.
The comment does not provide sufficient justification for the proposed changes.

**Table 120G–11—Eye opening reference receiver parameter values**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Receiver 3 dB bandwidth | $f_r$ | $0.75 \times f_b$ | GHz |
| Continuous time filter, DC gain for TP1a<br>Range for $g_{DC2} = 0$<br>Range for $-1 \le g_{DC2} < 0$<br>Range for $-2 \le g_{DC2} < -1$<br>Range for $-3 \le g_{DC2} < -2$<br>Step size | $g_{DC}$ | <br>–2 to –9<br>–2 to –12<br>–4 to –12<br>–6 to –13<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP1a<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–3<br>0<br>0.5 | dB |
| Continuous time filter, DC gain for TP4 near-end<br>Minimum value<br>Maximum value<br>Step size | $g_{DC}$ | <br>–5<br>–1<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP4 near-end<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–2<br>0<br>0.5 | dB |
| Continuous time filter, DC gain for TP4 far-end<br>Minimum value<br>Maximum value<br>Step size | $g_{DC}$ | <br>–9<br>–3<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP4 far-end<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–3<br>–1<br>0.5 | dB |

# test system response 120

Cl 120G SC 120G.3.1.5 P 252 L 16 # 120

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *test system response*

"without the use of a reference receiver" which occurs several times, is misleading; the BT4 filter, which is the reference receiver response in so many clauses, applies.

*SuggestedRemedy*

Change to "observed through the Bessel-Thomson response of 120G.3.1 in place of the reference receiver of 120G.5.2" or similar. Several places.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.1 and D2.0 or the unsatisfied negative comments from the initial ballot.
Hence it is not within the scope of the recirculation ballot.

There could be some misinterpretation since the reference receiver as defined in 120G.5.2 includes the effect of the test equipement filter. Also, since the response is prescriptive, it should not be in parentheses.
On page 252, line 16…
Change: "calibrated at TP4 (without the use of a reference receiver)"
To: "calibrated at TP4 using a test system with a response as defined in 120G.3.1 rather than the reference receiver of 120G.5.2"
Apply similarly at page/line: 254/12, 258/43, and 262/10.
Implement with editorial license.

**120G.3.1.5 Host output eye height and vertical eye closure (VEC)**

Figure 120G–6 depicts an example host output eye height and vertical eye closure (VEC) test configuration. Host output eye height and VEC are measured at TP1a using compliance boards defined in 120G.5.3. Eye height and VEC are measured according to the method described in 120G.5.2.

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (see 120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP4 (without the use of a reference receiver) with target differential peak-to-peak voltage of 900 mV and transition time of 8.5 ps.

# HO EH/VEC 61

*Cl* 120G *SC* 120G.3.1 *P* 250 *L* 18 # 61

Ghiasi, Ali — Ghiasi Quantum/Inphi

*Comment Type* TR *Comment Status* D *HO EH/VEC*

Data from Ghiasi page 7
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf
and Calvin page 4
https://www.ieee802.org/3/ck/public/adhoc/jun30_21/calvin_3ck_adhoc_01_063021.pdf
indicate meeting current VEO/VEC at TP1a not feasible to meet

*SuggestedRemedy*

Considering that on a system all 32 ports plus lanes must meet the TP1a, the best in practice channels should have margin to pass not fail. This is an area that we need more measurement but given what we know at this point VEC should be increased to 13 dB and VEO reduced to 8.5 mV

*Proposed Response* *Response Status* W

PROPOSED REJECT.

Comment #68 proposes new values for EH and VEC for the module input based on the same justification as this comment.
The presentation calvin_3ck_adhoc_01_063021 shows that the problem is not with the host meeting the requirements, but rather with the ability to test it properly. The latter should be addressed.
The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf
Slide 5 shows that for the Lim 9" channel simulation with COM tool version 3.2 results in marginal EH (9.4 mV vs 10 mV specification) and VEC (11.9 dB vs 12 dB specification).
For task force discussion.

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf

## COM Analysis on Lim Channel 1 and 4 – ASIC to Module

**esults with COM 3.1 and COM 3.2**

- Generally VEOs are larger with COM 3.2 and VEC is about the same
- Even with improvement on VEO still fails and there is no margin on VEC
- Recommend reducing VEO=9 mV and increasing VEC to 12.5 dB
- What is puzzling why FOM ILD and ICNs are larger?

| | Window | Fitted IL@26.56 GHz | IL wPKG@26.55 GHz | VEO Case I/II/III 12/13/31 mm | VEC Case I/II/III 12/13/31 mm | EW Case I/II/III 12/13/31 mm | COM Case I/II/III* 12/13/31 mm |
|---|---|---|---|---|---|---|---|
| el 2" at TP1a 4, ICN = 4.0 mV ]= [9.1, 8.9] dB | 0 | 5.9 dB | 11.3 dB | 37.5/25.5/27.3 | 6.8/11.1/7.8 | 0.19/0.14/0.18 | 5.3/2.83/4.5 |
| | +/- 50 mUI | 5.9 dB | 11.3 dB | 26.2/13.3/18.7 | 9.9/16.4/11.1 | 0.19/0.14/0.18 | 3.3/1.4/2.8 |
| el 9" at TP1a 6, ICN = 1.7 mV ]=[10.9,11.4] dB | 0 | 14.7 dB | 20.3 dB | 16.7/11.8/12.1 | 7.2/10/8.1 | 0.19/0.15/0.17 | 5.0/3.3/4.3 |
| | +/- 50 mUI | 14.7 dB | 20.3 dB | 11.3/7.1/7.9 | 10.6/14.4/11.8 | 0.19/0.15/0.17 | 2.6/1.8/3.0 |

| | Window | Fitted IL@26.56 GHz | IL wPKG@26.55 GHz | VEO Case I/II/III 12/13/31 mm | VEC Case I/II/III 12/13/31 mm | EW Case I/II/III 12/13/31 mm | COM Case I/II/III* 12/13/31 mm |
|---|---|---|---|---|---|---|---|
| el 2" at TP1a ILD = 0.111, ICN = 4.9 mV ERL[11,22]= [9.1, 8.9] dB | 0 | 5.9 dB | 11.3 dB | 48.5/12.2/30.7 | 6.5/12.2/8.6 | 0.19/0.09/0.17 | 5.5/2.4/4.0 |
| | +/- 50 mUI | 5.9 dB | 11.3 dB | 32.9/14.0/20.3 | 9.5/16.5/11.8 | 0.19/0.13/0.17 | 3.5/1.4/2.6 |
| Lim Channel 9" at TP1a ILD = 0.087, ICN = 2.0 mV ERL[11,22]=[10.9,11.4] dB | 0 | 14.7 dB | 20.3 dB | 19.2/14.1/14.6 | 6.7/9.5/8.1 | 0.18/0.13/0.15 | 5.4/3.6/4.3 |
| | +/- 50 mUI | 14.7 dB | 20.3 dB | 13.0/8.1/9.4 | 10.0/14.4/11.9 | 0.18/0.14/0.16 | 3.3/1.8/2.5 |

A. Ghiasi — IEEE 802.3ck Task Force — 6

# MO VEC/EH
# 59, 62, 97, 98, ghiasi_01

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf

Cl 120G SC 120G.3.2 P 253 L 12 # 62

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR Comment Status D MO VEC/EH

TP4 VEC can be lowered from current 12 dB to 11 dB to allow additional penalty for real host channel and host ASIC

SuggestedRemedy

Reduce TP4 VEC=11 dB, see ghiasi_3ck_01_0721

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.
This comment pertains to the module output VEC (max).
The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf
The slide shows that with the current g_dc constraints VEC fails for the long mode, near-end measurement. The comment suggests that g_dc max for TP4 far-end be increased from -3 dB to -2 dB. With this change to the g_DC limit there is no need to change VEC (max).
It may be necessary in 120G-11, for gDC and gDC2, to change "near-end" to "short mode" and "far-end" to "long mode".
For task force discussion.

Cl 120G SC 120G.3.2 P 253 L 13 # 59

Ghiasi, Ali — Ghiasi Quantum/Inphi

Comment Type TR Comment Status D MO VEC/EH

TP4 long VEO at max loss drops to 12 mV

SuggestedRemedy

Reduce TP4 high loss VEO=12 mV, see ghiasi_3ck_01_0721

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.
This comment pertains to the module output eye height (min) for long mode, far end.
The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf
Slide 7 shows the EH (VEO) going below the required 15 mV and slide 9 proposes reducing the specification to 13 mV.
For task force discussion.

Cl 120G SC 120G.3.2 P 253 L 11 # 98

Dawe, Piers — Nvidia

Comment Type TR Comment Status D MO VEC/EH

If the eye height limit is the same at long near end as at long far end, there is huge margin at near end and the implementer is encouraged to optimise for far end or beyond, only limited by the NE VEC spec, while we want modules to be set up consistently, for the full range from near to far. EH is naturally larger at NE for a well set up output.

SuggestedRemedy

Increase the eye height, long mode near end, by 3 dB from 15 mV to 21 mV

Proposed Response Response Status W

PROPOSED REJECT.
This comment pertains to the module output eye height (min) for long mode, near end.
The comment does not provide sufficient evidence that the proposed change is necessary.
For task force discussion.

Cl 120G SC 120G.3.2 P 253 L 11 # 97

Dawe, Piers — Nvidia

Comment Type TR Comment Status D MO VEC/EH

The driver swing has to be aggressively reduced from 600 mV pk-pk to deliver only 15 mV at near end, short mode. 120E has 70 mV, and D1.4 had 24 mV, ghiasi_3ck_adhoc_01a_042121 shows 35 mV (before Vpkpk was reduced). Yet a host can usefully optimise for e.g. different crosstalk or noise if given a reasonable signal strength. A NIC has no high-loss ports so it can do this even if a switch won't. There is room to increase this weak signal without overloading the receiver. Also, making the limits more like reality encourages more consistent module setup across the industry.

SuggestedRemedy

Increase the eye height, short mode near end, by 1.1 dB from 15 mV to 17 mV

Proposed Response Response Status W

PROPOSED REJECT.
This comment pertains to the module output eye height (min) for short mode, near end.
Although the differential peak to peak voltage was reduced in D1.1, the short mode EH was not reduced accordingly.
The comment does not provide sufficient evidence that the proposed change is necessary.
For task force discussion.

# MO VEC/EH
# 59, 62, 97, 98, ghiasi_01

**Table 120G–3—Module output characteristics (at TP4)**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate, each lane (nominal) | | 53.125[a] | GBd |
| AC common-mode output voltage (max, RMS) | 120G.5.1 | 17.5 | mV |
| Differential peak-to-peak output voltage (max)<br>Short mode<br>Long mode | 120G.5.1 | <br>600<br>900 | <br>mV<br>mV |
| Eye height (min) | 120G.3.2.2 | 15 | mV |
| Vertical eye closure, VEC (max) | 120G.3.2.2 | 12 | dB |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G–1) | dB |
| Effective return loss, ERL (min) | 120G.3.2.3 | 8.5 | dB |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % |
| Transition time (min) | 120G.3.1.4 | 8.5 | ps |
| DC common-mode voltage (min)[b] | 120G.5.1 | –350 | mV |
| DC common-mode voltage (max)[a] | 120G.5.1 | 2850 | mV |

[a]The signaling rate range is derived from the PMD receiver input.
[b]DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

#97: long mode, near-end, increase to 17 mV
#59: long mode, far end, increase to 13 mV
Presumably leave at 15 mV for SM NE/FE

#62:
long-mode, near end: marginal, should we fix?

long mode, far end:
VEC is failing, leave limit alone
Instead, change TP4 far end g_DC (max) to -2 dB

# MO VEC/EH
# 59, 62, 97, 98, ghiasi_01

**Table 120G–11—Eye opening reference receiver parameter values**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Receiver 3 dB bandwidth | $f_r$ | $0.75 \times f_b$ | GHz |
| Continuous time filter, DC gain for TP1a<br>Range for $g_{DC2} = 0$<br>Range for $-1 \le g_{DC2} < 0$<br>Range for $-2 \le g_{DC2} < -1$<br>Range for $-3 \le g_{DC2} < -2$<br>Step size | $g_{DC}$ | <br>–2 to –9<br>–2 to –12<br>–4 to –12<br>–6 to –13<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP1a<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–3<br>0<br>0.5 | dB |
| Continuous time filter, DC gain for TP4 ~~near-end~~<br>Minimum value<br>Maximum value<br>Step size | $g_{DC}$ | <br>–5<br>–1<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP4 ~~near-end~~<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–2<br>0<br>0.5 | dB |
| Continuous time filter, DC gain for TP4 ~~far-end~~<br>Minimum value<br>Maximum value<br>Step size | $g_{DC}$ | <br>–9<br>–3<br>1.0 | dB |
| Continuous time filter, DC gain 2 for TP4 ~~far-end~~<br>Minimum value<br>Maximum value<br>Step size | $g_{DC2}$ | <br>–3<br>–1<br>0.5 | dB |
| Centered frequency for reference | $f_c$ | 12.89 | GHz |

#62 “replace “near-end” short mode”?

#62 replace “far-end” with “long mode”?

#62 change to -2 dB, no change to VEC (max)

# HI SI EH/VEC 66

*Cl* 120G *SC* 120G.3.3.4.2 *P* 259 *L* 16 # 66

Ghiasi, Ali — Ghiasi Quantum/Inphi

*Comment Type* TR *Comment Status* D *HI SI EH/VEC*

Host stress input VEC is too high and does not account for real host channel and ASIC packge and VEO can be as small as 12 mV

*SuggestedRemedy*

Reduce VEC=11-11.5 dB range and VEO to 12 mV, see ghiasi_3ck_01_0721

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf
Comments #59 and #62 propose changes to VEC and EH for the module output. Update the host input values based upon the resolution of those comments.
For task force discussion.

**Table 120G–8—Host stressed input parameters**

| Parameter | Value |
|---|---|
| Pattern generator transition time (target) | 9 ps |
| Applied peak-to-peak sinusoidal jitter | Table 162–16 |
| Eye height (target) | 15 mV |
| Vertical eye closure, VEC (min) | 12 dB |
| Vertical eye closure, VEC (max) | 12.5 dB |
| Crosstalk differential peak-to-peak voltage | 870 |
| Crosstalk transition time<br>for short mode<br>for long mode | <br>10 ps<br>15 ps |

Resolve using the resolution to comments for module output EH and VEC values for the module output. Comments: 59, 62, 97, 98

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf

# MI EH/VEC 68

Cl 120G SC 120G.3.4.2.2 P 262 L 18 # 68

Ghiasi, Ali — Ghiasi Quantum/Inphi

*Comment Type* TR *Comment Status* D *MI EH/VEC*

Data from Ghiasi page 7
https://www.ieee802.org/3/ck/public/adhoc/apr21_21/ghiasi_3ck_adhoc_01a_042121.pdf
and Calvin page 4
https://www.ieee802.org/3/ck/public/adhoc/jun30_21/calvin_3ck_adhoc_01_063021.pdf
indicate meeting current VEO/VEC at TP1a not feasible to meet

*SuggestedRemedy*

This is an area that we need more measurement but given what we know at this point VEC should be increased to 13 to 13.5 dB and VEO reduced to 8.5 mV to support Lim Channels, see ghiasi_3ck_01_0721

*Proposed Response* *Response Status* W

PROPOSED REJECT.
Comment #61 proposes new values for EH and VEC for the host output based on the same justification as this comment.
The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf
Resolve using the response to comment #61.

**Table 120G–10—Module stressed input parameters**

| Parameter | Value |
|---|---|
| Pattern generator transition time (target) | 9 ps |
| Applied peak-to-peak sinusoidal jitter | Table 162–16 |
| Eye height (target) | 10 mV |
| Vertical eye closure, VEC (min) | 12 dB |
| Vertical eye closure, VEC (max) | 12.5 dB |
| Crosstalk differential peak-to-peak voltage | 900 mV |
| Crosstalk transition time | 8.5 ps |

Resolve using the resolution to comments for host output EH and VEC values for the module output.
Comments: 61

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ghiasi_3ck_01_0721.pdf

# HO TT 58

Cl 120G SC 120G.3.1 P 250 L 25 # 58

Ghiasi, Ali — Ghiasi Quantum/Inphi

*Comment Type* TR *Comment Status* D *HO TT*

Transition time host requesting short mode or long mode is for TP4

*SuggestedRemedy*

Please revert to 10 ps in draft D2.0, please move this parameter to TP4 table 120G-3

*Proposed Response* *Response Status* W

PROPOSED REJECT.
This comment relates to the host output transition time specified in Table 120G-1. Separate values for host long and short modes were added per D2.1 comment #188. The justification was that the host input and host output PCB insertion loss will likely be similar, which is reflected in the transition times chosen for the host input crosstalk calibration. This must also be explicitly allowed and constrained at the hout output.

**Table 120G–8—Host stressed input parameters**

| Parameter | Value |
|---|---|
| Pattern generator transition time (target) | 9 ps |
| Applied peak-to-peak sinusoidal jitter | Table 162–16 |
| Eye height (target) | 15 mV |
| Vertical eye closure, VEC (min) | 12 dB |
| Vertical eye closure, VEC (max) | 12.5 dB |
| Crosstalk differential peak-to-peak voltage | 870 |
| Crosstalk transition time<br>for short mode<br>for long mode | <br>10 ps<br>15 ps |

**Table 120G–1—Host output characteristics at TP1a**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate, each lane (range) | | 53.125 ± 50 ppm[a] | GBd |
| DC common-mode output voltage (max) | 120G.5.1 | 2.8 | V |
| DC common-mode output voltage (min) | 120G.5.1 | –0.3 | V |
| Single-ended output voltage (max) | 120G.5.1 | 3.3 | V |
| Single-ended output voltage (min) | 120G.5.1 | –0.4 | V |
| AC common-mode RMS output voltage (max) | 120G.5.1 | 17.5 | mV |
| Differential peak-to-peak output voltage (max)<br>Transmitter disabled<br>Transmitter enabled | 120G.5.1 | <br>35<br>870 | mV |
| Eye height (min) | 120G.3.1.5 | 10 | mV |
| Vertical eye closure, VEC (max) | 120G.3.1.5 | 12 | dB |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G–1) | dB |
| Effective return loss, ERL (min) | 120G.3.1.2 | 7.3 | dB |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % |
| Transition time (min)<br>Host is requesting short mode<br>Host is requesting long mode | 120G.3.1.4 | <br>10<br>15 | <br>ps<br>ps |

[a]For a PMA in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the signaling rate presented to the PMA input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMA or FEC sublayers.

The comment suggests moving these parameter values to the module output characteristics, but that would not make sense, since the transition time is not affected by the module output setting.

The two transition times are listed for the module output crosstalk calibration already.

**120G.3.2.2 Module output eye height and VEC**

Figure 120G–7 depicts an example module output eye height and VEC test configuration. Module output eye height and VEC are measured at TP4 using compliance boards defined in 120G.5.3. For each module output mode, eye height and VEC are measured according to the method described in 120G.3.2.2.1 using both the near-end and far-end host channels.

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP1a (without the use of a reference receiver) with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps for short mode and 15 ps for long mode.

# MO DC CM voltage tolerance 49, 50

Cl 120G SC 120G.3.2 P 253 L 20 # 49

Ran, Adee Cisco systems

*Comment Type* TR *Comment Status* D *MO DC CM voltage tolerance*

footnote b says "Specification includes effects of ground offset voltage." - what does it mean?

It is unclear why the module needs a specification of DC common-mode voltage at all, given that its output is AC coupled (per 120G.1). Without AC coupling in the module, the limits given in this table are not reasonable.

*SuggestedRemedy*

Clarify what the quoted sentence mean, or delete it.

Consider removing the DC common mode voltage specification.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.1 and D2.0 or the unsatisfied negative comments from the initial ballot.
Hence it is not within the scope of the recirculation ballot.

The comment is referring to module output "DC common-mode voltage" specifications which are intended to define a tolerance for the module output to host DC bias voltage. A DC common-mode voltage tolerance specification is required as the module output, whether it be a discrete capacitor or decoupling on the die, must tolerate the DC common-mode voltage applied by the host input. This is a necessary requirement and thus should not be deleted. However, this specification as written is difficult to interpret.
Per comment #50, the footnote for "DC common-mode voltage (max)" should be "b" not "a".
Also, footnote b is informative and thus should be converted to a table note or regular text, if retained.
With editorial license implement the following as a minimum:
- change footnote "b" to a table note (per style guide)
The commenter has offered to provide a presentation to address this comment further.
For task force discussion.

Cl 120G SC 120G.3.2 P 253 L 22 # 50

Ran, Adee Cisco systems

*Comment Type* ER *Comment Status* D *MO DC CM voltage tolerance*

"DC common-mode voltage (max)" - assuming this specification is not removed, it should refer to footnote b, not footnote a.

*SuggestedRemedy*

change footnote reference from a to b.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.1 and D2.0 or the unsatisfied negative comments from the initial ballot.
Hence it is not within the scope of the recirculation ballot.

Resolve using the response to comment #49.

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ran_3ck_02_0721.pdf

# MO DC CM voltage tolerance, part 2
# 49, 50

**Table 120G–7—Host input characteristics**

| Parameter | Reference | Test point | Value | Units |
|---|---|---|---|---|
| Signaling rate, each lane (range) | 120G.3.3.1 | TP4a | 53.125 ± 100 ppm | GBd |
| Differential peak-to-peak input voltage tolerance (min)<br>for short mode<br>for long mode | 120G.5.1 | TP4 | <br>600<br>900 | mV |
| Differential to common-mode return loss (min) | 120G.3.3.2 | TP4a | Equation (120G–2) | dB |
| Effective return loss, ERL (min) | 120G.3.3.3 | TP4a | 7.3 | dB |
| Host stressed input test[a] | 120G.3.3.4 | TP4 | See 120G.3.3.4 | |
| Differential termination mismatch (max) | 120G.3.1.3 | TP4a | 10 | % |
| Common-mode voltage[b]<br>Min<br>Max | 120G.5.1 | TP4a | <br>–0.3<br>2.8 | V |

[a]Meets BER specified in 120G.1.1.
[b]Generated by host, referred to host ground.

**Table 120G–1—Host output characteristics at TP1a**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate, each lane (range) | | 53.125 ± 50 ppm[a] | GBd |
| DC common-mode output voltage (max) | 120G.5.1 | 2.8 | V |
| DC common-mode output voltage (min) | 120G.5.1 | –0.3 | V |
| Single-ended output voltage (max) | 120G.5.1 | 3.3 | V |
| Single-ended output voltage (min) | 120G.5.1 | –0.4 | V |
| AC common-mode RMS output voltage (max) | 120G.5.1 | 17.5 | mV |
| Differential peak-to-peak output voltage (max)<br>Transmitter disabled | 120G.5.1 | <br>35 | mV |

**Table 120G–3—Module output characteristics (at TP4)**

| Parameter | Reference | Value | Units |
|---|---|---|---|
| Signaling rate, each lane (nominal) | | 53.125[a] | GBd |
| AC common-mode output voltage (max, RMS) | 120G.5.1 | 17.5 | mV |
| Differential peak-to-peak output voltage (max)<br>Short mode<br>Long mode | 120G.5.1 | <br>600<br>900 | mV<br>mV |
| Eye height (min) | 120G.3.2.2 | 15 | mV |
| Vertical eye closure, VEC (max) | 120G.3.2.2 | 12 | dB |
| Common-mode to differential return loss (min) | 120G.3.1.1 | Equation (120G–1) | dB |
| Effective return loss, ERL (min) | 120G.3.2.3 | 8.5 | dB |
| Differential termination mismatch (max) | 120G.3.1.3 | 10 | % |
| Transition time (min) | 120G.3.1.4 | 8.5 | ps |
| DC common-mode voltage (min)[b] | 120G.5.1 | –350 | mV |
| DC common-mode voltage (max)[a] | 120G.5.1 | 2850 | mV |

[a]The signaling rate range is derived from the PMD receiver input.
[b]DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

**Table 120G–9—Module input characteristics**

| Parameter | Reference | Test point | Value | Units |
|---|---|---|---|---|
| Signaling rate, each lane (range) | 120G.3.4.1 | TP1 | 53.125 ± 100 ppm | GBd |
| Differential pk-pk input voltage tolerance (min) | 120G.5.1 | TP1a | 900 | mV |
| Differential to common-mode return loss (min) | 120G.3.3.2 | TP1 | Equation (120G–2) | dB |
| Effective return loss, ERL (min) | 120G.3.4.3 | TP1 | 8.5 | dB |
| Differential termination mismatch (max) | 120G.3.1.3 | TP1 | 10 | % |
| Module stressed input test[a] | 120G.3.4.2 | TP1a | See 120G.3.4.2 | |
| Single-ended voltage tolerance range (min) | 120G.5.1 | TP1a | –0.4 to 3.3 | V |
| DC common-mode voltage (min)[b] | 120G.5.1 | TP1 | –350 | mV |
| DC common-mode voltage (max)[b] | 120G.5.1 | TP1 | 2850 | mV |

[a] Meets BER specified in 120G.1.1.
[b] DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

# MO DC CM voltage tolerance, part 3
# 49, 50

Alternate implementation…

| Table 120G–3—Module output characteristics at TP4 | | | |
|---|---|---|---|
| **Parameter** | **Reference** | **Value** | **Units** |
| DC common-mode voltage tolerance (range)<br>Upper limit<br>Lower limit | 120G.3.2.4 | <br>2.85<br>-0.35 | <br>V<br>V |

New subclause…

**120G.3.2.4 Module output common-mode voltage tolerance**
DC common-mode voltage is generated by the host. A module shall meet all output specifications with any DC common-mode voltage (see 120G.5.1), as measured at TP4, within the range specified in Table 120G-3.
NOTE--The specified voltages allow for the effects of ground offset voltage.

| Table 120G–9—Module input characteristics | | | | |
|---|---|---|---|---|
| **Parameter** | **Reference** | **Test point** | **Value** | **Units** |
| DC common-mode voltage tolerance (range)<br>Upper limit<br>Lower limit | 120G.3.4.4 | TP1 | <br>2.85<br>-0.35 | <br>V<br>V |

New subclause…

**120G.3.4.4 Module input common-mode voltage tolerance**
DC common-mode voltage is generated by the host. A module shall meet all input specifications with any DC common-mode voltage (see 120G.5.1), as measured at TP1, within the range specified in Table 120G-9.
NOTE--The specified voltages allow for the effects of ground offset voltage.

# MO SI host reference channel 102

Cl 120G SC 120G.3.2.2.1 P 254 L 51 # 102

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *MO SI host reference channel*

The near end and far end should be placed far enough apart so that the module implementer has little choice what emphasis to use, so that all modules are set up similarly. As short is easier than long, this means that far minus near (mm or dB) for short should be at least as much as far minus near for long. As real host channels are not exactly like the theoretical reference host channel, there should be a healthy overlap of short and long to give the host room for its implementation. D2.0's 160 mm delivered on both these criteria, D2.1's 133 mm doesn't.

*SuggestedRemedy*

Change 133 to 150, change 80 to 90

*Proposed Response* *Response Status* W

PROPOSED REJECT.
The comment does not provide sufficient justification for the proposed changes.

**120G.3.2.2.1 Near-end and far-end eye measurement methodology**

The signal measured at TP4 is first convolved with a reference host channel. The reference host channel is the host receiver printed circuit board (PCB) signal path $S^{(HOSPR)}$ defined in 162.11.7.1.1 with the exceptions that the length $z_p$ for each test is provided in Table 120G–5, and $C_0$ and $C_1$ are both 0 nF. The eye height and VEC are measured using the method in 120G.5.2.

**Table 120G–5—PCB length for module output measurements**

| Module output mode | Host channel type | PCB length, $z_p$ (mm) |
|---|---|---|
| Short | near-end | 0 |
| Short | far-end | 133 |
| Long | near-end | 80 |
| Long | far-end | 244.7 |

# HI/MI AC CM voltage tolerance, part 1
# 51, 55

Cl 120G SC 120G.3.3 P 255 L 34 # 51

Ran, Adee Cisco systems

*Comment Type* TR *Comment Status* D *MO AC CM noise tolerance*

The host should tolerate the AC common mode output allowed for the module output. Even if this is not included in the stressed input test, this expectation should be part of the host input specification.

*SuggestedRemedy*

Add a row to Table 120G–7 with parameter "AC common-mode input voltage tolerance (RMS)" and value based on Table 120G–3.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
Comment #55 proposes a similar change to the host input.
A parameter with only a value is not sufficient. A test method including some constraints on the CM noise, e.g., frequency spectrum, PDF, etc., is necessary.
For task force discussion.

Cl 120G SC 120G.3.4 P 260 L 9 # 55

Ran, Adee Cisco systems

*Comment Type* TR *Comment Status* D *MI AC CM noise tolerance*

The module should tolerate the AC common mode output allowed for the host output. Even if this is not included in the stressed input test, this expectation should be part of the module input specification.

*SuggestedRemedy*

Add a row to Table 120G–9 with parameter "AC common-mode input voltage tolerance (RMS)" and value based on Table 120G–1.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
Comment #51 proposes a similar change to the host input.
Resolve using the response to comment #51.

Context and proposal provided in presentation.

The following presentation was provided by the commenter:
https://www.ieee802.org/3/ck/public/21_07/ran_3ck_03_0721.pdf

# HI/MI AC CM voltage tolerance, part 2
# 51, 55

Alternate implementation…

| Table 120G–7—Host input characteristics | | | | |
|---|---|---|---|---|
| **Parameter** | **Reference** | **Test point** | **Value** | **Units** |
| AC common-mode RMS voltage tolerance (min) | 120G.3.3.6 | TP4 | 25 | mV |

New subclause…

**120G.3.3.6 Module input AC common-mode voltage tolerance**
A host input shall meet all other specifications with AC common-mode voltage (see 120G.5.1) up to the limit specified in Table 120G-7.

| Table 120G–9—Module input characteristics | | | | |
|---|---|---|---|---|
| **Parameter** | **Reference** | **Test point** | **Value** | **Units** |
| AC common-mode RMS voltage tolerance (min) | 120G.3.4.5 | TP1a | 25 | mV |

New subclause…

**120G.3.4.5 Module input AC common-mode voltage tolerance**
A module input shall meet all other specifications with AC common-mode voltage (see 120G.5.1) up to the limit specified in Table 120G-9.

# MI SI method 9

Cl 120G SC 120G.3.4.2.2 P 262 L 26 # 9

Brown, Matt Huawei

*Comment Type* T *Comment Status* D *MI SI method*

This step g) has criteria for VEC which might be interpreted as conflicting.
"The pattern generator random
... are adjusted so that ... VEC is within the limits in Table 120G–10."
"The pattern generator pre-emphasis and
reference receiver settings that minimize VEC are used."
I believe the the latter criteria was intended to specify that for each pattern generator output jitter/voltage the pre-emphasis is adjusted to minimize VEC.

*SuggestedRemedy*

Change: "The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used."
To: "For any jitter and voltage setting, the pattern generator pre-emphasis and reference receiver settings that minimize VEC are used."

*Proposed Response* *Response Status* W

PROPOSED ACCEPT.

g) Eye height and VEC are measured at TP1a as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–10. The differential peak-to-peak input voltage tolerance given in Table 120G–9 is not exceeded. For the high-loss case, the reference receiver CTLE is limited to settings where $g_{DC} + g_{DC2}$ is less than or equal to –13 dB. This restriction does not apply for the low-loss case. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

# HI SI method
# 53, 71, 72

Cl 120G SC 120G.3.3.4.2 P 258 L 33 # 53

Ran, Adee Cisco systems

*Comment Type* T *Comment Status* D *HI SI method*

Unlike the jitter levels in step c, the initial signal levels in the calibration procedure are not defined. Using inappropriately low levels can result in bad jitter measurement in step c.

To achieve good jitter measurement, the initial output levels should be as high as possible without exceeding the differential peak to peak specification.

Also applies in module stressed input test, 120G.3.4.2.2.

*SuggestedRemedy*

Add guidance to step a to use initial signal level as high as possible such that the differential peak-to-peak input voltage tolerance given in Table 120G–9 is not exceeded.

*Proposed Response* *Response Status* W

PROPOSED REJECT.
The proposed change is one of many considerations that are outside the scope of this test procedure.
For task force discussion.

Cl 120G SC 120G.3.3.4.2 P 258 L 39 # 72

Dudek, Mike Marvell

*Comment Type* E *Comment Status* D *HI SI method*

The final values of jitter used in the test are unlikely to match these values of Jrms and J4u because crosstalk is added in step e and random jitter is adjusted in step g. It would be helpful to the reader to indicate this.

*SuggestedRemedy*

Add to the end of bullet c. "Note that these are initial jitter values. They will be modified by the addition of crosstalk in step e and adjustment of random jitter in step g" Add this to the end of bullet c on page 262 as well.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
For task force discussion.

**120G.3.3.4.2 Host stressed input test calibration**

The host stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at TP4a as specified in Table 120G–8.

b) Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–16.

c) Random jitter and bounded uncorrelated jitter are added to the sinusoidal jitter such that the jitter profile of the signal at the pattern generator output approximates $J_{RMS}$ (max) and J4u (max) and complies with the even-odd jitter (max) specification in Table 120F–1.

d) The HCB is plugged into the MCB.

e) The counter-propagating crosstalk signals are calibrated to the differential peak-to-peak voltage and transition time specified in Table 120G–8, measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

f) The reference host channel is configured in the same way as the host PCB in 120G.3.2.2.1 using the parameters in Table 120G–5 for far-end host channel type and the requested mode (short or long).

g) Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-to-peak input voltage tolerance given in Table 120G–7 is not exceeded.

Cl 120G SC 120G.3.3.4.2 P 259 L 4 # 71

Dudek, Mike Marvell

*Comment Type* T *Comment Status* D *HI SI method*

The pattern generator pre-emphasis should be optimized for the host stressed input just as it is for the module stressed input.

*SuggestedRemedy*

Add a sentence to the end of bullet g. "The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used."

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
The additional text proposed in the suggested remedy is warranted. However, comment #9 suggests changes to similar text in 120G.3.4.
With editorial license, implement similar text in 120G.3.3 as modified by comment 9 if it is adopted, otherwise implement the suggested remedy.
For task force discussion.

# HI SI SJ 54

*Cl* **120G** *SC* **120G.3.3.4.2** *P* **258** *L* **36** # **54**

Ran, Adee — Cisco systems

*Comment Type* **T** *Comment Status* **D** *HI SI SJ*

The host stressed input calibration is performed with PRBS13Q and with SJ at 40 MHz (case F of table 162-16). This frequency is not coherent with the PRBS13Q cycle, so the combination of SJ and ISI can create different signal statistics depending on the alignment of the SJ cycle and the PRBS13Q cycle. This can create variability in eye metrics and may require repeated or long measurements.

If the calibration is done with an SJ whose frequency is coherent with the PRBS13Q cycle, data collection can be done with a period which has an integer number of PRBS13Q cycles and integer number of SJ cycles. This can reduce the variability of the calibration. The different frequency would not affect the test which is performed with much longer pattern anyway.

It would be preferable to use a frequency of f_b*6/8191 (approximately 38.915 MHz) instead of 40 MHz during calibration. This would enable more repeatable calibration if the data is collected from an integer multiple of 6 PRBS13Q cycles. The frequency difference should have little effect as the proposed frequency is still far out the reference CRU bandwidth.

Also applies to module stressed input calibration, 120G.3.4.2.2.

*SuggestedRemedy*

Change item b from "Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–16." to:

"Sinusoidal jitter is applied with a frequency of at least 38 MHz and pk-pk amplitude of 0.05 UI."

Add the following informative note after the list:
NOTE—It is recommended to use a sinusoidal jitter frequency which is coherent to the frequency of the PRBS13Q pattern, such as f_b*6/8191 where f_b is the signaling rate of the pattern generator (approximately 38.915 MHz) and calculate eye height and VEC from 6N full cycles of the sinusoidal jitter, where N is an integer.

Apply similar changes in 120G.3.4.2.2.

Implement with editorial license.

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.
The proposed changes are not sufficiently justified by the comment. A coherent or synchronous pattern also prove to result in non-repeatable tests since the arbitrary relative phase of the SJ and the test pattern.
For task force discussion.

### 120G.3.3.4.2 Host stressed input test calibration

The host stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at TP4a as specified in Table 120G–8.

b) Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–16.

c) Random jitter and bounded uncorrelated jitter are added to the sinusoidal jitter such that the jitter profile of the signal at the pattern generator output approximates $J_{RMS}$ (max) and J4u (max) and complies with the even-odd jitter (max) specification in Table 120F–1.

d) The HCB is plugged into the MCB.

e) The counter-propagating crosstalk signals are calibrated to the differential peak-to-peak voltage and transition time specified in Table 120G–8, measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

f) The reference host channel is configured in the same way as the host PCB in 120G.3.2.2.1 using the parameters in Table 120G–5 for far-end host channel type and the requested mode (short or long).

### 120G.3.4.2.2 Module stressed input test calibration

The stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at the input to the frequency-dependent attenuator as specified in Table 120G–10.

b) Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–16.

c) Random jitter and bounded uncorrelated jitter are added to the sinusoidal jitter such that the jitter profile of the signal at the output of the pattern generator approximates $J_{RMS}$ (max) and J4u (max) and complies with the even-odd jitter (max) specification in Table 120F–1.

# HI/MI SI method 122

Cl 120G SC 120G.3.3.4 P 256 L 50 # 122

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *HI/MI SI method*

While we are upturning this section, we might as well do it correctly. 802.3 is not a test spec. There is no requirement to test, only to comply.

*SuggestedRemedy*

Change "The host stressed input tolerance is tested using the test setup described in 120G.3.3.4.1 which is calibrated as described in 120G.3.3.4.2, and the test procedure in 120G.3.3.4.3." to "The host stressed input tolerance is defined by the test procedure in 120G.3.3.4.3 using the test setup described in 120G.3.3.4.1, which is calibrated as described in 120G.3.3.4.2." Similarly in 120G.3.4.2 Module stressed input test.

*Proposed Response* *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
The intent of the suggested remedy is an improvement to the quality of the draft. However, for consistency in the draft the language should be consistent with other clauses. Use similar clause 162.9.4.2 as a template.
Change: "The host stressed input tolerance is tested using the test setup described in 120G.3.3.4.1 which is calibrated as described in 120G.3.3.4.2, and the test procedure in 120G.3.3.4.3."
To: "Host stressed input tolerance is measured according to the procedure described in 120G.3.3.4.1 through 120G.3.3.4.3."
Update 120G.3.4.2 Module stressed input test in a similar way.
Implement with editorial license.

**162.9.4.3 Receiver interference tolerance**

Receiver interference tolerance is measured according to the procedure described in 162.9.4.3.1 through 162.9.4.3.5. Receiver interference tolerance test requirements are specified in Table 162–15.

**120G.3.3.4 Host stressed input test**

The host stressed input tolerance is tested using the test setup described in 120G.3.3.4.1 which is calibrated as described in 120G.3.3.4.2, and the test procedure in 120G.3.3.4.3.

**120G.3.4.2 Module stressed input test**

The module stressed input tolerance is tested using the test setup described in 120G.3.4.2.1 calibrated as described in 120G.3.4.2.2, and the test procedure in 120G.3.4.2.3.

# MI reference channel 36

Cl 120G SC 120G.3.4.2.1 P 261 L 4 # 36

Ran, Adee Cisco systems

*Comment Type* TR *Comment Status* D *MI reference channel*

The test setup includes "Frequency-dependent attenuation representing the host channel" but the frequency dependence is not defined. The only requirement is given in step f of 120G.3.4.2.2 as 18.2 dB at 26.56 GHz - a single frequency. This can be implemented by a notch filter - obviously not what we intend.

The attenuator should be specified across a wide frequency range. The suggested remedy is to use a reference PCB model. Alternatively, a frequency mask can be used.

*SuggestedRemedy*

With editorial license, define the frequency-dependent attenuation based on the PCB model of 162.11.7.1 (as in Annex 163B) with zp=461 mm (value scaled from Annex 163B to create 18.2 dB at 26.5625).

*Proposed Response* *Response Status* W

PROPOSED ACCEPT.

**120G.3.4.2.2 Module stressed input test calibration**

The stressed input signal is calibrated by the following procedure.

...

f) For the low-loss signal calibration, the output of the pattern generator is fed directly to the MCB input (TP1). For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the loss at 26.56 GHz from the output of the pattern generator to TP1a is 18.2 dB. This represents 16 dB channel loss with an additional allowance for host transmitter package loss.

**120G.3.4.2.1 Module stressed input test setup**

The module stressed input test setup is illustrated in Figure 120G–10. The stressed signal is applied at TP1 and is calibrated at TP1a.

The stressed signal includes the following impairments:

— Sinusoidal jitter, random jitter, and bounded uncorrelated jitter

— Frequency-dependent attenuation representing the host channel, which may be implemented with PCB traces. The frequency-dependent attenuation is used only for the high-loss case (see 120G.3.4.2.2).

— Counter-propagating crosstalk signals.

**162.11.7.1 Channel signal and crosstalk path calculations**

The channel paths between TP0 and TP5 used for calculation of the cable assembly COM consist of measured cable assembly signal and crosstalk paths, representative transmitter PCB signal paths, and representative receiver PCB signal paths.

The scattering parameters for a PCB transmission line are calculated using the method defined in 93A.1.2.3 using Equation (93A–13), Equation (93A–14) and the parameter values given in Table 162–19. The PCB trace length parameter $z_p$ has different value for each specific signal path, as specified in 162.11.7.1.1 and 162.11.7.1.2.

The channel path calculations use the function cascade() defined in 93A.1.2.1.

**Table 162–20—PCB model parameters and values**

| Parameter | Value | Units |
|---|---|---|
| $\gamma_0$ | 0 | 1/mm |
| $a_1$ | $3.8206 \times 10^{-4}$ | $ns^{1/2}/mm$ |
| $a_2$ | $9.5909 \times 10^{-5}$ | ns/mm |
| $\tau$ | $5.79 \times 10^{-3}$ | ns/mm |
| $C_0$ | $2.9 \times 10^{-5}$ | nF |
| $C_1$ | $1.9 \times 10^{-5}$ | nF |
| $Z_c$ | 100 | Ω |

# HI/MI pattern table
# 119

*Cl* 120G *SC* 120G.3.1.5 *P* 252 *L* 13 # 119

Dawe, Piers Nvidia

*Comment Type* TR *Comment Status* D *pattern table*

As this annex uses several test patterns like an optical PMD, it should have a table of test patterns giving the pattern number, which this draft lacks, and description, and reference for definition.

*SuggestedRemedy*

Copy Table 167-10, Test patterns, leaving out the rows that don't apply. Refer to the table from elsewhere in the annex to reduce clutter end repetition.

*Proposed Response* *Response Status* W

PROPOSED REJECT.

!! This response was updated on 2021/7/28. !!

Table 167-10 may be found in 802.3db.

It is not clear that the proposed table with pattern numbers will improve the draft all things considered.

It can indeed reduce some clutter for cases where multiple patterns are listed for a particular test step, but not in cases where a single pattern is referenced. It is more convenient to the reader to list the pattern names; the reader would otherwise have to memorize the relationship between pattern numbers and the pattern they represent. The test pattern names line up better with the test equipment controls.

**120G.3.1.5 Host output eye height and vertical eye closure (VEC)**

Figure 120G–6 depicts an example host output eye height and vertical eye closure (VEC) test configuration. Host output eye height and VEC are measured at TP1a using compliance boards defined in 120G.5.3. Eye height and VEC are measured according to the method described in 120G.5.2.

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (see 120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP4 (without the use of a reference receiver) with target differential peak-to-peak voltage of 900 mV and transition time of 8.5 ps.

**167.8.1 Test patterns for optical parameters**

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 167–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 167–11 may be used to perform that test. The test patterns used in this clause are shown in Table 167–10.

**Table 167–10—Test patterns**

| Pattern | Pattern description | Defined in |
|---|---|---|
| Square wave | Square wave (8 threes, 8 zeros) | 120.5.11.2.4 |
| 3 | PRBS31Q | 120.5.11.2.2 |
| 4 | PRBS13Q | 120.5.11.2.1 |
| 5 | Scrambled idle encoded by RS-FEC | 82.2.11 and 91, or 119.2.4.9 |
| 6 | SSPRQ | 120.5.11.2.3 |