Validating C2M VEC and VEO Limits at TP1a/TP4

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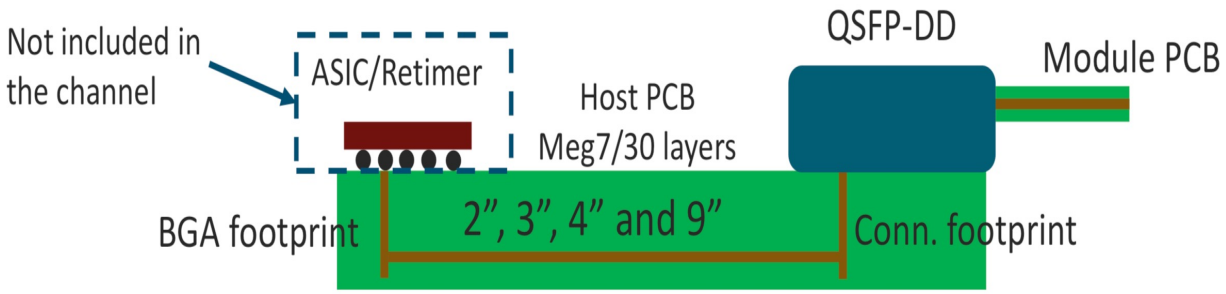
Overview

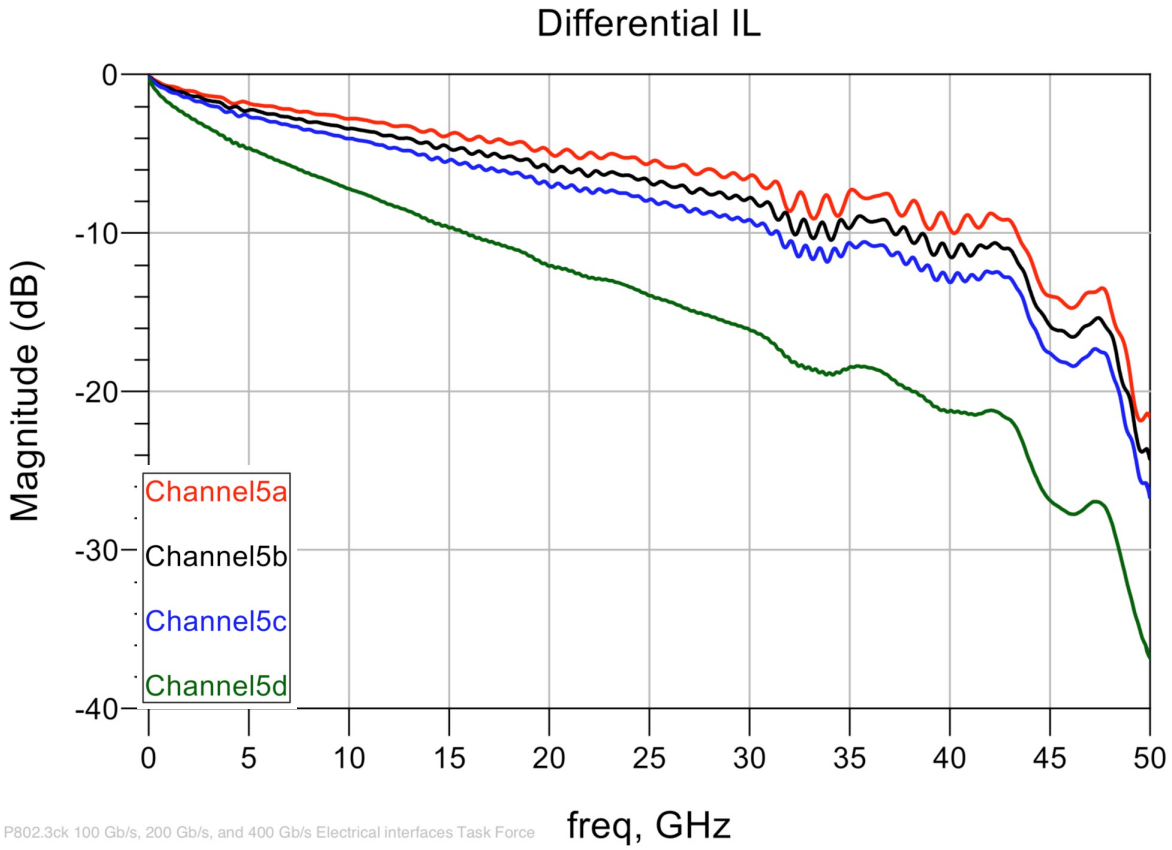
- **Updated analysis with COM 3.2.0 investigate limits at TP1a and TP4**
  - The updated TP1a analysis uses lim_3ck_adhoc_02_073119 channels
  - The updated TP4 nearend and farend analysis based on Yamaichi QSFP56 mated test board with 5 dB loss at Nyquist
- **Addressing D2.1 comments 59, 61, 62, 63, 66, and 68.**

C2M TP1a Channels for Updated Analysis

- **Channel based on lim_3ck_adhoc_02_073119 as shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
  - PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
  - PCB via stub length is modeled as 10 mils
  - Diff pair trace width/spacing is 4.5 mils /8.5 mils
  - ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.



- **This analysis uses min loss channel 5a and max loss channel 5d.**



COM Code 3.2.0 Host-Module TP1a

❑ Test case I/II/III (12, 13, 31 mm) ASIC packages.

Table 93A-1 parameters				
Parameter	**Setting**	**Units**	**Information**	
f_b	53.125	GBd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[1.2e-4 0]	nF	[TX RX]	
L_s	[0.12 0]	nH	[TX RX]	
C_b	[0.3e-4 0]	nF	[TX RX]	
z_p select	[1 2 3]		[test cases to run]	
z_p (TX)	[12 13 30; 1.8 1.8 1.8]	mm	[test cases]	
z_p (NEXT)	[0 0 0 ; 0 0 0]	mm	[test cases]	
z_p (FEXT)	[12 13 30; 1.8 1.8 1.8]	mm	[test cases]	
z_p (RX)	[0 0 0 ; 0 0 0]	mm	[test cases]	
C_p	[0.87e-4 0]	nF	[TX RX]	
R_0	50	Ohm		
R_d	[50 50]	Ohm	[TX RX]	
A_v	0.415	V		
A_fe	0.415	V		
A_ne	0.450	V		
L	4			
M	32	Samp/UI		
samples_for_C2M	100	Samp/UI		
T_O	50	mUI		
AC_CM_RMS	0	V	[test cases]	[0.0235 0.0256]
filter and Eq				
f_r	0.75	*fb		
c(0)	0.54		min	
c(-1)	[-0.2:0.02:0]		[min:step:max]	
c(-2)	[0:0.02:0.1]		[min:step:max]	
c(-3)	[0]		[min:step:max]	
c(1)	[-0.1:0.02:0]		[min:step:max]	
N_b	4	UI		
b_max(1)	**0.4**		**As/dffe1**	
b_max(2..N_b)	**[0.15 0.15 0.1]**		**As/dfe2..N_b**	
b_min(1)	**0.1**		**As/dffe1**	
b_min(2..N_b)	**[-0.15 -0.15 -0.05]**		**As/dfe2..N_b**	
g_DC	[-13:1:-0]	dB	[min:step:max]	
f_z	12.58	GHz		
f_p1	20	GHz		
f_p2	28	GHz		
g_DC_HP	[-3:0.5:0]		[min:step:max]	
f_HP_PZ	1.328125	GHz		
G_Qual	[-2 -9 ;-2 -12; -4 -12;-6 -13]	dB	ranges	
G2_Qual	[0 -1 -2 -3]	dB	ranges	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	12	db
EH_min	10	mV
ERL Pass threshold	7.3	dB
Min_VEO_Test	10	mV
DER_0	0.00001	
T_r	0.0075	ns
FORCE_TR	1	logical
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.594	*Fb
f_f	0.594	GHz f_r specified in first column
f_n	0.594	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	407	mm
z_bp (NEXT)	407	mm
z_bp (FEXT)	407	mm
z_bp (RX)	407	mm
C_0	0	nF
C_1	0	nF
Include PCB	0	logical
new		

COM Code 3.2.0 Module to Host TP4

- **Test case I/II (4, 7 mm) CDR packages.**

Table 93A-1 parameters				
Parameter	**Setting**	**Units**	**Information**	
f_b	53.125	GBd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[1.0e-4 0]	nF	[TX RX]	
L_s	[0.12 0]	nH	[TX RX]	
C_b	[0.3e-4 0]	nF	[TX RX]	
z_p select	[1 2]		[test cases to run]	
z_p (TX)	[4 7; 0 0]	mm	[test cases]	
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]	
z_p (FEXT)	[4 7; 0 0]	mm	[test cases]	
z_p (RX)	[0 0; 0 0]	mm	[test cases]	
C_p	[0.65e-4 0]	nF	[TX RX]	
R_0	50	Ohm		
R_d	[50 50]	Ohm	[TX RX]	
A_v	0.415	V	vp/vf=.694	
A_fe	0.415	V	vp/vf=.694	
A_ne	0.45	V		
L	4			
M	32	Samp/UI		
samples_for_C2M	100	Samp/UI		
T_O	50	mUI		
AC_CM_RMS	[0, 0]	V	[test cases]	[0.0235 0.0256]
filter and Eq				[0.015, 0.015]
f_r	0.75	*fb		[0, 0]
c(0)	0.82		min	
c(-1)	-0.16		[min:step:max]	
c(-2)	0.02		[min:step:max]	
c(-3)	[0]		[min:step:max]	
c(1)	0		[min:step:max]	
N_b	4	UI		
b_max(1)	**0.4**		**As/dffe1**	
b_max(2..N_b)	**[0.15 0.1 0.1]**		**As/dfe2..N_b**	
b_min(1)	**0.1**		**As/dffe1**	
b_min(2..N_b)	**[0.1 -0.15 -0.05]**		**As/dfe2..N_b**	
g_DC	[-5:1:-1]	dB	[min:step:max]	
f_z	12.58	GHz		
f_p1	20	GHz		
f_p2	28	GHz		
g_DC_HP	[-2:0.5:0]		[min:step:max]	
f_HP_PZ	1.328125	GHz		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[2 4 1 3]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	12	db
EH_min	15	mV
ERL Pass threshold	8.5	dB
DER_0	0.00001	
T_r	0.0075	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	400	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.594	*Fb
f_f	0.594	GHz f_r specified in first column
f_n	0.594	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*61*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*61*	mm
z_bp (RX)	*0*	mm
Include PCB	**0**	**logical**

new

upodated for D2.1

COM Analysis on Lim Channel 1 and 4 – ASIC to Module

❑ Results with COM 3.1 and COM 3.2

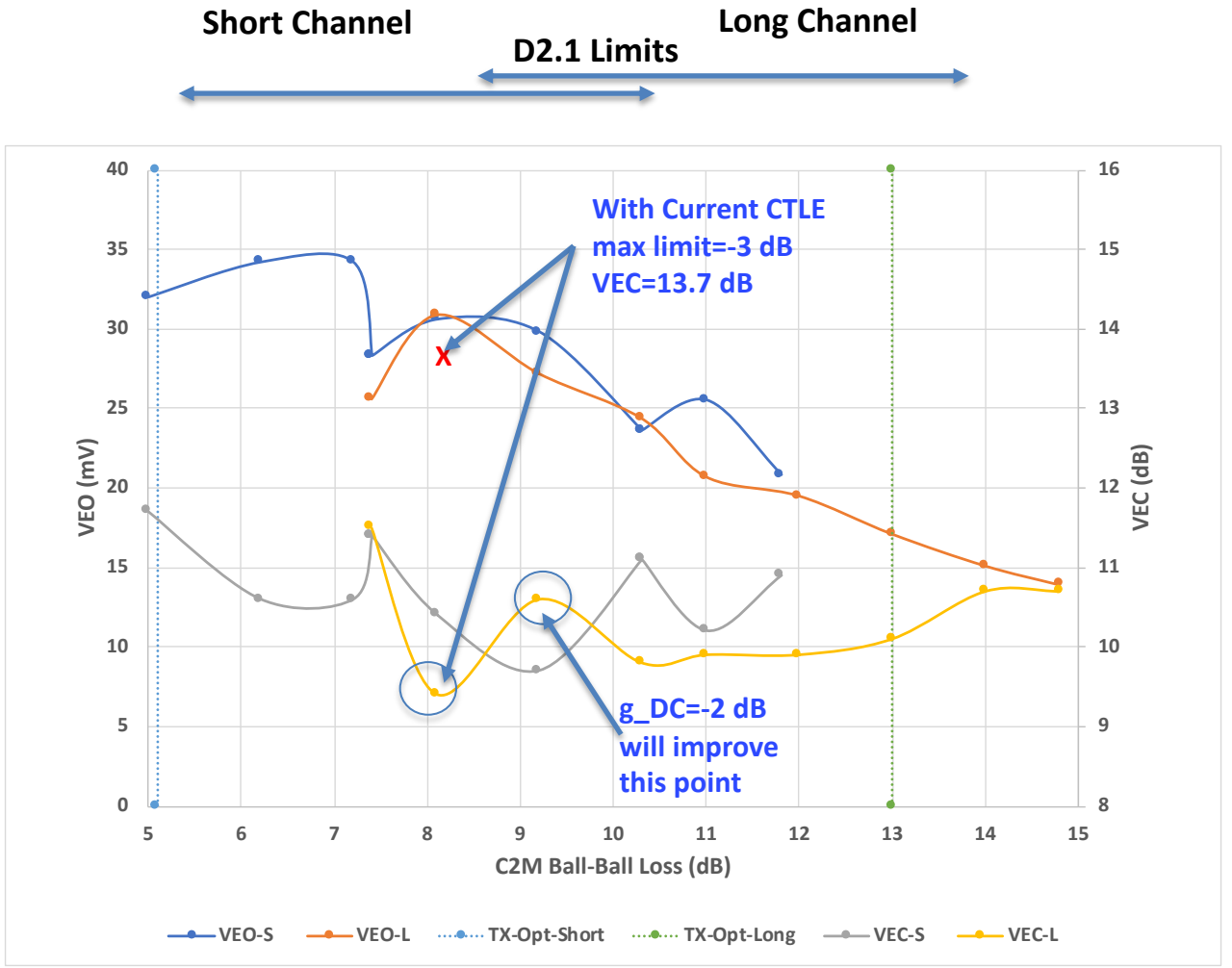
- Generally VEOs are larger with COM 3.2 and VEC is about the same
- Even with improvement on VEO still fails and there is no margin on VEC
- Recommend reducing VEO=9 mV and increasing VEC to 12.5 dB
- What is puzzling why FOM ILD and ICNs are larger?

COM 3.1	Window	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II/III 12/13/31 mm	VEC Case I/II/III 12/13/31 mm	EW Case I/II/III 12/13/31 mm	COM Case I/II/III* 12/13/31 mm
Lim Channel 2" at TP1a ILD = 0.084, ICN = 4.0 mV ERL[11,22]= [9.1, 8.9] dB	0	5.9 dB	11.3 dB	37.5/25.5/27.3	6.8/11.1/7.8	0.19/0.14/0.18	5.3/2.83/4.5
	+/- 50 mUI	5.9 dB	11.3 dB	26.2/13.3/18.7	9.9/16.4/11.1	0.19/0.14/0.18	3.3/1.4/2.8
Lim Channel 9" at TP1a ILD = 0.066, ICN = 1.7 mV ERL[11,22]=[10.9,11.4] dB	0	14.7 dB	20.3 dB	16.7/11.8/12.1	7.2/10/8.1	0.19/0.15/0.17	5.0/3.3/4.3
	+/- 50 mUI	14.7 dB	20.3 dB	11.3/7.1/7.9	10.6/14.4/11.8	0.19/0.15/0.17	2.6/1.8/3.0

COM 3.2	Window	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II/III 12/13/31 mm	VEC Case I/II/III 12/13/31 mm	EW Case I/II/III 12/13/31 mm	COM Case I/II/III* 12/13/31 mm
Lim Channel 2" at TP1a ILD = 0.111, ICN = 4.9 mV ERL[11,22]= [9.1, 8.9] dB	0	5.9 dB	11.3 dB	48.5/12.2/30.7	6.5/12.2/8.6	0.19/0.09/0.17	5.5/2.4/4.0
	+/- 50 mUI	5.9 dB	11.3 dB	32.9/14.0/20.3	9.5/16.5/11.8	0.19/0.13/0.17	3.5/1.4/2.6
Lim Channel 9" at TP1a ILD = 0.087, ICN = 2.0 mV ERL[11,22]=[10.9,11.4] dB	0	14.7 dB	20.3 dB	19.2/14.1/14.6	6.7/9.5/8.1	0.18/0.13/0.15	5.4/3.6/4.3
	+/- 50 mUI	14.7 dB	20.3 dB	13.0/8.1/9.4	10.0/14.4/11.9	0.18/0.14/0.16	3.3/1.8/2.5

M2C Short and Long Channels

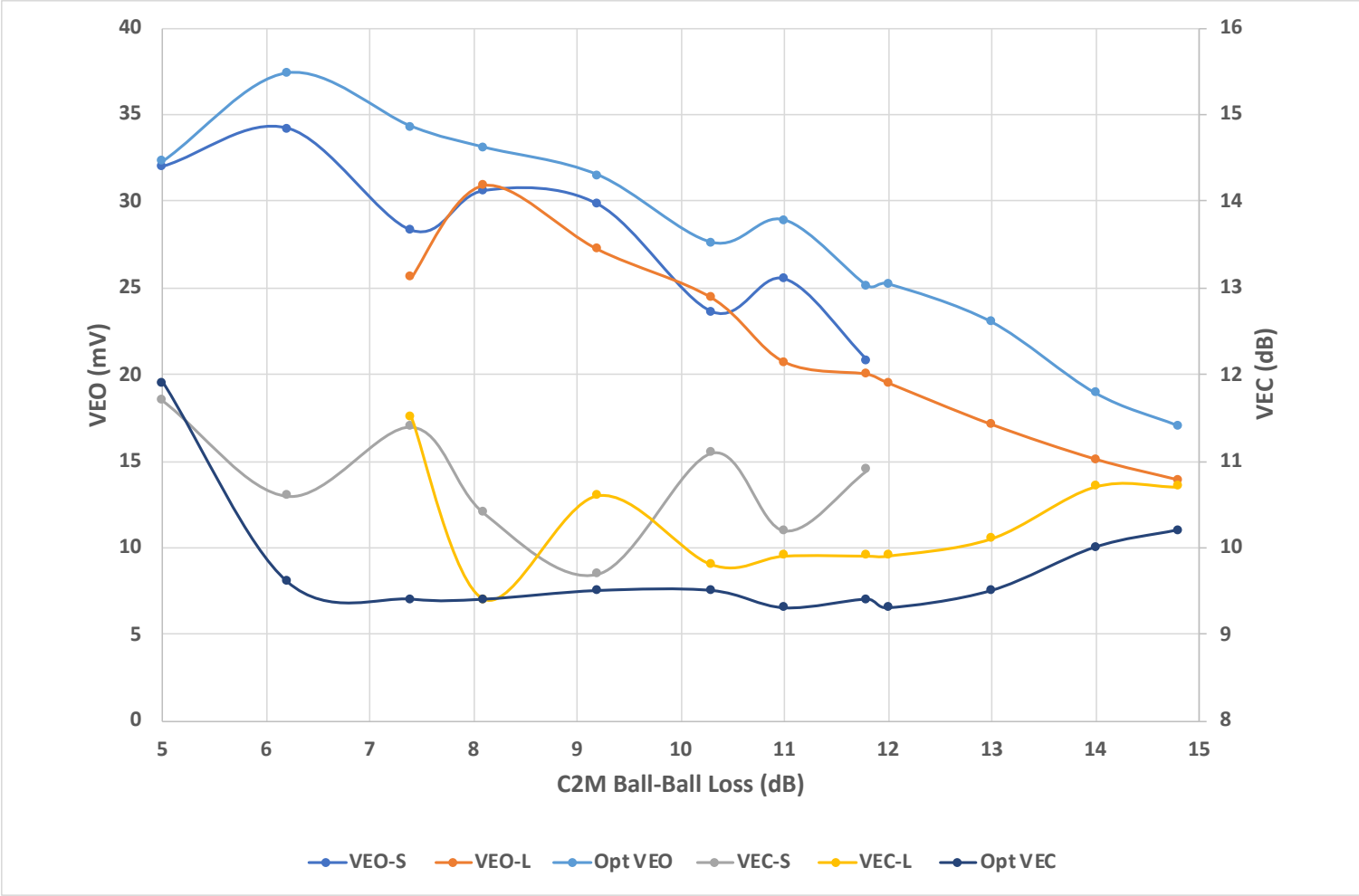
- **Current D2.1 definition of TP4 short and long**
  - Short 0 – 133 mm (5.2 dB) + MTF Loss
  - Long 80 mm (3.1 dB) – 244.7 mm (9.6 dB) + MTF Loss (6.6 dB)
  - VEO=15 mV and VEC=12 dB for short and long
- **Data based**
- **TP4 near end was optimized at module output to meet 12 dB limit**
  - Nearend VEC is higher than VEC farend with max loss a
  - Calvin results indicate similar behavior with farend of VEC=9 dB and Nearend VEC=11.6 dB
- **TP4 long can not be met with current limits**
  - Min CTLE g_DC=-3 dB results in VEC=13.9 dB but reducing g_DC=-2 dB then VEC=9.4 dB
  - Even optimizing TP4 long at 13 dB (204 mm) VEO of 15 mV can't be met
  - Need to reduce VEO long=12.5 mV and g_DC long (max)=-2 dB.



* TX FIR for short channel [0.02 -0.16 0.82 0]
** TX FIR for long channel [0.04 -0.18 0.78 0]

AUI-S/L TX FIR Setting vs Optimum TX FIR

- **Penalty from optimum over AUI-S range**
  - Up to 6 mV in VEO penalty
  - Up to 1.6 dB in VEC penalty
- **Penalty from optimum over AUI-l range**
  - Up to 8.2 mV in VEO penalty
  - Up to 1.1 dB in VEC penalty.



Summary

- **COM 3.2 produces VEO results at TP1a which are ~20% larger than COM 3.1 produced**
  - After ignoring results of 13 mm pathological package COM 3.1 produced 7.9 mV
  - After ignoring results of 13 mm pathological package COM 3.2 produces 9.4 mV
  - VEO still fails for well constructed channel
  - Recommend to reduce VEO=9 mV
- **After reducing g_DC=-1 in D2.1 TP4 nearend can meet VEC=12 dB and VEO=15 mV with single TX FIR**
  - TP4 nearend had to be optimized at MCB output to meet VEO/VEC otherwise it will at min loss
- **Even with COM 3.2 some of the limits TP4 farend if not challenging are failing VEC=12 dB and VEO=15 mV limits**
  - Having difficult meeting with single setting at max loss with 244.7 mm and min loss at 80 mm
  - TP4 farend was optimized at high loss (204 mm) but still coming short meeting VEO=15 mV
  - TP4 farend VEC stays less than 11 dB but running out of signal power recommend reducing VEO=13 mV
  - TP4 farend short end badly fails with current g_DC(min)=- 3dB but reducing g_DC(min)=-2 dB addresses this issue.