802.3ck D2.2 Comment Resolution Annex 120G (C2M)

Matt Brown, Huawei, P802.3ck Editor-In-Chief

120G channel IL 48

Cl 120G SC 120G.4.1 P 276 L 14 # 48

Ran, Adee Cisco

Comment Type T *Comment Status* D *channel IL*

"For correct operation, the actual differential-mode to differential-mode insertion loss could be higher or lower than that given by Equation (120G–3) due to the channel ILD, return loss, and crosstalk"

This sentence is meaningless as written, and not helpful for readers, whatever the intended meaning is.

Looking at 83E, there was no such statement; the insertion loss that was provided in Equation (83E-1) was described as "typical application" with no attempt to make it even a recommendation. 120E changed it to a recommendation but did not add the quoted statement either.

This seems like a statement from the days when channels were specified by insertion loss limits, and that was a poor specification. We have no ground for making Equation 120G-3 anything other than a recommendation; and as such it does not need any disclaimers.

SuggestedRemedy

Delete the quoted sentence.

Proposed Response *Response Status* W

PROPOSED REJECT.
It is not clear what value the reference sentence has, however there may have been some sound logic for including it.
For task force discussion.

120G.4 Channel characteristics

120G.4.1 Channel differential-mode to differential-mode insertion loss (informative)

The channel differential-mode to differential-mode insertion loss is expected to be equal to or less than Equation (120G–3), which is illustrated in Figure 120G–12. For correct operation, the actual differential-mode to differential-mode insertion loss could be higher or lower than that given by Equation (120G–3) due to the channel ILD, return loss, and crosstalk. Note that for this equation the differential-mode to differential-mode insertion loss at the Nyquist frequency is less than or equal to 16 dB. The differential-mode to differential-mode insertion loss budget is illustrated in Figure 120G–2.

$$ILdd(f) \le \begin{cases} 0.05 + 1.8\sqrt{f} + 0.2513f & 0.01 \le f \le 26.56 \\ -12.4181 + 1.07f & 26.56 < f \le 40 \end{cases} \quad \text{(120G–3)}$$

where

ILdd(f) is the channel differential-mode to differential-mode insertion loss in dB

f is the frequency in GHz

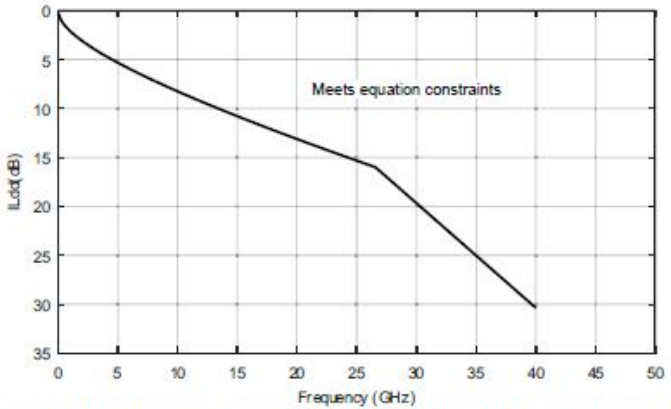

Figure 120G–12—Recommended channel differential-mode to differential-mode insertion loss

120G EO mask, part 1
Comments 95, 101

Cl 120G *SC* 120G.5.2 *P* 279 *L* 43 # 95

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *EO mask*

The Gaussian weighting has the effect of destroying the histogram width, allowing bad fast eyes to pass, while giving the impression that the histogram width still applies. With a weighting standard deviation of 0.02 UI, the eye height is measured at around +/-0.03 UI rather than the +/-0.05 UI in the previous draft. Compare 120E with ESMW of 0.2 or 0.22 UI.

SuggestedRemedy

Remove the Gaussian weighting and set the eye height and VEC limits (which need revision anyway) appropriately.

Proposed Response *Response Status* W

PROPOSED REJECT.
The current method of determining eye height and VEC using a weighted window was introduced in D2.2 based on approved D2.1 comment #39. A final straw poll indicated acceptance of the response with a ratio (yes:no) of 21:11.
For task force discussion.

Cl 120G *SC* 120G.5.2 *P* 279 *L* 6 # 101

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *EO mask*

This draft has a weighted rectangular eye mask spec with mask height = max(EHmin, EA/VECmax) and effective mask width ~2x0.03 UI, although it is described as a histogram 2x0.05 UI wide. Measuring a diamond eye with a rectangular mask provides weak and uncertain protection against too much jitter; de-weighting the sides of the histogram weakens it further; the effective BER criterion is hard to establish but seems to be around 1e-4, not 1e-5 as intended.
We need an eye mask that's more eye shaped, so that a higher proportion of the samples near the boundary are measured at full weight and contribute properly to the measurement. Eye mask measurement with a 10-sided mask has been pre-programmed into scopes for about 20 years, we should use established tools and methods where they work well.

SuggestedRemedy

Change from a 4-cornered weighted mask with corners at t = ts+/-0.05, V = y +/-H/2 to a 10-cornered unweighted mask with corners at t = ts+/-1/16, ts+/-0.05, ts+/-3/32, V = y +/-H/2, k +/-H*0.4, y. y is near VCmid, VCupp or VClow (vertically floating, as in D2.2).
H is max(EHmin, Eye Amplitude * 10^(-VECmax/20)). Eye Amplitude is AVupp, AVmid or AVlow, as in D2.2.
This simple scalable method can remain as the EH and VEC limits are revised.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.1 comment #106 and D2.0 comment #180 for which there was no consensus to make the proposed changes.
No new evidence or consensus has been provided.

120G EO mask, part 2
Comments 95, 101

D2.0 comment #180

Cl 120G *SC* 120G.5.2 *P* 253 *L* 23 # 180

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *EH/VEC method*

This draft has a primitive rectangular eye mask (H = either EHmin or EA/VECmax), although it is described as a histogram. It's an inefficient/inaccurate way of measuring a signal quality vertically and provides weak and uncertain protection against too much jitter. This is worse with the higher VEC limit in the latest draft that allows worse and more varied signals, and is a particular concern for very short host channels (see Mike Dudek's work) that can have faster edges than higher loss ones.

SuggestedRemedy

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = k +/-H/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-1/16, ts+/-3/32, V = k +/-H/2, k +/-H*0.4, k. k is VCmid, VCupp or VClow.
In case it's not clear, H is either EHmin or Eye Amplitude * 10^(-VECmax/20).
This simple scalable method can remain as the EH and VEC limits are revised. Scopes have been measuring with 10-sided masks for many years, it's not more difficult than a rectangular mask.

Response *Response Status* U

REJECT.
The currently methodology was chosen over an eye mask method like that being proposed in this comment.
See slide 3 of the following presentation was reviewed by the task force:
https://www.ieee802.org/3/ck/public/21_01/brown_3ck_04_0121.pdf
The comment does not provide sufficient justification to support the proposed changes.

D2.1 comment #106

Cl 120G *SC* 120G.5.2 *P* 266 *L* 23 # 106

Dawe, Piers Nvidia

Comment Type TR *Comment Status* A *EO method*

This draft has a primitive rectangular eye mask spec with mask height = max(EHmin, EA/VECmax) and mask width = 0.1 UI, although it is described as a histogram. Measuring a diamond eye with a rectangular mask is an inefficient, inaccurate way of measuring signal quality and provides weak and uncertain protection against too much jitter. Its effective width is less than its actual because of the 1e-5 probability criterion and the inefficient shape.
De-weighting the sides of the histogram/mask would make this worse, equivalent to increasing the target BER by 10x or so. A higher VEC / smaller EH limit with the rectangular mask would allow more jittered and more varied signals, particularly for very short host channels (see Mike Dudek's work) that can have faster edges than higher loss ones. The target BER is not going to change.
We need an eye mask that's more eye shaped, so that a higher proportion of the samples are near the boundary and contribute to the measurement.

SuggestedRemedy

Change from a 4-cornered mask with corners at t = ts+/-0.05, V = y +/-H/2 to a 10-cornered mask with corners at t = ts+/-0.05, ts+/-1/16, ts+/-3/32, V = y +/-H/2, k +/-H*0.4, y. y is near VCmid, VCupp or VClow (vertically floating, as in D2.1).
H is max(EHmin, Eye Amplitude * 10^(-VECmax/20)). Eye Amplitude is AVupp, AVmid or AVlow, as in D2.1.
This simple scalable method can remain as the EH and VEC limits are revised. Scopes have been measuring with 10-sided masks for many years, it's not more difficult than a rectangular mask and gives better results.

Response *Response Status* U

error: #127 should have been #180

ACCEPT IN PRINCIPLE.

This comment is a restatement of D2.0 comment #127, which was rejected on the basis of insufficient justification and insufficient analysis to show equivalent or better interoperability.

Straw polls 5, 6, and 7 indicate there is no consesus to make the proposed change. However, the resolution to comment #39 addresses the concern expressed in this comment.

120G EO mask, part 3
Comments 95, 101

Cl 120G SC 120G.5.2 P 266 L 25 # 39

Ran, Adee Cisco systems

Comment Type TR *Comment Status* A *EO method*

As has been reported in calvin_3ck_adhoc_01_063021, the authors have been "unable to reliably close the calibration loop on TP1a at 12.5dB VEC with precision lab equipment" for insertion loss of 16.4 dB. This suggests that the VEC specification may be unfeasible.

Allowing a higher (worse) VEC for transmitters (host/module outputs) might pass bad receivers with very closed eyes, which will put more burden on receivers (even if the signal in stressed input test does not change, receivers will have to work with transmitters that have the same VEC due to other reasons, e.g. a "rectangular eye" closed by high noise that can't be equalized, rather than ISI).

Instead of lowering the VEC bar for transmitters, we should look at the definition of VEC and make it more suitable to the expected eye shape of good transmitters after processing with the reference receiver (this shape is not rectangular), taking into account the expected behavior of real receivers.

The calculation of VEC and EH from a CDF accumulated over ts ± 0.05 UI gives the same weight to all phases. This makes sense if the receiver's phase is distributed uniformly in this window; it supposedly makes sense it we don't know where the receiver will sample within this region and account for sampling error. But the eye is not independent of the receiver - it is shaped by the receiver's equalization, and in the reference receiver we assume a certain behavior.

A receiver is expected to optimize its equalization (CTLE+DFE or equivalent) at the sampling point ts - this is part of the measurement procedure (currently steps k and l) - which would result in the maximum vertical opening being at ts. We should assume the average sampling phase is then ts; any difference between the optimized phase and the average phase is an implementation penalty that should be covered by the minimum EH.

A real receiver's CDR does not have a uniform phase distribution around its mean; the probability of sampling at either -0.05 UI or +0.05 UI from ts is smaller than the probability of sampling closer to ts. The rare events where the sample is taken far from ts contribute less to the average BER, so they should be weighted down in the calculation of the CDFs. Having equal weights as in the current method is overly pessimistic in both EH and VEC.

It is therefore proposed to apply a weighting function to the sampled data based on the phase.

SuggestedRemedy

A detailed proposal will be provided in a presentation.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.1 and D2.0 or the unsatisfied negative comments from the initial ballot.

Hence it is not within the scope of the recirculation ballot.

The following presentation analyzed the effect of the currently specified measurement method. A similar analysis is required to make any changes.
Https://www.ieee802.org/3/ck/public/20_10/healey_3ck_01a_1020.pdf

The following presentation was reviewed by the task force:
https://www.ieee802.org/3/ck/public/21_07/ran_3ck_01a_0721.pdf

Per straw polls 5, 6, and 7 there was consensus to implement the proposal in ran_01a (slide 9) with sigma_r set to 0.02 UI.

Implement the method in ran_01a (slide 9) with sigma_r set to 0.02 UI.

Straw poll #5 (chicago rules) direction
Straw poll #6 (pick one) direction
For the eye opening method in 120G.5.2 I would support:
A: a weighted method similar to comment #39 and ran_01a
B: a multi-sided eye mask similar to comment #106
C: no change
D: need more information
#5: A: 25 B: 15 C: 13 D: 11
#6: A: 15 B: 8 C: 11 D: 5

Straw poll #7 (decision)
I support resolving comment #39 using the proposal in ran_01a (slide 9) except with standard deviation (sigma_r) of 0.02 UI.
Yes: 21
No: 11

D2.1 comment #39

120G EO method 104

Cl 120G	*SC* 120G.5.2	*P* 277	*L* 17	# 104

Dawe, Piers — Nvidia

Comment Type T *Comment Status* D *EO method*

This needs explanation/correction/deletion: "Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured." For a histogram, it should be the expectation of number of bad samples in the histogram / total number of samples "in the histogram". In conventional eye mask terminology, hit ratios are hits in a keepout region / number of samples, assumed evenly distributed across 1 UI (see 86.8.3.2.1). Anyway, are there any probabilities outside eye height / VEC, which is covered later in this subclause and is indeed done per sample not per symbol.

SuggestedRemedy

Delete the sentence.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
It is not clear what value the reference sentence has, however there may have been some sound logic for including it.
For task force discussion.

120G.5.2 Eye opening measurement method

The eye opening parameters eye height and vertical eye closure are measured with the effect of a reference receiver which includes receiver input referred noise, a continuous-time filter as defined in 93A.1.4.3, a receiver noise filter as defined in 93A.1.4.1, and a decision-feedback equalizer as defined in 93A.1.6, using the parameters specified in Table 120G–12. All parameters in Table 120G–12 apply to TP1a, TP4 far-end, and TP4 near-end unless indicated otherwise. The pattern used for output eye diagram measurements is PRBS13Q. Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured. Eye height and vertical eye closure parameters are defined by the following procedure.

The referenced sentence was imported from 120E, when some of the method was localized instead of referring to 120E, as a resolution to D1.1 comment #137.

120E.4.2 Eye width and eye height measurement method

Eye diagrams in 200GAUI-4 and 400GAUI-8 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is PRBS13Q. Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured. The following procedure should be used to obtain the eye height and eye width parameters, as illustrated by Figure 120E–13:

Given that the procedure is now quite explicit how the CDF is calculated from the samples, it seems that the reference sentence is not relevant.

already in $y_{TX}(k)$.

h) Compute Vmid, Vupp, Vlow, VCmid, VCupp, VClow from the eye diagram using 120E.4.2 steps 4) through 6) with the exception that the CDF of the signal voltage is calculated from the set of voltage samples within the time interval $t_2 \pm 0.05$ UI and with accumulated probability for each sample weighted by the function $w(t)$ defined by Equation (120G–4). As an example, UPPCDF1 may be calculated using Equation (120G–6) from a set of N samples $\{v_i, t_i\}$.

i) The eye height is the minimum of Vmid, Vupp, and Vlow.

120G MI SI calibration, part 1
72, 131, dudek_01

Cl 120G SC 120G.3.4.3.2 P 274 L 17 # 72

Dudek, Mike — Marvell

Comment Type TR *Comment Status* D *MI SI calibration*

The optimum value of CTLE peaking (gdc+gdc2) when calibrating the high loss stressed module receiver test is only 10.5dB. See Dudek_3ck_01_0921. Requiring at least 13dB is degrading the signal making it difficult to generate the signal (see e.g. Snapshot of Receiver Module Input Tests (no convergence on high-loss TP1a channel) and private discussions). Note also that the maximum allowed peaking for testing the host output should not be significantly different from this value. A presentation will be made.

SuggestedRemedy

Change -13dB to -10.5dB. Also in Table 120G-11 change the gdc values for TP1a range for -1<GDC2 <0 to -2 to -11,
the range for -2<GDC2 <-1 to -4 to -10, and
the range for -3<GDC2 <-2 to -4 to -9

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
Comment #131 proposes changes to the wording to the text referenced in this comment.
The following related presentation was provided for review…
https://www.ieee802.org/3/ck/public/21_09/dudek_3ck_01_0921.pdf
Implement the suggested remedy.
For task force discussion.

Cl 120G SC 120G.3.4.3.2 P 274 L 17 # 131

Dawe, Piers — Nvidia

Comment Type T *Comment Status* D *MI SI calibration*

This is open to misinterpretation: "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case." Even the previous text, "The CTLE setting, gDC+gDC2, has to be less than or equal to -13 dB" was misinterpreted to mean that there is no constraint on gDC + gDC2 for the low loss case. Yet the limits for the appropriate test point in Table 120G-11 still apply.
Actually, for a stressed signal calibration, we are looking for a signal where the optimum CTLE setting obeys the rules (so that the signal is not low stress but outside the expected range, but right stress and in the expected range).
See another comment for whether -13 dB is the right value.

SuggestedRemedy

Change "Eye height and VEC are measured at TP1a as described in 120G.5.2." to "Eye height and VEC are measured at TP1a as described in 120G.5.2, with an additional constraint for the high-loss case: the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to -13 dB."
Delete "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case."

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
Comment #72 proposes to change the limit on the CTLE peaking gain.
Change "Eye height and VEC are measured at TP1a as described in 120G.5.2." to "Eye height and VEC are measured at TP1a as described in 120G.5.2 with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to -13 dB."
Delete "For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to -13 dB. This restriction does not apply for the low-loss case."

g) Eye height and VEC are measured at TP1a as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–10. The differential peak-to-peak input voltage tolerance given in Table 120G–9 is not exceeded. For the high-loss case, the reference receiver CTLE is limited to settings where $g_{DC} + g_{DC2}$ is less than or equal to –13 dB. This restriction does not apply for the low-loss case. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

The result of the combined proposed responses would be as follows:

Eye height and VEC are measured at TP1a as described in 120G.5.2 with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to -13 dB. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–10. The differential peak-to- peak input voltage tolerance given in Table 120G–9 is not exceeded. For the high-loss case, the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to ~~–13~~10.5 dB. ~~This restriction does not apply for the low-loss case. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.~~

120G EO RR bbmax/g_DC
100, 98, 99, 115

Cl 120G SC 120G.5.2 P 277 L 32 # 100

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *EO RR bbmax*

My recent simulations don't use gDC as strong as the table allows, but occasionally, the first DFE tap hits the limit of 0.4

SuggestedRemedy

Increase bbmax(1) from 0.4 to 0.5, increase the minimum for gDC at TP1a and TP4 long far end.

Proposed Response *Response Status* W

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

The comment provides only annecdotal evidence.

For task force discussion.

Revised response:

<out of scope boilerplate>

The comment provides only anecdotal evidence. The suggested remedy does not provide alternate value(s) for the minimum g_DC.

The comment does not provide sufficient evidence to support the proposed changes nor does the suggested remedy provide sufficient detail to implement.

Table 120G–11—Eye opening reference receiver parameter values *(continued)*

Parameter	Symbol	Value	Units
Continuous time filter, pole frequencies	f_{p1} f_{p2}	20 28	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	f_b / 40	GHz
Decision feedback equalizer (DFE) length	N_b	4	UI
Normalized DFE coefficient maximum limit $n = 1$ $n = 2$ $n = 3$ or 4	$bb_{max}(n)$	 0.4 0.15 0.1	 — — —
Normalized DFE coefficient minimum limit $n = 1$ $n = 2$ $n = 3$ or 4	$bb_{min}(n)$	 0.1 –0.15 –0.05	 — — —
One-sided noise spectral density	η_0	4.1×10^{-8}	V^2/GHz

This comment relates to the reference receiver used for VEC/EH measurements at both TP1a (host output) and TP4 (module output).

It seems to be requesting that bb_max(1) be set to 0.5 for all test scenarios. It is also requesting increasing minimum g_DC for TP1a and TP4 long-mode but provides no values.

120G EO RR bbmax/g_DC 100, 98, 99, 115

Cl 120G SC 120G.5.2 P 277 L 38 # 98

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *EO RR gdc*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes. Obviously, different channels will need different CTLE settings. Obviously, CTLE settings that only signals outside what the spec is designed for use, should be excluded, to make implementers set up their product correctly.

SuggestedRemedy

Create separate limits for TP4 short and long output modes, so 4 sets for TP4+, in the style of TP1a. If you don't have any better numbers, create them anyway with the same numbers in each set - but see another comment.

Proposed Response *Response Status* W

PROPOSED REJECT.

This comment is a restatement of D2.1 comment #103 and D2.0 comment #183, which were rejected on the basis of providing insufficient justification and detail.

This comment provides expanded justification, but the suggested remedy does not provide sufficient detail to implement.

D2.0 comment #183

Cl 120G SC 120G.5.2 P 252 L 16 # 183

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *RR CTLE*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes.

SuggestedRemedy

Create separate limits for TP4 short and long output modes.

Response *Response Status* U

REJECT.

The comment does not provide sufficient justification to support any changes and the suggested remedy does not provide sufficient detail to implement.

D2.1 comment #103

Cl 120G SC 120G.5.2 P 265 L 16 # 103

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *RR gdc*

The limits for TP4 gDC, gDC2 should not be the same for short and long output modes.

SuggestedRemedy

Create separate limits for TP4 short and long output modes, so 4 sets for TP4+, in the style of TP1a.

Response *Response Status* U

REJECT.

This comment is a restatement of D2.0 comment #179, which was rejected on the basis of insufficient justification and detail. It adds request to provide 4 sets of values in the style used for TP1a but does not provide specific values. No further justification is provided.

The comment does not provide sufficient justification for the proposed changes nor does the suggested remedy provide sufficient detail to implement.

120G EO RR bbmax/g_DC 100, 98, 99, 115

Cl 120G SC 120G.5.2 P 277 L 46 # 99

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *EO RR gdc*

As a lot of the channel for TP4 far-end is known exactly and the max loss to TP4 far end is less than to TP1a, the range of gDC, gDC2 combinations should be a subset of the TP1a ones.

SuggestedRemedy

For Continuous time filter, DC gain for TP4 far-end (gDC), change to sets of limits that depend on gDC2 in the same style as for TP1a. The allowed values should be subsets of those for TP1a. For TP4 long far end, use minimum gDC 1 dB higher than allowed for TP1a; for TP4 short far end, 3 dB higher than for TP1a.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.1 comment #104 and D2.0 comment #178, which were rejected on the basis of providing insufficient justification and detail.
This comment provides no new justification, but does provide more details for implementation.

D2.0 comment #178

Cl 120G SC 120G.5.2 P 252 L 25 # 178

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *RR CTLE*

As a lot of the channel for TP4 far-end is known exactly, one would expect that a known subset of gDC, gDC2 combinations would be the only candidates to try. As for TP1a, I believe the strongest gDC and gDC2 should add to a constant.

SuggestedRemedy

For Continuous time filter, DC gain for TP4 far-end (gDC), change to a set of limits that depend on gDC2 in the same style as for TP1a, with the strongest gDC and gDC2 adding to a constant. The allowed values should be a subset of those for TP1a.

Response *Response Status* U

REJECT.

The comment does not provide sufficient justification to support any changes and the suggested remedy does not provide sufficient detail to implement.

D2.1 comment #104

Cl 120G SC 120G.5.2 P 265 L 25 # 104

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *RR gdc*

As a lot of the channel for TP4 far-end is known exactly and the max loss to TP4 far end is less than to TP1a, the range of gDC, gDC2 combinations should be a subset of the TP1a ones. As for TP1a, I believe the strongest gDC and gDC2 should add to a constant.

SuggestedRemedy

For Continuous time filter, DC gain for TP4 far-end (gDC), change to a set of limits that depend on gDC2 in the same style as for TP1a, with the strongest gDC and gDC2 adding to a constant. The allowed values should be a subset of those for TP1a.

Response *Response Status* U

REJECT.
This comment is a restatement of D2.0 comment #178, which was rejected on the basis of insufficient justification and detail. No further justification or implementation detail is provided.
The comment does not provide sufficient justification for the proposed changes nor does the suggested remedy provide sufficient detail to implement.

120G EO RR bbmax/g_DC
100, 98, 99, 115

Cl **120G** *SC* **120G.5.2** *P* **277** *L* **29** # 115

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **D** *EO RR gdc*

In D2.1, max gDC for TP4 near-end was increased from -2 to -1. While hosts typically have bigger packages and more trace loss than modules, neither is required (e.g. an on-board repeater).

SuggestedRemedy

Consider if max gDC for TP1a should be increased similarly.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The comment does not provide sufficient justification to implement the proposed changes nor does the suggested remedy provide sufficient detail to implement.

120G HO/MO output swing, part 1
37, 38, 96,150

Cl 120G SC 120G.3.1 P 261 L 3 # 37

Ran, Adee Cisco

Comment Type TR *Comment Status* D *HO output swing (CC)*

Following up on unsatisfied comment #37 against D2.1:

As demonstrated in https://www.ieee802.org/3/ck/public/21_07/ran_3ck_04b_0721.pdf, the differential peak to peak specification measured with PRBS13Q is broken, especially for host output, because the result is strongly dependent on the host channel and equalization applied.

Since the proposal to define/measure this parameter with other patterns was not accepted, this comment proposes a new specification, based on PRBS13Q, to verify that the output swing is not too high. Namely, v_f using the linear fit procedure, similar to 162.9.3.1.2, with the exception that the transmitter equalization is not specified (it is whatever the host sets it to).

v_f represents the asymptote of the (linear) step response of the transmitter, including any equalization applied. It can be used to predict the effect of arbitrarily long runs which are not present in PRBS13Q itself.

The suggested limit corresponds to Vdiffptp of 900 mV which was the assumed value for the host in all earlier C2M specifications. This limit may be somewhat too high but changing it is a different topic.

SuggestedRemedy

Add a row to Table 120G–1 with Parameter: Steady-state voltage v_f (max), Reference: 120G.5.4, Value: 450, Units: mV.

Add subclause 120G.5.4 with the following text:
120G.5.4 Steady-state voltage
The steady-state voltage v_f is defined as the sum of the linear fit pulse p(1) through p(M×Nv) divided by M with the specific equalization used by the transmitter. Nv is set equal to Np. The linear fit procedure for obtaining p and the values of M and Np are defined in 162.9.3.1.1.

Proposed Response *Response Status* W

PROPOSED REJECT.
Comment #38 suggests conditionally reducing the limit to 300 mV.
The following related presentation was provided for consideration:
https://www.ieee802.org/3/ck/public/adhoc/sept22_21/kochuparambil_3ck_adhoc_01_092221.pdf
The proposed solution requires consideration by the task force.
For task force review.

Cl 120G SC 120G.3.1 P 261 L 3 # 38

Ran, Adee Cisco

Comment Type TR *Comment Status* D *HO output swing (CC)*

The host output differential peak-to-peak voltage is defined at TP1a so it is close to what a module input will have. The limit of 870 mV is too high for modern module host-side receivers which may used low-voltage CMOS processes. The reference CTLE is fully linear but real CTLEs may become nonlinear with such large signals and it may messs with its adaptation and CDR functionality and create much worse BER than what the reference receiver predicts.

Note that the module output "short" setting, which assumes a low-loss host channel (such that the receiver is close to the measurement point TP4), has a differential peak to peak limit of 600 mV.

SuggestedRemedy

Change the value of Differential peak-to-peak output voltage (max) with transmitter enabled from 870 to 600 mV.

In addition, if the steady-state voltage specification is added (subject of another comment), set the limit of that specification to 300 mV.

Proposed Response *Response Status* W

PROPOSED REJECT.
Comment #150 proposes an alternate solution.
The referenced comment regarding steady-state voltage is comment #37.
The proposed solution requires consideration by the task force.
For task force review.

The following presentation relating to comments 37, 38, and 150 was previously reviewed.
https://www.ieee802.org/3/ck/public/adhoc/sept22_21/kochuparambil_3ck_adhoc_01_092221.pdf

120G HO/MO output swing, part 2
37, 38, 96,150

Cl 120G SC 120G.3.1 P 261 L 16 # 150

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HO output swing (CC)*

We under-estimated the pattern dependency on Vpkpk

SuggestedRemedy

Reduce 870 mV to 800 mV

Proposed Response *Response Status* W

PROPOSED REJECT.
Comment #38 proposes an alternate solution.
The proposed solution requires consideration by the task force.
For task force review.

Cl 120G SC 120G.3.2 P 264 L 10 # 96

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *MO DPPV value*

For module output, the differential peak-to-peak output voltage (envelope) is weakly pattern dependent, predictably so because the loss to the observation point (TP4) is moderate and mostly known. The spec is clear and unambiguous and not broken because it tells the reader which pattern applies. The envelope at a "long mode" host IC would be lower than at TP4. However, it may be that we intended that the envelope at TP4 in service should be 900 mV, which I believe was the intention in other VSR-like specs.

SuggestedRemedy

If so, reduce the "900" in Table 120G-3 by ~4% to 845.

Proposed Response *Response Status* W

PROPOSED REJECT.
The proposed solution requires consideration by the task force.
For task force review.

120G MO/MI DC CM voltage, part 1
94, 9

Cl 120G SC 120G.3.2 P 264 L # 94

Dawe, Piers
Nvidia

Comment Type TR *Comment Status* D *MO/MI DC CM voltage*

There used to be a footnote under the table: "DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.", as in OIF VSR, and annexes 83E and 120E. That note told the reader how the system worked, and told him why these numbers aren't the same as in Table 120G-1, and everyone could get oin with earning their living. Now, there is a gratuitous, silly "DC common-mode voltage tolerance" spec row, which fussy customers will ask to see satisfied with a test report. If a module uses traditional capacitors, that's pointless. Notice that there is no equivalent spec in 162.11 Cable assembly characteristics (nor in annexes 83E and 120E).

SuggestedRemedy

Restore the DC common-mode voltage rows to the way they were and reinstate the table footnote. Delete 120G.3.2.4. Similarly in Table 120G-9, and delete 20G.3.4.5.

Proposed Response *Response Status* W

PROPOSED REJECT.
The information in the footnotes was not lost as it was moved to subclauses 120G.3.2.4 and 120G.3.4.5. The specifications as previously written had the implication as currently specified but required some extrapolation to come to that realization. The specifications as they were previously written were ambiguous. The assumption that there will be AC-coupling capacitors on the module is circular, since the specified common-mode voltages may force the use of a capacitor.

Cl 120G SC 120G.3.4.5 P 276 L 5 # 9

Brown, Matt
Huawei

Comment Type T *Comment Status* D *MO DC CM voltage*

The term "ground offset voltage" is not defined.

SuggestedRemedy

Provide explanation for what is meant by "ground offset voltage".

Proposed Response *Response Status* W

PROPOSED REJECT.
Adding an explanation as requested would be an improvement to the draft, however the suggested remedy does not provide sufficient detail to implement.

120G MO/MI DC CM voltage, part 2
94, 9

From Draft 2.2 (current) ...

Table 120G–3—Module output characteristics at TP4

DC common-mode voltage tolerance (range) Upper limit Lower limit	120G.3.2.4	 2.85 -0.35	 V V

[a]The signaling rate range is derived from the PMD receiver input.

120G.3.2.4 Module output common-mode voltage tolerance

DC common-mode voltage is generated by the host. A module shall meet all output specifications with any DC common-mode voltage (see 120G.5.1), as measured at TP4, within the range specified in Table 120G–3.

NOTE—The specified voltages allow for the effects of ground offset voltage.

Table 120G–9—Module input characteristics

DC common-mode voltage tolerance (range) Upper limit Lower limit	120G.3.4.5	TP1	 2.85 -0.35	 V V

[a] Meets BER specified in 120G.1.1.

120G.3.4.5 Module input common-mode voltage tolerance

DC common-mode voltage is generated by the host. A module shall meet all input specifications with any DC common-mode voltage (see 120G.5.1), as measured at TP1, within the range specified in Table 120G–9.

NOTE—The specified voltages allow for the effects of ground offset voltage.

From Draft 2.1...

Table 120G–3—Module output characteristics (at TP4)

DC common-mode voltage (min)[b]	120G.5.1	–350	mV
DC common-mode voltage (max)[a]	120G.5.1	2850	mV

[a]The signaling rate range is derived from the PMD receiver input.
[b]DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Table 120G–9—Module input characteristics

DC common-mode voltage (min)[b]	120G.5.1	TP1	–350	mV
DC common-mode voltage (max)[b]	120G.5.1	TP1	2850	mV

[a] Meets BER specified in 120G.1.1.
[b] DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

120G MO EH 93

Cl 120G SC 120G.3.2 P 264 L 11 # 93

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *MO EH*

If the eye height limit is the same at long near end as at long far end, there is huge margin at near end and the implementer is encouraged to optimise for far end or beyond, only limited by the NE VEC spec, while we want modules to be set up consistently, for the full range from near to far. EH is naturally larger at NE than FE for a well set up output and the spec should reflect that. Host designers know their own loss and medium-loss hosts can take advantage of a better signal that cost the module nothing.

SuggestedRemedy

Change the eye height, long near end, so that it is 3 dB above long far end, e.g. 15 mV (far) and 21 mV (near) if long far is not changed. 3 dB is about half the loss from long near end to long far end, so long far end remains the harder one to meet.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.1 comment #98, for which there was no consensus to make the proposed changes.
The intent of specifications is to enforce what is necessary not what is possible. However, as this comment states, a long-mode might be able to take advantage of the extra eye height.
For task force discussion.

Table 120G–3—Module output characteristics at TP4

Parameter	Reference	Value	Units
Signaling rate, each lane (nominal)		53.125[a]	GBd
AC common-mode output voltage (max, RMS)	120G.5.1	25	mV
Differential peak-to-peak output voltage (max) Short mode Long mode	120G.5.1	 600 900	 mV mV
Eye height (min)	120G.3.2.2	15	mV
Vertical eye closure, VEC (max)	120G.3.2.2	12	dB

Cl 120G SC 120G.3.2 P 253 L 11 # 98

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *MO VEC/EH*

If the eye height limit is the same at long near end as at long far end, there is huge margin at near end and the implementer is encouraged to optimise for far end or beyond, only limited by the NE VEC spec, while we want modules to be set up consistently, for the full range from near to far. EH is naturally larger at NE for a well set up output.

SuggestedRemedy

Increase the eye height, long mode near end, by 3 dB from 15 mV to 21 mV

Response *Response Status* U

REJECT.

This comment pertains to the module output eye height (min) for long mode, near end.

The comment does not provide sufficient evidence that the proposed change is necessary.

The comment relates to module output eye height (min).

The comment proposes that for the long mode near-end measurement only, the eye height requirement be increased to 21 mV, resulting in:

Eye height (min)
short mode, near end and far end: 15 mV (no change)
long mode far end: 15 mV (no change)
long mode near-end: 21 mV (new value)

120G MO reference host channel 97(R)

Cl 120G SC 120G.3.2.2.1 P 265 L 46 # 97

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *MO SI channel*

The near end and far end should be placed far enough apart so that the module implementer has little choice what emphasis to use, so that all modules are set up similarly. As short is easier than long, this means that far minus near (mm or dB) for short should be more than far minus near for long. As real host channels are not exactly like the theoretical reference host channel and host makers hate avoidable precision, measurement and record-keeping, there should be a healthy overlap of short and long to give the host room for its implementation. D2.0's 160 mm delivered on both these criteria, D2.1's 133 mm doesn't.

SuggestedRemedy

Change 133 to 150, change 80 to 90

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.1 comment #102 for which there was no consensus to make the proposed changes.
No further convincing justification is provided with this comment.

Revised response:

PROPOSED REJECT.
This comment is a restatement of D2.1 comment #102 for which there was no consensus to make a change. However, the response notes that there may be some benefit to explore this further.
However, no further analysis or significant additional justification has been provided.

D2.1 comment #102

Cl 120G SC 120G.3.2.2.1 P 254 L 51 # 102

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *MO SI host reference channel*

The near end and far end should be placed far enough apart so that the module implementer has little choice what emphasis to use, so that all modules are set up similarly. As short is easier than long, this means that far minus near (mm or dB) for short should be at least as much as far minus near for long. As real host channels are not exactly like the theoretical reference host channel, there should be a healthy overlap of short and long to give the host room for its implementation. D2.0's 160 mm delivered on both these criteria, D2.1's 133 mm doesn't.

SuggestedRemedy

Change 133 to 150, change 80 to 90

Response *Response Status* U

REJECT.

The comment does not provide sufficient justification for the proposed changes.

There may be some benefit to balancing the length range between short and long modes. Further analysis is encouraged.

120G.3.2.2.1 Near-end and far-end eye measurement methodology

The signal measured at TP4 is first convolved with a reference host channel. The reference host channel is the host receiver printed circuit board (PCB) signal path $S^{(HOSPR)}$ defined in 162.11.7.1.1 with the exceptions that the length z_p for each test is provided in Table 120G–5, and C_0 and C_1 are both 0 nF. The eye height and VEC are measured using the method in 120G.5.2.

Table 120G–5—PCB length for module output measurements

Module output mode	Host channel type	PCB length, z_p (mm)
Short	near-end	0
Short	far-end	133
Long	near-end	80
Long	far-end	244.7

120G MI SI FDA, part 1
8,15, 110

Cl 120G SC 120G.3.4.3.2 P 273 L 54 # 8

Brown, Matt Huawei

Comment Type T *Comment Status* D *MI SI FDA*

In D2.2 a precise definition of the target insertion loss for the frequency dependent attenuator was added. However, the frequency range over which to "match" the real channel is not specified.

SuggestedRemedy

Specify the frequency range over which the the frequency dependent attenuator must approximate the target insertion loss.
Perhaps 0.01 to 40 GHz.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy and remove the editor's note.

Cl 120G SC 120G.3.4.3.2 P 274 L 9 # 15

Lusted, Kent Intel Corporation

Comment Type ER *Comment Status* D *MI SI FDA (bucket1)*

There is an editor's note to be removed in the next draft, pending changes to the Z_p value and the frequency range.

SuggestedRemedy

Resolve the value of z_p and adjust the frequency range as necessary

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #8.

Cl 120G SC 120G.3.4.3.2 P 275 L 14 # 110

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *MI SI FDA*

The formula and target exist at all frequencies. The loss board consists of PCB and good grade microwave connectors. We should not be encouraging implementers to do a bad job above 40 GHz. It's a target, there is no spec on how "approximate" is good enough.

SuggestedRemedy

Graph the target up to the signalling rate as done in Figure 163B-1, delete the editor's note on the previous page.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #8.

Comment #8 proposes the constraint is from 0.1 GHz to 40 GHz.

Comme #110 proposes no frequency range for constraint, but suggests graphing up to the signaling rate (53.125 GHz).

References:

KR/C2C test fixture is constrained up to 26.5625 GHz.

KR channel recommended ILdd is constrained from 0.01 to 40 GHz.

C2C channel recommended ILdd is constrained from 0.01 to 53.125 GHz.

KR/C2C example test fixture provides exemplary s-parameters. The resulting ILdd is plotted out to 53.125 GHz.

120G MI SI FDA, part 2
8,15, 110

120G.3.4.3.2 Module stressed input test calibration

f) For the low-loss signal calibration, the output of the pattern generator is fed directly to the MCB input (TP1). For the high-loss signal calibration, the frequency-dependent attenuator is configured such that the scattering parameters approximate those calculated from Equation (93A–13) and Equation (93A–14) using z_p = 464 mm in length and the parameter values given in Table 162–20, representing *ILdd* from the output of the pattern generator to TP1a of 18.2 dB at 26.56 GHz. This represents 16 dB channel loss with an additional allowance for host transmitter package loss. The *ILdd* of the target scattering parameters is illustrated in Figure 120G–11.

Editor's note (to be removed in next draft): The value of z_p was adjusted from 461 mm as proposed in D2.1 comment #39 to 464 mm to obtain 18.2 dB at 26.56 GHz. Also, the frequency range was not specified the comment, so ILdd curve in Figure 120G–11 was plotted arbitrarily to 40 GHz.

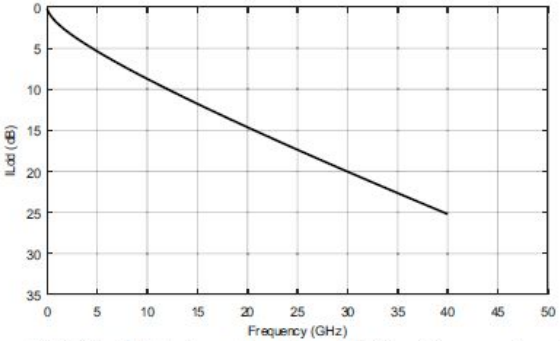

Figure 120G–11—Module stressed input target high-loss frequency-dependent attenuator differential-mode to differential-mode insertion loss

163.9.2.1.1 Test fixture insertion loss

The insertion loss of the test fixture shall be between 1.7 and 5 dB at 26.56 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.2 dB from 0.05 to 26.56 GHz. Insertion loss deviation is calculated as specified in 93A.4, where T_t is 0.01 ns, and f_b and f_r values are taken from Table 163–10.

163B.2 Characteristics

This example test fixture is defined using the PCB trace model in 162.11.7.1, with z_p = 71 mm, and parameter values in Table 162–19, with the exception that C_0 and C_1 are both 0. This results in a TP0 to TP0a insertion loss of 2.8 dB at 26.5625 GHz. The reference values are calculated for the transmitter characteristics of Clause 163. The reference transmitter device and package model uses the parameter values T_r = 7.5 ps, $f_r = 0.75 \times f_b$ = 39.8438 GHz, z_p = 31 mm, and A_v = 0.413 V. The values of v_{peak} and γ are calculated with f_b = 53.125 GBd and N_v = 200.

The insertion loss of the example test fixture is approximated by Equation (163–1) which is illustrated in Figure 163B–1.

$$IL(f) = 0.074 + 0.2104\sqrt{f} + 0.0674f \qquad 0.05 \le f \le 53.125 \qquad (163B\text{–}1)$$

where

$IL(f)$ is the insertion loss at frequency f in dB

f is the frequency in GHz

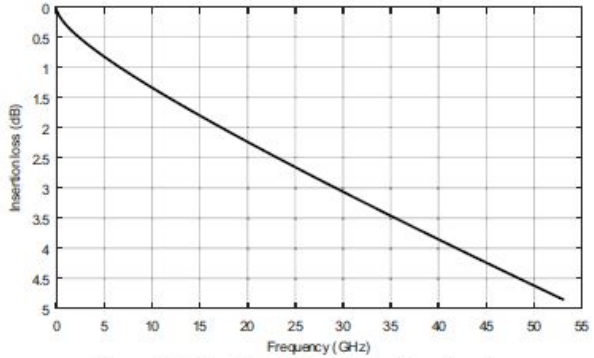

Figure 163B–1—Example test fixture insertion loss

120G MI SI FDA, part 3
8,15, 110

163.10.2 Channel insertion loss

The maximum recommended insertion loss of the channel is given by Equation (163–4).

$$IL(f) \le \begin{cases} 0.693 + 2.161\sqrt{f} + 0.607f & 0.01 \le f \le 26.5625 \\ -19.12 + 1.773f & 26.5625 < f \le 40 \end{cases} \quad (163\text{–}4)$$

where

$IL(f)$ is the insertion loss in dB at frequency f

f is the frequency in GHz

The insertion loss limit is illustrated by Figure 163–6.

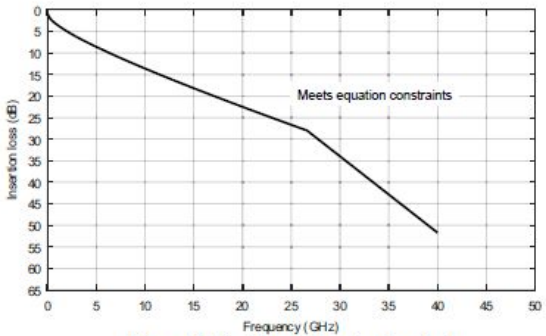

Figure 163–6—Channel insertion loss limit

120F.4.2 Channel insertion loss (informative)

The channel insertion loss should be equal to or less than Equation (120F–2). Actual channel loss could be higher or lower than that given by Equation (120F–2) due to the channel ILD, return loss, and crosstalk. Note that for this equation the channel loss at the Nyquist frequency is less than or equal to 20 dB.

$$Insertion\_loss(f) \le 1.083 + 1.444\sqrt{f} + 0.432f \quad \text{(dB)} \quad \text{for } 0.01 \le f \le 53.125 \quad (120\text{F–}2)$$

where

f is the frequency in GHz

$Insertion\_loss(f)$ is the informative C2C insertion loss

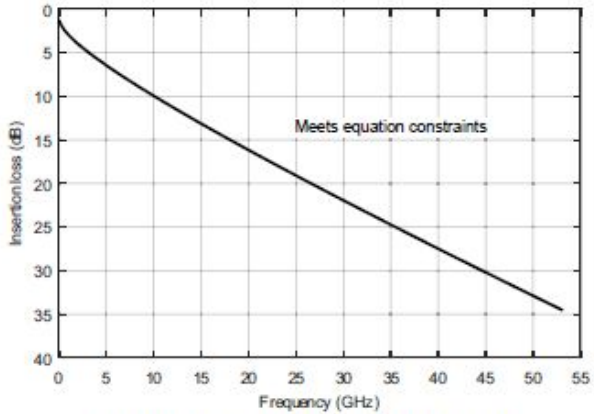

Figure 120F–5—Channel insertion loss limit

120G HI SI method
128

Cl 120G SC 120G.3.3.5.2 P 270 L 3 # 128

Dawe, Piers Nvidia

Comment Type E *Comment Status* D *HI SI method*

"transition time ... at TP4a", "jitter profile of the signal at the pattern generator output". These are the same place apart from the DC block, and if that makes a difference it would be better to calibrate after it. Also 120G.3.5.2.2 says "at the output of the pattern generator" (words in a different order, so a search won't find both).

SuggestedRemedy

Change "at the pattern generator output" to "at Tp4a".

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
The comment does not provide sufficient justification to support the proposed change. Note also that the proposed change is technical, not editorial.
For task force discussion.

c) Random jitter and bounded uncorrelated jitter are added to the sinusoidal jitter such that the jitter profile of the signal at the pattern generator output approximates J_{RMS} (max) and J4u (max) and complies with the even-odd jitter (max) specification in Table 120F–1. These are initial jitter values that will be modified by the addition of crosstalk in step e and adjustment of random jitter in step g.

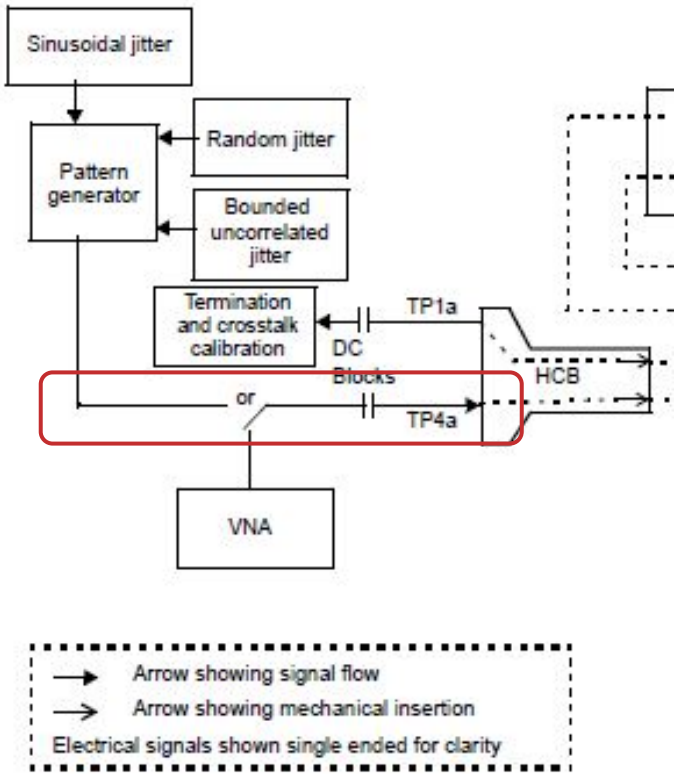

Figure 120G–9—Example host st

120G HI SI method 130

CI 120G SC 120G.3.3.5.2 P 270 L 19 # 130

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

If "differential peak-to-peak voltage" is supposed to convey the idea that the MSB and LSB are not adjusted separately as in 120E.3.3.2.1 and D2.0, it doesn't do it. Also, differential peak-to-peak voltage is limited at TP4, not the PG.

SuggestedRemedy

Change "differential peak-to-peak voltage are adjusted" to "amplitude are adjusted".
Change "voltage tolerance given" to "voltage tolerance at TP4 given".
See another comment against p268 line 45 about introducing the pattern generator.
Similarly in 120G.3.4.3.2 step g.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
The other comment referenced in the suggested remedy is comment #118.
The amplitude rather than the DPPV is adjusted, so a change in wording may be warranted here.
The label in Table 120G-7 is "Differential peak-to-peak input voltage tolerance" without "at TP4", although TP4 is shown in the test point column. There is no ambiguity with the reference as written. No changes in this regard is warranted.
For task force discussion.

Table 120G–7—Host input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, each lane (range)	120G.3.3.1	TP4a	53.125 ± 100 ppm	GBd
Differential peak-to-peak input voltage tolerance (min) for short mode for long mode	120G.5.1	TP4	 600 900	mV

120G.3.3.5.2 Host stressed input test calibration

g) Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-to-peak input voltage tolerance given in Table 120G–7 is not exceeded. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

The sentence constraining the voltage tolerance is poorly written even with the proposed changes. The paragraph might be rewritten as follows:

Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and ~~differential peak-to-peak voltage~~ amplitude are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-to-peak voltage measured at TP4 does not exceed the differential peak-to-peak input voltage tolerance given in Table 120G–7 ~~is not exceeded~~. The pattern generator preemphasis and reference receiver settings that minimize VEC are used.

120G.3.4.3.1 Module stressed input test setup

g) Eye height and VEC are measured at TP1a as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–10. The differential peak-to-peak input voltage tolerance given in Table 120G–9 is not exceeded. For the high-loss case, the reference receiver CTLE is limited to settings where $g_{DC} + g_{DC2}$ is less than or equal to –13 dB. This restriction does not apply for the low-loss case. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

120G HI SI method (preemphasis adjustment) 7

Cl 120G SC 120G.3.3.5.2 P 270 L 19 # 7

Brown, Matt Huawei

Comment Type T *Comment Status* D *HI SI method*

In item g, the adjustment of jitter, voltage, and equalization to minimize VEC are iterative, but this is not clear in the description.

SuggestedRemedy

Update the description to reflect the interative nature. Update item g in 120G.3.4.3.2 in a similar way.

Proposed Response *Response Status* W

PROPOSED REJECT.
While addressing D2.1 comment #9, there was some agreement that the text should be updated to address the concerns expressed in this comment, however sufficient detail was not provided at that time. However, the suggested remedy for this comment does not provide sufficient detail to implement.

g) Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-to-peak input voltage tolerance given in Table 120G–7 is not exceeded. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

The comment might be resolved using the following modifications to the text:

Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted, , while the pattern generator preemphasis and reference receiver settings are adjusted to minimize VEC, so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-topeak input voltage tolerance given in Table 120G–7 is not exceeded. ~~The pattern generator preemphasis and reference receiver settings that minimize VEC are used.~~

120G HI SI method (crosstalk pattern)
45

Cl 120G SC 120G.3.3.5.2 P 270 L 11 # 45

Ran, Adee Cisco

Comment Type T *Comment Status* D *HI SI method*

"If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane"

This sentence seems out of place after the calibration of the crosstalk signal transition time. Also it's unclear why 31 UI are required with a PRBS13Q.

Looking back at the corresponding text in 83E where this requirement was inherited from, it refers to PRBS31, and appears in reference to the effect of the crosstalk signals on the stress signal, not to the calibration of the crosstalk signal.

It seems that this text should refer to PRBS31Q after the crosstalk calibration is complete, to ensure that the different crosstalk sources are not in-phase (and appear uncorrelated).

This comment also applies to 120G.3.4.3.2 (module stressed input).

SuggestedRemedy

Move the quoted sentence to the end of the paragraph (item e) and change "PRBS13Q" to "PRBS31Q".

Implement similarly in 120G.3.4.3.2.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
The way this procedure step is written PRBS13Q is a candidate pattern for the crosstalk signals, while allowing replacement with other patterns, including PRBS31Q, once calibration using PRBS13Q is complete. The minimum pattern offset of 31 might be also be intended to provide some time separation between PAM4 symbols taking ISI into account. However, a similar consideration for PRBS31Q might be warranted.
Delete:
"If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane."
Insert the following sentence at the end of item e:
"If the PRBS13Q or PRBS31Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q or PRBS31Q patterns on one lane and any other lane."

e) The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

The amended text would be as follows:

The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. ~~If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane.~~ The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration. If the PRBS13Q or PRBS31Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane.

120G HI SI method (crosstalk pattern)
46

Cl 120G SC 120G.3.3.5.2 P 270 L 13 # 46

Ran, Adee Cisco

Comment Type TR *Comment Status* D *HI SI method*

"The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration."

The "may" in this sentence means that the pattern may also _not_ be changed, so PRBS13Q can be used as the crosstalk pattern for EH/VEC calibration. But PRBS13Q is not a representative signal and the crosstalk it creates may be different from the other signals (which have wider spectrum). This gives room for undesired variability in test conditions.

Looking back at the corresponding text in 83E, it has "The pattern is changed", not optionally "may be changed".

This comment also applies to 120G.3.4.3.2 (module stressed input).

SuggestedRemedy

In the quoted sentence, change "may be" to "is", and change "for amplitude calibration" to "for amplitude and stressed signal calibration".

Implement similarly in 120G.3.4.3.2.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
Since the crosstalk response passes very little low frequency (e.g., less than 1 GHz) signal, PRBS13Q should be sufficient as the pattern for a crosstalk signal and thus is a relevant candidate pattern.
The comment does not provide sufficient justification for the proposed changes.

e) The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

120G HI SI method
121

Cl 120G SC 120G.3.3.5.2 P 270 L 13 # 121

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

This sentence used to say "The pattern may be changed to a valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration and the stressed input test". The same sentence was used for host stressed input calibration with target amplitude and transition time, and module stressed input calibration with target amplitude and slew time. It wasn't as clear as it could have been: crosstalk pattern or victim pattern? Amplitude calibration of crosstalk or victim? I believe it meant that the crosstalk pattern could be changed to a long one when calibrating the eye height of the victim. CEI 16.3.10.3.1 says "The crosstalk signal is calibrated at TP4 or TP1a using a QPRBS13-CEI pattern, then the pattern is changed to QPRBS31-CEI for the test".

SuggestedRemedy

Change "The pattern" to "The crosstalk pattern", change "amplitude calibration" to "stressed signal eye height and VEC calibration". Also in 120G.3.4.2.2 step e.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed changes are an improvement to the draft.
Implement the suggested remedy with editorial license.

120G.3.3.5.2 Host stressed input test calibration

e) The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

The amended text in 120G.3.3.5.2 would be as follows:

The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The crosstalk pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11 and 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for ~~amplitude~~ stressed signal eye height and VEC calibration.

120G.3.4.3.2 Module stressed input test calibration

e) The counter-propagating crosstalk signals are calibrated at TP4 using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–10. The crosstalk signal transition time is calibrated with a PRBS13Q pattern. If the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane. The pattern may be changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11, 119.2.4.9), or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R signal for amplitude calibration.

120G HI SI method
112

Cl 120G SC 120G.3.4.3.2 P 273 L 34 # 112

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *HI SI method*

"as X as possible" is bad language in a standard or any kind of spec. How hard is the reader supposed to try? No expense spared!? This isn't a moonshot, what we ask for has to be achievable at a reasonable cost. I know in this case, the cost of getting to the differential peak-to-peak input voltage tolerance should not be a problem, but avoid bad language.

SuggestedRemedy

Change "The initial signal level is set as high as possible without exceeding the differential peak-to-peak input voltage tolerance given in Table 120G-9" to "The initial signal level does not exceed the differential peak-to-peak input voltage tolerance given in Table 120G-9, but may be set at the high end of the range for jitter calibration". Similarly in 120G.3.3.5.2.

Proposed Response *Response Status* W

PROPOSED REJECT.
The proposed changes do not improve the quality of the draft.

120G.3.4.3.2 Module stressed input test calibration

The stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at the input to the frequency-dependent attenuator as specified in Table 120G–10. The initial signal level is set as high as possible without exceeding the differential peak-to-peak input voltage tolerance given in Table 120G–9.

b) Sinusoidal jitter is applied with frequency and amplitude per case F in Table 162–16.

120G HI SI method (near end)
120

CI 120G SC 120G.3.3.5.1 P 269 L 12 # 120

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

short or long mode far-end

SuggestedRemedy

short or long mode far-end test or long mode near-end test

Proposed Response *Response Status* W

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

The comment does not provide any justification to support the proposed changes.

As written, the text requests that regardless of whether the host requests long mode or short mode, only the far end test is required.

For task force discussion.

The measurement receiver used for test calibration includes:

— clock recovery unit (CRU) that acts as a high-pass jitter filter with a 3 dB corner frequency of 4 MHz and a slope of 20 dB/decade,

— reference host channel to be configured for short or long mode far-end test as specified in 120G.3.2.2.1, and

— a reference receiver as specified in 120G.5.2.

120G HI SI method (near end)
123

Cl 120G SC 120G.3.3.5.2 P 270 L 17 # 123

Dawe, Piers Nvidia

Comment Type E *Comment Status* D *HI SI method*

"parameters in Table 120G–5 for far-end host channel type and the requested mode": but in one case, the near end needs a parameter from the table

SuggestedRemedy

parameters in Table 120G–5 for host channel type and the requested module output mode

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
The stressed input tolerance test is defined using only the far-end reference host channels, so only the far end parameters are required.

f) The reference host channel is configured in the same way as the host PCB in 120G.3.2.2.1 using the parameters in Table 120G–5 for far-end host channel type and the requested mode (short or long).

120G HI SI method
148

Cl 120G	*SC* 120G.3.3.5.2	*P* 270	*L* 22	# 148

Dawe, Piers — Nvidia

Comment Type TR *Comment Status* D *HI SI method*

The host stressed input signal is emulating a module so must obey the same rules. VEC and eye height must be in spec for both near end and far end. The signal should be adjusted to minimise VEC for both, or possibly to minimise VEC for far end while keeping in spec at near end. The eye height should match the target at far end and be graeter at near end.

SuggestedRemedy

This procedure needs road-testing before the draft can be said to be "without technical issues". In the meantime, add text to the draft to explain more fully what the procedure is.

Proposed Response *Response Status* W

PROPOSED REJECT.

Item g) instructs that the eye height of the smallest eye match the target value in Table 120G-8. Table 120G-8 provides only one value to be used for both near-end and far-end measurements.

Item g) instructs that VEC is within the limits in Table 120G-8. Table 120G-8 provide only one range (with maximum and minimum) to be used for both near-end and far-end measurements.

The module output specifications for eye height and VEC are the same for near-end and far-end.

There is no need for testing the host input with different target values and ranges for near-end and far-end.

g) Eye height and VEC are measured at TP4 as described in 120G.5.2. The pattern generator random jitter and differential peak-to-peak voltage are adjusted so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–8. The differential peak-to-peak input voltage tolerance given in Table 120G–7 is not exceeded. The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used.

120G HI SI method
125

Cl 120G SC 120G.3.3.5.3 P 270 L 48 # 125

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

This says that "the pattern generator is set ... with sinusoidal jitter for each case in Table 162-16" then the HCB is detached from the MCB, implying that all SJ cases are used together (as one might for a TV receiver that must receive one channel while all others are active).
Editorial: detached and plugged are an odd pair.

SuggestedRemedy

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence. The HCB is unplugged from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above. The sinusoidal jitter is stepped through the six cases in Table 162-16.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
Implement the suggested remedy.

The amended text would be as follows (option 1):

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence~~, with sinusoidal jitter for each case in Table 162–16~~. The HCB is ~~detached~~ unplugged from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above. The sinusoidal jitter is stepped through the six cases in Table 162-16.

Alternately (option 2)…

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence~~, with sinusoidal jitter for each case in Table 162–16~~. The HCB is ~~detached~~ unplugged from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above. The test is repeated with sinusoidal jitter set to each of the six cases in Table 162-16.

120G.3.3.5.3 Host stressed input test procedure

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, with sinusoidal jitter for each case in Table 162–16. The HCB is detached from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above.

120G HI SI method (BER) 126

120G.3.3.5.3 Host stressed input test procedure

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, with sinusoidal jitter for each case in Table 162–16. The HCB is detached from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above.

If the test is performed with PRBS31Q, the host BER may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits. The host BER is the average of the BER of each of its lanes.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the host BER may be calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

The number of received bits may be estimated based on the test time.

Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results.

120E.3.3.2.1 Host stressed input test procedure

If the test is performed with pattern 3, the host BER may be calculated using the host's PMA test pattern checker (see 120.5.11.2.2). If the test is performed with pattern 5 or a valid 200GBASE-R/400GBASE-R signal, the BER may be calculated using the host's PCS Reed-Solomon decoder error counters (see 119.3.1), as the number of FEC symbol errors divided by the number of received bits. The number of received bits may be estimated based on the test time.

Cl 120G *SC* 120G.3.3.5.3 *P* 270 *L* 50 # 126

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

There's a problem with identifying which lanes are relevant. For "The host electrical output is enabled on all lanes with any of the patterns above", this is to include realistic crosstalk so it could include all 8 transmit lanes of a QSFP-DD, or maybe all the output lanes on the host if it makes a difference. While for "The host BER is the average of the BER of each of its lanes", only the lanes in the PMA (AUI) under test (1, 2 or 4 lanes) are relevant. "Module BER" in 120G.3.4.2.3 is even more open to misinterpretation because we are so clear how many lanes a module has. But, terminology for this has been set up: the term "interface BER" occurs 19 times in section 6, and is defined in 86.8.2.1, 86.8.4.7, 86.8.4.8, 95.8.1.1...

SuggestedRemedy

Change paragraph to:
The relevant BER is the interface BER, which is the average of the BER of each of the lanes in the AUI under test.
If the test is performed with PRBS31Q, the BER of a PMA lane may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits.
If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the interface BER may be calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.
Similarly in 120G.3.4.2.3.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
The term "interface BER" is used exclusively in Clause 86 and Clause 95 and is related to optical PMDs. The term "host BER" is used in Annex 120E which specifies the 200GAUI-4 and 400GAUI-8, which are a more relevant to 120G.
However, it doesn't make sense to use multiple terms for essentially the same thing.
Implement the suggested remedy with editorial license.
For task force discussion.

120G HI SI method (BER) 127

CI 120G SC 120G.3.3.5.3 P 271 L 7 # 127

Dawe, Piers Nvidia

Comment Type E *Comment Status* D *HI SI method*

"Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results" - more wordy than needed for something that shouldn't need saying each time.

SuggestedRemedy

Other methods of extracting the received bit pattern and counting errors may be used if they generate equivalent results.
Also in 120G.3.4.2.3.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not the scope of the recirculation ballot.
The proposed changes do not improve the quality of the draft.

120G.3.3.5.3 Host stressed input test procedure

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, with sinusoidal jitter for each case in Table 162–16. The HCB is detached from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above.

If the test is performed with PRBS31Q, the host BER may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits. The host BER is the average of the BER of each of its lanes.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the host BER may be calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

The number of received bits may be estimated based on the test time.

Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results.

120G.3.4.3.3 Module stressed input test procedure

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, with sinusoidal jitter for each case in Table 162–16. The HCB is detached from the MCB and the module under test is plugged into the MCB. The module electrical output is enabled on all lanes with any of the patterns above.

If the test is performed with PRBS31Q, the module BER may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits. The module BER is the average of the BER of each of its lanes.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, or 400GBASE-R sequence, the module BER may be calculated by placing the module under test into local loopback (see 120.5.9) and feeding the module output into a compliant host or its equivalent. The module BER is calculated using the host FEC decoder error counters (see 91.6 and 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

The number of received bits may be estimated based on the test time.

Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results.

120G HI/MI SI PG EQ [56, 66, 67, 132]

Cl 120G SC 120G.3.3.5.2 P 270 L 21 # 56

Ran, Adee Cisco

Comment Type TR *Comment Status* D *HI/MI SI PG EQ*

(CC - Host stressed input and Module stressed input)

The term "pattern generator pre-emphasis" is used in both procedures without any definition, and does not appear anywhere else. Furthermore, it is stated that the "settings that minimize VEC are used". But it is not stated from which set of settings the minimum is taken.

Pattern generators used to create the stressed input signal may be able to apply arbitrarily long FFEs for "pre-emphasis". Consider the following two cases:
1. An FFE that optimizes the signal (e.g., zero-forces the ISI) after the test channel and the reference RX with some CTLE setting (there is a different FFE for each CTLE setting even without any DFE)
2. An FFE that similarly optimizes the signal at the slicer of a DUT with a receiver which is different from the reference (for example, has a more capable equalizer with lower noise).

The FFE(s) (one per CTLE) of the first case would create the best VEC during stress calibration (which would require adding jitter to get the VEC to the target). The specification can be interpreted as if one of these multiple FFEs is the "pre-emphasis" that should be used (as there is no restriction), and each one creates a different stress. This does not make sense, as the signal in real life will not be optimized like that.

The FFE in the second case would create a signal that may look less ideal in calibdation (so less jitter will be added) but is actually better for the DUT. If we allow this FFE it can be used to game the test.

With no limitation on what "pre-emphasis" means, both cases above are equally valid; we do not expect people to go into the trouble of finding these FFE, but different people can use different settings and get different stressed signals which would defeat the purpose of a standard test. And other people may use signal generators with shorter FFEs or no FFE at all, creating even more variability in test conditions.

If we think the allosed "pre-emphasis" settings are not unlimited, we should specify what is allowed (and thus the optimization space for creating the stressed signal).

Although any specification would be better than none, the most reasonable specification would be the 5-tap FFE (3 pre, 1 post) in the COM model of clauses 162, 163, and annex 120D, which was used in multiple presentations that analyzed channels and stress signals, and will be widely implemented.

SuggestedRemedy

Insert the following paragraph after the 3rd paragraph of 120G.3.3.5.1 (Host stressed input test setup):

"The pattern genrator has pre-emphasis capability equivalent to the functional model of the transmit equalizer defined in 120F.3.1.2, with the coefficient values ranges and step sizes

in Table 120F–8."

Apply similarly for module stressed input test setup in 120G.3.4.3.1.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment proposes that test results will be very inconsistent since the strength of the tranmitter equalizer may very from just good enough to overkill. A similar sentiment is echoed by comments #66, #67, and #132.
#56 proposes PG EQ be constrained like the C2C TX in 120F.3.1.2
#66 and #67 proposes PG EQ be contrained like KR TX in 163.9.2
132 proposes PG EQ be constrained as having at most 2 taps with one post-cursor tap with value >= 0
Apply chosen constraint to both 120G.3.3.5.2 and 120G.3.4.3.1.
For task force discussion.

Cl 120G SC 120G.3.3.5.2 P 270 L 22 # 132

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *HI/MI SI PG EQ*

Remove ambiguity. The reader doesn't know if the writer had precursor emphasis in mind, or calls any output emphasis "pre-". Also, we can reduce the search space and variation among stressed signal setups a little.

SuggestedRemedy

Change "pattern generator pre-emphasis" to "pattern generator emphasis". Add "There is no more than one pattern generator post-emphasis tap, with a positive or zero value." Similarly in 120G.3.4.3.2.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
"Pre-emphasis" implies the equalization is provided by the transmitter rather than the receiver so the wording is not ambiguous.
Resolve using the response to comment #56.

120G HI/MI SI PG EQ [56, 66, 67, 132]

CI 120g SC 120g.3.3.5.2 P 270 L 21 # 66

Mellitz, Richardd Samtec

Comment Type TR *Comment Status* D *HI/MI SI PG EQ*

The statement following statement offers little constraint on what may be used for preemphasis. "The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used." For example: Why couldn't the pattern generator use a discrete mutli-tone (DMT) equalizer? There may be other examples.

SuggestedRemedy

Add a line indicating that the pattern generator pre-emphasis may be approximately the capability specified in 163.9.2

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #56.

CI 120g SC 120g.3.4.5.2 P 274 L 19 # 67

Mellitz, Richardd Samtec

Comment Type TR *Comment Status* D *HI/MI SI PG EQ*

The statement following statement offers little constraint on what may be used for preemphasis. "The pattern generator pre-emphasis and reference receiver settings that minimize VEC are used." For example: Why couldn't the pattern generator use a discrete mutli-tone (DMT) equalizer? There may be other examples.

SuggestedRemedy

Add a line indicating that the pattern generator pre-emphasis may be approximately the capability specified in 163.9.2

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #56.

These comments propose that some constraints on the pattern generator equalization architecture is required, but suggest different architectures/values.

#56 proposes PG EQ be constrained like the C2C TX in 120F.3.1.2
4 taps

#66 and #67 proposes PG EQ be constrained like KR TX in 163.9.2

#132 proposes PG EQ be constrained as having at most 2 taps with one post-cursor tap with value >= 0

C2C taps, Table 120F-1

Output waveform[c]			
absolute value of step size for all taps (min)	162.9.3.1.4	0.005	—
absolute value of step size for all taps (max)	162.9.3.1.4	0.025	—
value at min state for c(–3) (max)	162.9.3.1.5	–0.05	—
value at max state for c(–3) (min)	162.9.3.1.5	0	—
value at min state for c(–2) (max)	162.9.3.1.5	0	—
value at max state for c(–2) (min)	162.9.3.1.5	0.1	—
value at min state for c(–1) (max)	162.9.3.1.5	–0.3	—
value at max state for c(–1) (min)	162.9.3.1.5	0	—
value at min state for c(0) (max)	162.9.3.1.5	0.5	—
value at min state for c(1) (max)	162.9.3.1.5	–0.1	—
value at max state for c(1) (min)	162.9.3.1.5	0	—

KR taps, Table 163-5

Transmitter waveform			
absolute value of step size for all taps (min)	162.9.3.1.4	0.005	—
absolute value of step size for all taps (max)	162.9.3.1.4	0.025	—
value at minimum state for $c(-3)$ (max)	162.9.3.1.5	–0.06	—
value at maximum state for $c(-2)$ (min)	162.9.3.1.5	0.12	—
value at minimum state for $c(-1)$ (max)	162.9.3.1.5	–0.34	—
value at minimum state for $c(0)$ (max)	162.9.3.1.5	0.5	—
value at minimum state for $c(1)$ (max)	162.9.3.1.5	–0.2	—

120G HI SI PG BW 119

Cl 120G SC 120G.3.3.5.1 P 269 L 2 # 119

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI PG BW*

This used to say "corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input" because some pattern generators have jitter bandwidths around 100 MHz.

SuggestedRemedy

Before arbitrarily deleting technical content, I would like to hear from the PG companies and users if this is still a problem, and if it is, whether a tactic such as relying on the PG's own response with no extra filter is reasonable, or what to do.

Proposed Response *Response Status* W

PROPOSED REJECT.

This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.

The comment incorrectly observes that the reference content has been deleted. The referenced text states states: "The low-pass filter has 20 dB/decade rolloff with a –3 dB corner frequency between 150 MHz and 300 MHz."

The suggested remedy does not provide an actionable remedy, but rather requests information.

[Editor's note: Invalid comment.]

[Editor's note: Changed page from 268 to 269.]

This comment pertains to the recipe for creating bounded uncorrelated jitter.

The concern that, while D2.0 recommends a low-pass bandwidth range of 150-300 MHz and requires the BW to be within the frequency range of the test equipment, D2.2 rather requires the range to be in the 150-300 MHz range and says nothing about the test equipment bandwidth.

However, the comment provides no actionable remedy.

D2.0

Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to ensure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value is kept below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the output jitter profile given by maximum J_{RMS} and maximum J4u, and complies with the even-odd jitter specification, in Table 120F–1. The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target differential peak-to-peak voltage of 870 mV and transition time of 10 ps as measured at TP1a (without the use of a reference receiver). The crosstalk signal transition time is calibrated with PRBS13Q. The pattern

D2.2

Bounded uncorrelated jitter may not be available in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a low-pass filtered pseudo-random pattern. The pattern should be either PRBS7 or PRBS9 (see 83.5.10) with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 5.3125 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source. The low-pass filter has 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz.

120G HI SI PG output
118

Cl 120G SC 120G.3.3.5.1 P 268 L 45 # 118

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI PG output*

Before listing the impairments, this would be a good place to say that there is a pattern generator with adjustable amplitude, yet the four PAM4 levels are kept nominally (i.e. at low frequency) equally spaced.

SuggestedRemedy

Add sentence per comment. Similarly in 120G.3.3.4.1.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
The referenced Figure 120G-9 showing the presence of a pattern generator. Adjustable amplitude is implicit in the calibration procedure in 120G.3.3.5.2.
However, it might be appropriate to formally constrain the relative level mismatch.
For task force discussion.

120G.3.3.5.1 Host stressed input test setup

The host stressed input test setup is illustrated in Figure 120G–9. The stressed signal is applied at TP4a and is calibrated at TP4.

The stressed signal includes the following impairments:

— Sinusoidal jitter, random jitter, and bounded uncorrelated jitter and
— Counter-propagating crosstalk signals.

120G.3.4.3.1 Module stressed input test setup

The module stressed input test setup is illustrated in Figure 120G–10. The stressed signal is applied at TP1 and is calibrated at TP1a.

The stressed signal includes the following impairments:

— Sinusoidal jitter, random jitter, and bounded uncorrelated jitter
— Frequency-dependent attenuation representing the host channel, which may be implemented with PCB traces. The frequency-dependent attenuation is used only for the high-loss case (see 120G.3.4.3.2).
— Counter-propagating crosstalk signals.

120G HI SI method (PG transition time)
133

Cl 120G SC 120G.3.3.5.2 P 269 L 51 # 133

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *HI SI method*

Changing the "pattern generator [pre-]emphasis" in step g will change the pattern generator transition time from step a.
More generally, is asking the pattern generator for a particular edge speed reasonable, or should the calibration be based on the signal at TP4 rather than the signal at TP1 and the tolerances of the mated compliance boards (and the frequency-dependent attenuator, for module stressed input tolerance).

SuggestedRemedy

In step a, say that, exceptionally, this pattern generator transition time is defined for neutral emphasis at the pattern generator output.
Similarly in 120G.3.4.3.2.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D2.2 and D2.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
It might make sense to specify the pattern generator output equalization state for the transition time measurement. However, there is no explicit requirement for the pattern generator to support a neutral state as proposed.
For task force discussion.

120G.3.3.5.2 Host stressed input test calibration

The host stressed input signal is calibrated by the following procedure.

a) The pattern generator is set to generate a PRBS13Q pattern (see 120.5.11.2.1) with transition time (see 120G.3.1.4) at TP4a as specified in Table 120G–8. The initial signal level is set as high as possible without exceeding the differential peak-to-peak input voltage tolerance given in Table 120G–7.

120G pattern numbers 114

D2.0 comment #178

Cl 120G SC 120G.3.1.5 P 263 L 8 # 114

Dawe, Piers Nvidia

Comment Type TR *Comment Status* D *pattern numbers*

Removing any mention of the pattern numbers that have been used for module testing for 20 years, 40GBASE-CR4 and 100GBASE-CR10, and AUIs 83E and 120E, is not warranted. There is no need for the writer to obstruct module professionals. As this annex uses several test patterns like an optical PMD, it should have a table of test patterns giving the pattern number, which this draft lacks, and description, and reference for definition.

SuggestedRemedy

After
All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q (see 120.5.11.2.1) or PRBS31Q (see 120.5.11.2.2) pattern
add
PRBS13Q is also known as pattern 4 and PRBS31Q is also known as pattern 3.
If it's worth repeating the references to 120.5.11.2.1 and 120.5.11.2.2 in 120G.3.2.2 (and it is, because a module professional doesn't have a specific reason to read 120G.3.1.5 Host output eye height and vertical eye closure (VEC)), add the same sentence there. It could be an informative NOTE. We could assume that someone using a stressed input section will read the section for one of the outputs, so I'm not asking to add the same information to the stressed input sections.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment is a restatement of D2.2 comment #119 with a modified suggested remedy.
D2.2 comment #119 requested a table listing patterns and providing patttern numbers.
There was no consensus by the task force to make the proposed changes.
The reference to pattern numbers is not necessary as this is not an opitical interface.

Cl 120G SC 120G.3.1.5 P 252 L 13 # 119

Dawe, Piers Nvidia

Comment Type TR *Comment Status* R *pattern table*

As this annex uses several test patterns like an optical PMD, it should have a table of test patterns giving the pattern number, which this draft lacks, and description, and reference for definition.

SuggestedRemedy

Copy Table 167-10, Test patterns, leaving out the rows that don't apply. Refer to the table from elsewhere in the annex to reduce clutter end repetition.

Response *Response Status* U

REJECT.

Table 167-10 may be found in 802.3db.

It is not clear that the proposed table with pattern numbers will improve the draft all things considered.

It can indeed reduce some clutter for cases where multiple patterns are listed for a particular test step, but not in cases where a single pattern is referenced. It is more convenient to the reader to list the pattern names; the reader would otherwise have to memorize the relationship between pattern numbers and the pattern they represent. The test pattern names line up better with the test equipment controls.

120G MI SI FDA equation 109

Cl 120G SC 120G.3.4.3.2 P 274 L 4 # 109

Dawe, Piers Nvidia

Comment Type T *Comment Status* D *(bucket1)*

I believe that when the complex numbers are boiled down to decibels, and noting that gamma0 is 0 and Zc is 100 ohm, the respones has the form Ildd = A.sqrt(f) + B.f exactly.

SuggestedRemedy

Please give the equation.

Proposed Response *Response Status* W

PROPOSED REJECT.
The equations provide the complex s-parameters necessary as a target for the frequency-dependent loss and the ILdd in decibles is provide in Figure 120G-11. It is not necessary to provide yet another equation.

Piers provided the following equation.
Ildd = 1.53979838173527*sqrt(f) +0.386537515033892*f
reduce coefficient precision to 4 significant digits
Ildd = 1.540*sqrt(f) +0.3865*f

The equation does indeed match the plotted curved. See plot to the right.
The red circles are a plot of the ILdd equation above.

This might be appropriate as an informative equation.