Supporting material for comment i-71

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Text in question

g) Eye height and VEC are measured at TP1a as described in 120G.5.2 with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to –10.5 dB. The pattern generator amplitude and random jitter are adjusted, while the pattern generator output equalization and reference receiver settings are adjusted to minimize VEC, so that the eye height of the smallest eye matches the target value and VEC is within the limits in Table 120G–10. The differential peak-to-peak voltage measured at TP4 does not exceed the differential peak-to-peak input voltage tolerance given in Table 120G–9.

This should be TP1a – TP4 is copy-paste inherited from the host stress input test.

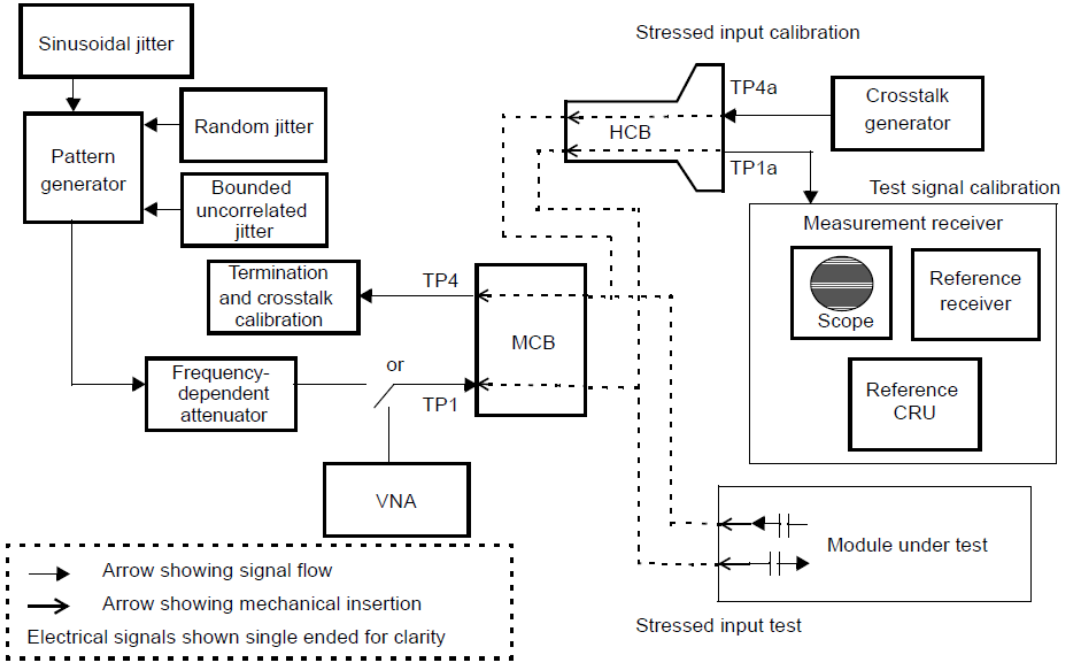
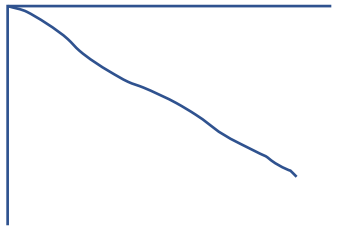


Figure 120G–10—Example module stressed input test

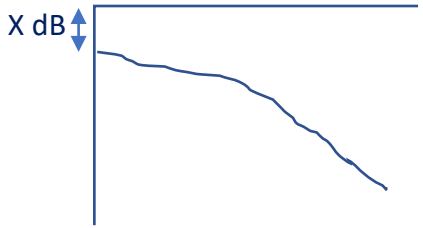
Thought experiment

- Assume we limit the reference receiver settings as instructed but limit ourselves to **CTLE settings with gDC + gDC2 less than or equal to –10.5 dB**.
  - At the chosen CTLE setting, the CTLE is doing at least some equalization of the signal, attenuating low frequencies by at least 10.5 dB.
  - The pattern generator output equalization is adjusted to the best VEC with this CTLE setting. It may be left with some “work” (more DC attenuation, say X dB) but it can’t take the 10.5 dB from the CTLE.
  - The PG output equalization is now fixed! The stress signal is applied to the DUT.
  - The VEC is optimized after the reference RX (CTLE+DFE) – but not before it.

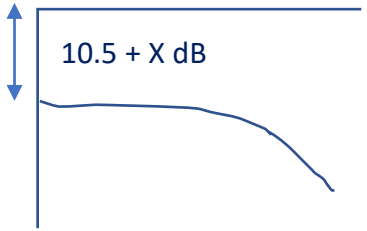
Crude illustration…



IL of the channel



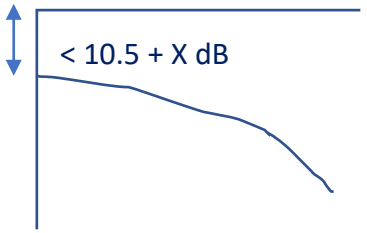
Spectrum of the signal with partial Tx equalization (input to the DUT)



Spectrum of the signal with Tx equalization + chosen setting of the reference CTLE
(not fully equalized – some ISI remains for the DFE)

Thought experiment

- The concern raised was: What if a “weaker” CTLE setting (lower gDC+gDC2) creates a lower VEC? Does it make life easier for the DUT?
  - But the PG output equalization is fixed!
  - If the DUT tries a weaker CTLE the DC attenuation will be lower ⇒ less optimized overall equalization
  - The DFE may compensate somewhat but it is too short to correct the discrepancy
- It might be possible to create a better signal for the DUT if the PG output equalization were adjusted to compensate for the weaker CTLE
  - But the DUT can’t do that – **the stress signal is not adjusted at this point!**



Spectrum of the signal with Tx equalization + weaker setting of the reference CTLE

The issue with the current text

- It creates a hypothetical problem – what if the minimal VEC is found with another, “weaker” CTLE setting (lower gDC+gDC2), and with PG equalization adjusted accordingly?
  - The test engineer may wonder what to do…
  - But the answer is simple: we want to create a signal that the module will need to equalize by at least 10.5 dB.
  - Any signal optimized with a weaker CTLE would be inadequate for the test purpose – and must not be used!
  - Whether a better signal can be achieved with a different PG equalization and weaker CTLE is irrelevant – because the DUT won’t be able to take advantage of it.
- Phrasing the instructions as suggested would make them clear and eliminate the “problem” for the test engineer.

Concerns

- From consensus building discussion:
  - Is it clear from the suggested text that the PG equalization has to be co-optimized with reference receiver setting?
    - The intention of the text "output equalization and reference receiver settings are adjusted to minimize VEC" is that all settings should be optimized together, but it may be misunderstood
  - What if the PG is configured sub-optimally such that VEC is within the target range, but a lower-boost setting turns out to have better VEC?
    - In a practical test setup this can't be ruled out – needs to be addressed
- Some additional text is suggested

Proposed change – updated

g) Eye height and VEC are measured at TP1a as described in 120G.5.2 ~~with the exception for the high-loss case that the reference receiver CTLE setting that minimizes VEC has gDC + gDC2 less than or equal to –10.5 dB~~. For the high-loss case, an exception is made that the reference receiver CTLE is limited to settings where gDC + gDC2 is less than or equal to –10.5 dB.

h) The pattern generator amplitude, output equalization, and random jitter are adjusted together~~, while the pattern generator output equalization and reference receiver settings are adjusted~~ to minimize VEC, so that the eye height of the smallest eye matches the target value, ~~and~~ VEC is within the limits in Table 120G–10, and the~~. The~~ differential peak-to-peak voltage measured at ~~TP4~~TP1a does not exceed the differential peak-to-peak input voltage tolerance given in Table 120G–9. The pattern generator output equalization has to be set such that for the resulting signal, the lowest VEC is achieved with a reference receiver CTLE setting within the limited range.

Other calibration procedures resulting in a signal that meets these requirements may be used.

NOTE—With a pattern generator output equalization that is fully optimized to minimize VEC for a given reference receiver, any other reference receiver setting results in a higher VEC.