Comment Resolution for Annex 120G Topics

Matt Brown, Huawei, 802.3ck Editor-in-Chief

Data path wording Comment 6

Cl 120G SC 120G.1 P 256 L 12 # R1-6

Brown, Matthew — Huawei Technologies Canada

Comment Type E *Comment Status* D *data paths*

The implementation of Draft 3.0 comment i-92 resulted in the sentence being changed from: "The C2M interface comprises independent data paths in each direction."
to: "The C2M interface is composed of independent transmit and receive data paths."
The first part of the proposal was to replace the use of "comprises" with "is composed of" to be consistent throughout the standard. There is nothing wrong with this change.
The other part of the proposal was to change the text used to describe the data paths.
Unfortunately, the new text uses terminology that is not consistent with the rest of the Annex. Specifically, there is no concept of a "transmit path" or "receive path". The original wording was chosen with this in mind.

SuggestedRemedy

Change: "The C2M interface is composed of independent transmit and receive data paths."
To: "The C2M interface is composed of independent data paths in each direction."

Proposed Response *Response Status* W

PROPOSED ACCEPT.

Changes between D3.1 and D3.0…

The C2M link is described in terms of a host C2M component, a C2M channel with associated ~~differential-mode to differential-mode~~ insertion loss (ILdd), and a module C2M component. The host C2M component and module C2M component have connected ground references. Figure 120G–2 depicts a typical C2M application and summarizes the ILdd budget associated with the C2M application. The ILdd budget reflects the highest ILdd intended to be supported and is characterized by Equation (120G–5) and illustrated in Figure 120G–17. The C2M interface ~~comprises~~ is composed of independent transmit and receive data ~~paths in each direction~~paths. Each 100GAUI-1, 200GAUI-2, and 400GAUI-~~-~~4 C2M data path contains one, two, or four differential lanes, respectively, using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

Cl 120G SC 120G.1 P 256 L 11 # I-92

Grow, Robert — RMG Consulting

Comment Type E *Comment Status* A *(bucket4)*

Similar misuses of "comprise" have been rewritten using "compose" in P802.3/D3.0.

SuggestedRemedy

The C2M interface is composed of independent transmit and receive data paths.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

Change: "The C2M interface comprises independent data paths in each direction."

To: "The C2M interface is composed of independent transmit and receive data paths."

Similar text in 802.3dc D3.2, 135G.1

The 50GAUI-1 C2M interface comprises independent data paths in each direction. The data path contains one differential lane, which is AC-coupled within the module.

The 100GAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled within the module.

Similar text in 802.3dc D3.2, 120E.1

The 200GAUI-4 C2M link is described in terms of a host 200GAUI-4 C2M component, a 200GAUI-4 C2M channel with associated insertion loss, and a module 200GAUI-4 C2M component. Figure 120E–2 depicts a typical 200GAUI-4 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 200GAUI-4 C2M interface comprises independent data paths in each direction. Each data path contains four differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

The 400GAUI-8 C2M link is described in terms of a host 400GAUI-8 C2M component, a 400GAUI-8 C2M channel with associated insertion loss, and a module 400GAUI-8 C2M component. Figure 120E–3 depicts a typical 400GAUI-8 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The recommended insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 400GAUI-8 C2M interface comprises independent data paths in each direction. Each data path contains eight differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

HO/HI return loss, part 1
Comments 50, 51

Cl 120G SC 120G.3.1.1 P 258 L 41 # R1-50

Dawe, Piers J G NVIDIA

Comment Type T *Comment Status* D *HO/HI RL*

Most product IL and RL specs (including ERL) start at 50 MHz, although test fixture specs start at 10 MHz and recommendations and reference equations are not bound by measurement practicalities. Including the RLdc limit in 162.9.4.7. I don't know why this product RLdc would be special.

SuggestedRemedy

Change 0.01 to 0.05. Also for Eq 120G-2 in 120G.3.3.3.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
This comment does not apply to the substantive changes between IEEE P802.3ck D3.0 and D3.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
However, the proposed change is an improvement to the draft.
Implement the suggested remedy with editorial license.

Cl 120G SC 120G.3.1.1 P 258 L 42 # R1-51

Dawe, Piers J G NVIDIA

Comment Type T *Comment Status* D *HO/HI RL*

This RLdc spec goes to 50 GHz while the one in 162.9.4.7 goes to 40 GHz. I know the channel in C2M can be super-low-loss, but the modulation format and receiver filtering remove a lot of energy above 40 GHz. I did not notice any other *product* specs going to 50 GHz, but we should review them if they exist.

SuggestedRemedy

If appropriate, change 50 to 40, here and in Eq 120G-2.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D3.0 and D3.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
CR and C2M are not the same interface and there may be valid reasons for the frequency ranges to be different.
For task force discussion.

120G.3.1.1 Host output common-mode to differential-mode return loss

The host output common-mode to differential-mode return loss shall meet Equation (120G–1) as illustrated in Figure 120G–5.

$$RLdc(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.01 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases} \quad \text{(120G–1)}$$

120G.3.3.3 Host input differential-mode to common-mode return loss

The host input differential-mode to common-mode return loss shall meet Equation (120G–2) as illustrated in Figure 120G–8.

$$RLcd(f) \geq \begin{cases} 22 - 16(f/53.125) & 0.01 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases} \quad \text{(120G–2)}$$

HO/HI return loss, part 2
Comments 50, 51

162.9.5.6 Differential-mode to common-mode return loss

The receiver differential-mode to common-mode return loss shall meet Equation (162–16) as illustrated in Figure 162–6.

$$RLcd(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases} \quad (162\text{–}16)$$

162.11.4 Differential-mode to common-mode return loss

The cable assembly differential-mode to common-mode return loss shall meet Equation (162–18).

$$RLcd(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases} \quad (162\text{–}18)$$

162.9.4.7 Common-mode to differential-mode return loss

The transmitter common-mode to differential-mode return loss shall meet Equation (162–5).

$$RLdc(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases} \quad (162\text{–}5)$$

120F.3.2.3 Receiver differential-mode to common-mode return loss

The differential-mode to common-mode return loss of the receiver shall meet Equation (120F–1). The differential-mode to common-mode return loss limit is illustrated by Figure 120F–4.

$$RLcd(f) \geq \begin{cases} 25 - 0.72f & 0.05 \leq f \leq 13.9 \\ 15 & 13.9 < f \leq 38 \end{cases} \quad (120F\text{–}1)$$

163.9.3.4 Receiver differential-mode to common-mode return loss

The differential-mode to common-mode return loss of the receiver shall meet Equation (163–5). The differential-mode to common-mode return loss limit is illustrated by Figure 163–5.

$$RLcd(f) \geq \begin{cases} 25 - 20(f/53.125) & 0.05 \leq f \leq 26.5625 \\ 15 & 26.5625 < f \leq 53.125 \end{cases} \quad (163\text{–}5)$$

163.10.4 Channel differential-mode to common-mode return loss

The TP0 to TP5 channel differential-mode to common-mode return loss shall meet Equation (163–9).

$$RLcd(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases} \quad (163\text{–}9)$$

Summary:

Clause 162, TX RLdc, 0.05 GHz and 40 GHz
Clause 162, RX RLcd, 0.05 GHz and 40 GHz
Clause 162, CA RLcd, 0.05 GHz and 40 GHz
Clause 163, RX RLcd, 0.05 GHz and 53.125 GHz
Clause 163, channel RLcd, 0.05 GHz and 40 GHz
Annex 120F, RX RLcd, 0.05 GHz and 38 GHz

For lower limit, 0.05 GHz is use everywhere by 120G.

For upper limit…
40 GHz is used throughout 162 and for Clause 163 channel
53.125 GHz is used for Clause 163 RX
38 GHz is used for Annex 120F RX

HI/MI Pattern Generator Comment 54, part 1

Cl 120G *SC* 120G.3.3.5.1 *P* 265 *L* 49 # R1-54

Dawe, Piers J G NVIDIA

Comment Type T *Comment Status* D *HI/MI PG*

For module output, the optimum setting for the second precursor is 0.02 to 0.04, so the optimum for any third precursor would be less than 1/2 a COM step of 0.02. We can simplify the tuning challenge for real modules and stressed signal generators by removing clutter. 120G has 4 dB more headline loss than 120F and a module doesn't have the very large package loss that 120F may have, so it may be reasonable that 120F has a small c(-3) term when C2M host stressed input doesn't need it.

SuggestedRemedy

Change "The pattern generator output equalization functional behavior is equivalent to the model shown in Table 120F-3. The tap coefficients are not specified" to "The pattern generator output equalization functional behavior is equivalent to the model shown in Table 120F-3, with c(-3) always zero. Other tap coefficients are not specified".

Unless the extra loss in the module stressed input signal tips makes this tap significant, this can apply to 120G.3.4.3.1 also.

Proposed Response *Response Status* W

PROPOSED REJECT.
This comment does not apply to the substantive changes between IEEE P802.3ck D3.0 and D3.1 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.
This comment is a restatement of comment i-192 against D3.0 recorded in the following comment report:
https://www.ieee802.org/3/ck/comments/draft3p0/8023ck_D3p0_final_closedcomments_sortedByNumber.pdf
A straw poll, also recorded in the comment response to i-192, indicated clear concensus to make no changes to the output equalizer c(-3) tap.

Cl 120G *SC* 120G.3.3.5.1 *P* 265 *L* 50 # I-192

Dawe, Piers J G NVIDIA

Comment Type TR *Comment Status* R *HI SIT PG*

For module output, the optimum setting for the *first* precursor is 0.02 to 0.04, and the optimum for the *second* precursor is much smaller, so very weak. It would be better to make stressed signals (and real signals) consistent across the industry and simplify the tuning challenge for real modules than to try to squeeze out the last drop of tuning. We don't use smaller than 0.02 steps in COM.
The same point applies to module stressed input signal generator, but 120G.3.4.3.1 refers back to here.

SuggestedRemedy

For the host stressed input signal generator functional model, set the third precursor to zero. Modify "The tap coefficients are not specified with the exception that".

Response *Response Status* C

REJECT.

Per straw poll #12 there is no consensus to make the proposed changes.

Straw poll #12
I support reducing the pattern generator reference architecture to have 2 precursor taps instead of 3.
Yes: 7
No: 21

HI/MI Pattern Generator Comment 54, part 2

120G.3.3.5.1 Host stressed input test setup

The host stressed input test setup is illustrated in Figure 120G–9. The stressed signal is applied at TP4a and is calibrated at TP4.

The stressed signal includes the following impairments:

— Sinusoidal jitter, random jitter, and bounded uncorrelated jitter and
— Counter-propagating crosstalk signals.

The pattern generator output equalization functional behavior is equivalent to the model shown in Figure 120F–3. The tap coefficients are not specified with the exception that the "no equalization" state is defined as setting coefficient c(0) to 1 and all other coefficients to 0.

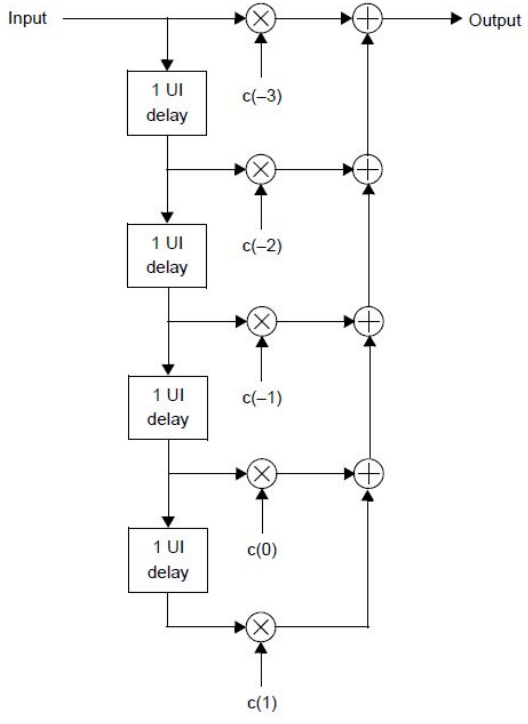

Figure 120F–3—Transmitter equalizer functional model