Loss from TP0 to TP2

P802.3ck Draft 3.1 comments 41, 43

Piers Dawe, Nvidia

April 2022

Updated 12 April: slides 10 to 13

Comments 41 and 43

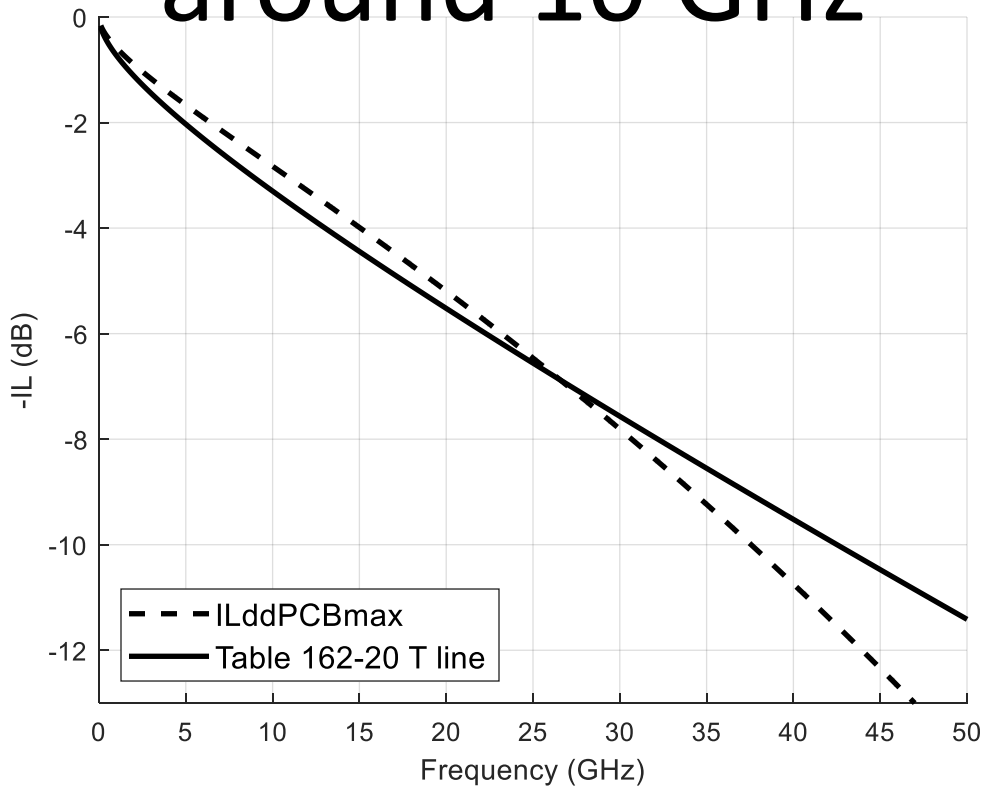
- 41 The equation for the channel from TP0 to TP2 or from TP3 to TP5 including the test fixture should be checked for consistency with the equations for the PCB, the mated test fixtures, and the cable test fixture traces, although there won't be a perfect match because of the allowances for ball grid array (BGA) footprint and host connector footprints, as well as the difference between product connector and test fixture connector
- 43 The revision to the mated test fixtures' reference loss to be more like real measurements makes a small difference to the expected Rpeak

Problem statement

- Expect that:
- $ILdd_{HostMax}$, TP0 to TP2 =
- PCB trace + small effects* + mated test fixtures
- PCB trace can be taken from
  - $ILdd_{PCBmax}$ in Eq. 162A–2, or
  - PCB model in Table 162–20
- Eq 162A–3 (TP0 to TP2) doesn't match either of these
  - Too little loss at low *f* and above Nyquist
- Mated test fixture definition has changed

  * 0.2 dB for BGA and connector footprints

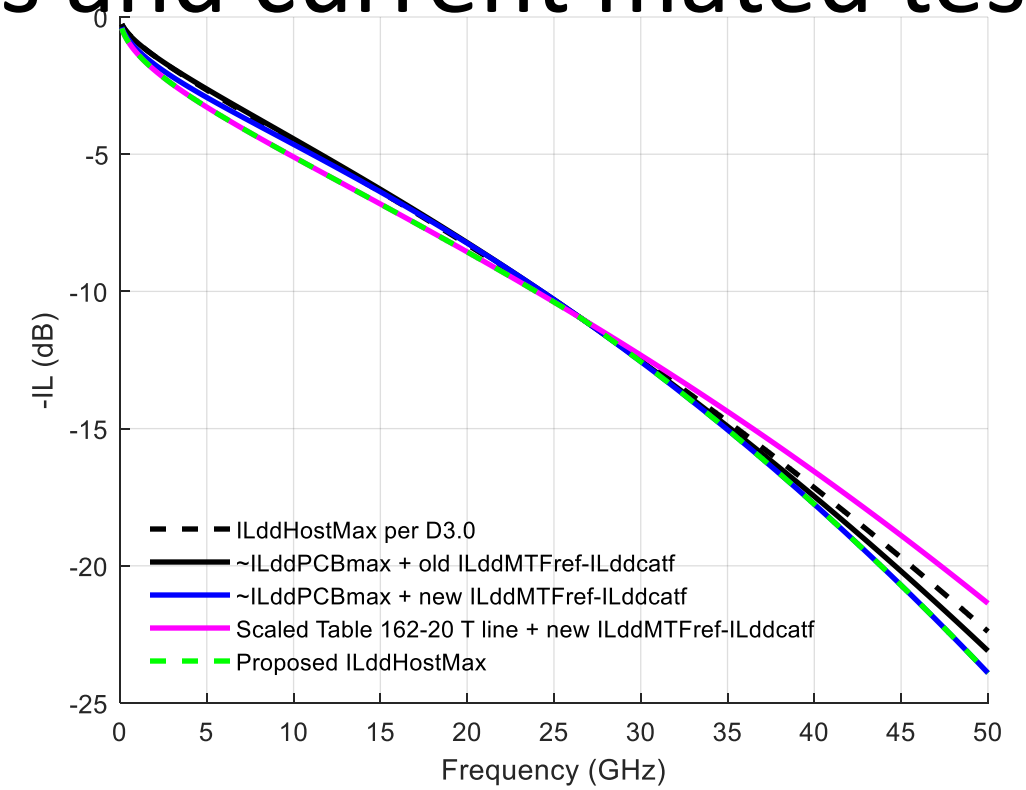
More than "max" loss is likely around 10 GHz



This is the PCB trace *only*

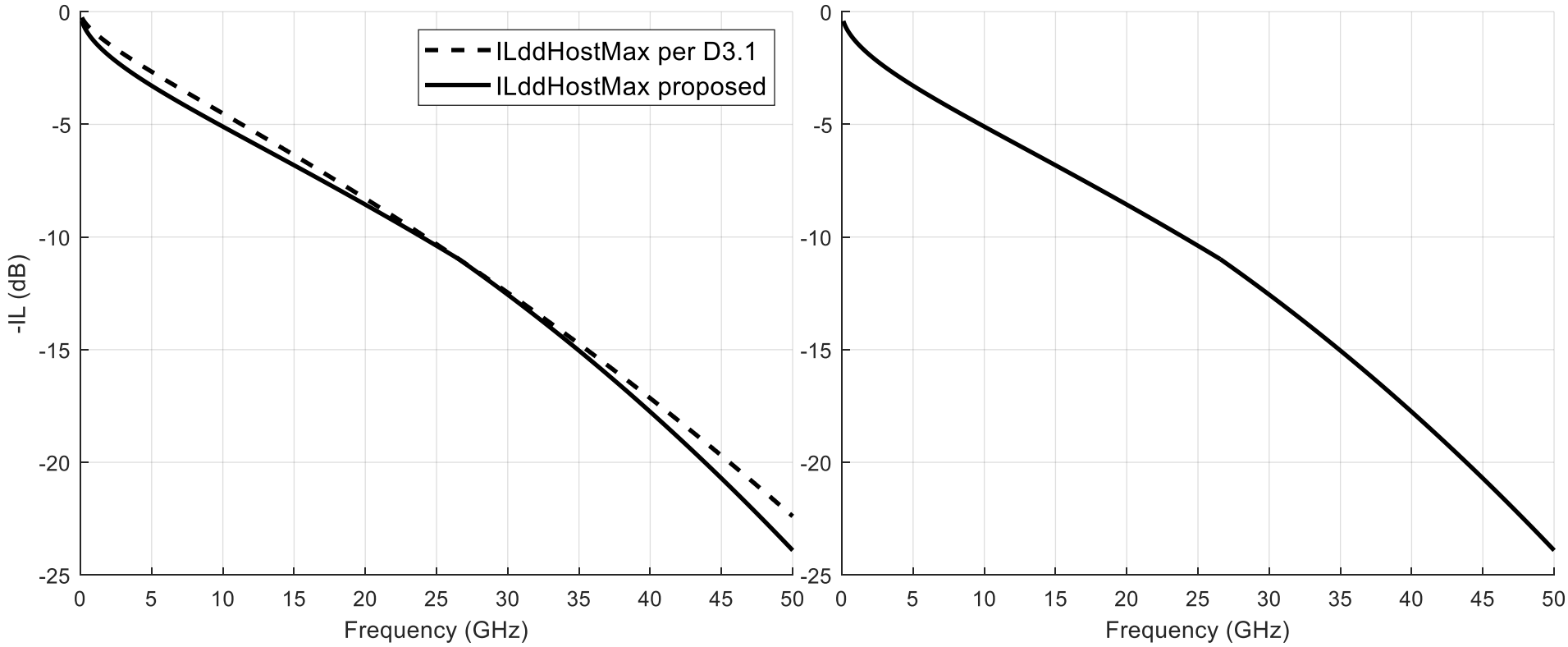
- We use the PCB model in Table 162–20 in COM for qualifying CR cables, and C2M module output and module stressed input, so it provides a valid host channel
- The $ILdd_{PCBmax}$ curve (scaled 120E MCB/HCB PCB traces) is valid too

TP0-TP2 with range of max-loss host channels and current mated test fixtures



- Need to allow more curvature at low frequencies, but also roll-off well above Nyquist
- Recommend the magenta line below Nyquist and the blue above
  - A channel that rolls off more strongly than blue above ~35 GHz would work too
- Combination is shown as dashed green

Summary, new plot for Fig 162A–2

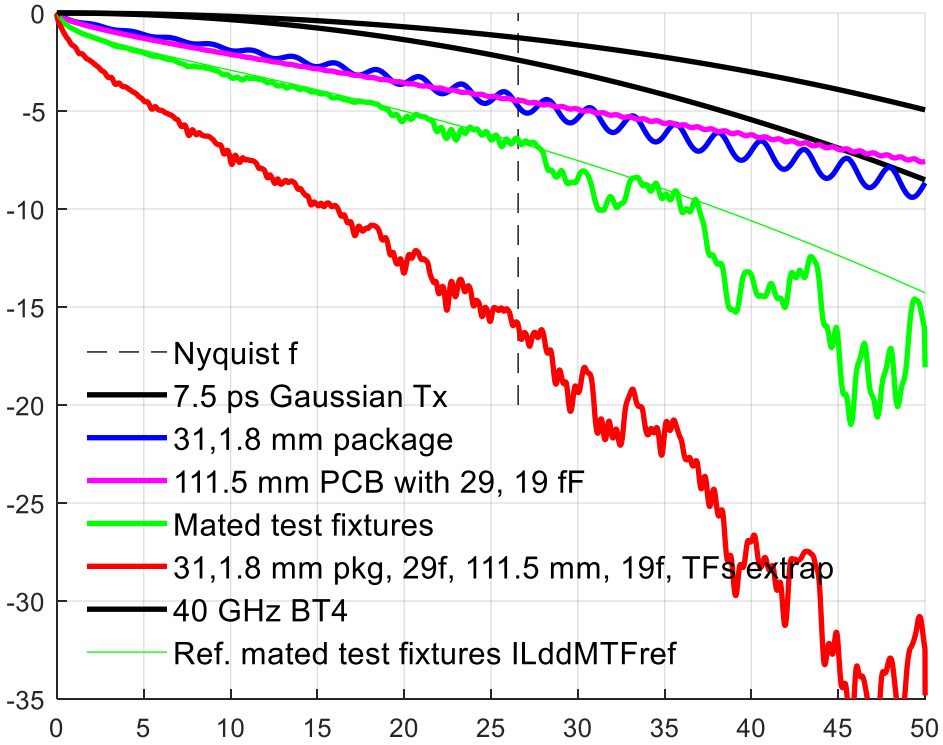


- Figure 162A–2 Insertion loss from TP0 to TP2 or from TP3 to TP5

Associated changes

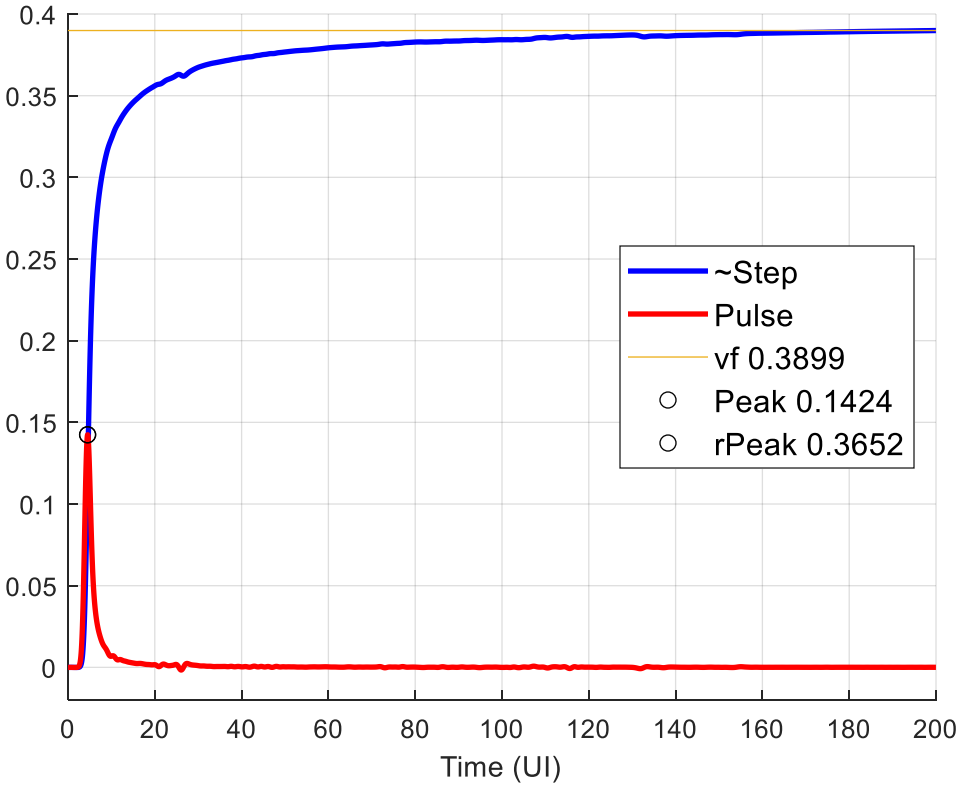
- Equation 162A–3
  - Existing: $ILdd_{Host} \leq ILdd_{HostMax}$ =
  - 1.5658*(0.471*sqrt(f) + 0.1194f + 0.002f^2)
  - Proposed: $ILdd_{Host} \leq ILdd_{HostMax}$ =
  - 1.2513*sqrt(f) + 0.08007f + 0.003405f^2 0.01 <= f <= 26.56
  - 1.1351*sqrt(f) + 0.05202f + 0.005310f^2 26.56 < f <= 50
- Recalculate *Rpeak* (min) based on the magenta line
  - Table 162-10
  - ISI affects *Rpeak* too, so can't use the smooth curves: have to go back to more realistic models with ISI
  - Existing: 0.397
  - Proposed: 0.365

The losses add up...



- Standard COM assumptions

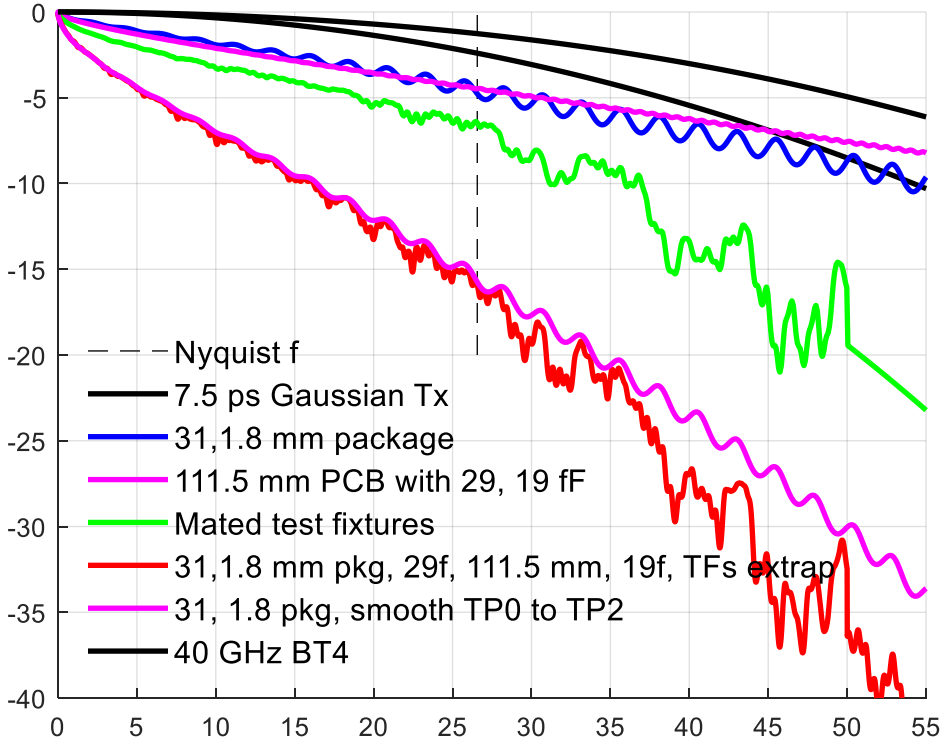
Fitted pulse analysis

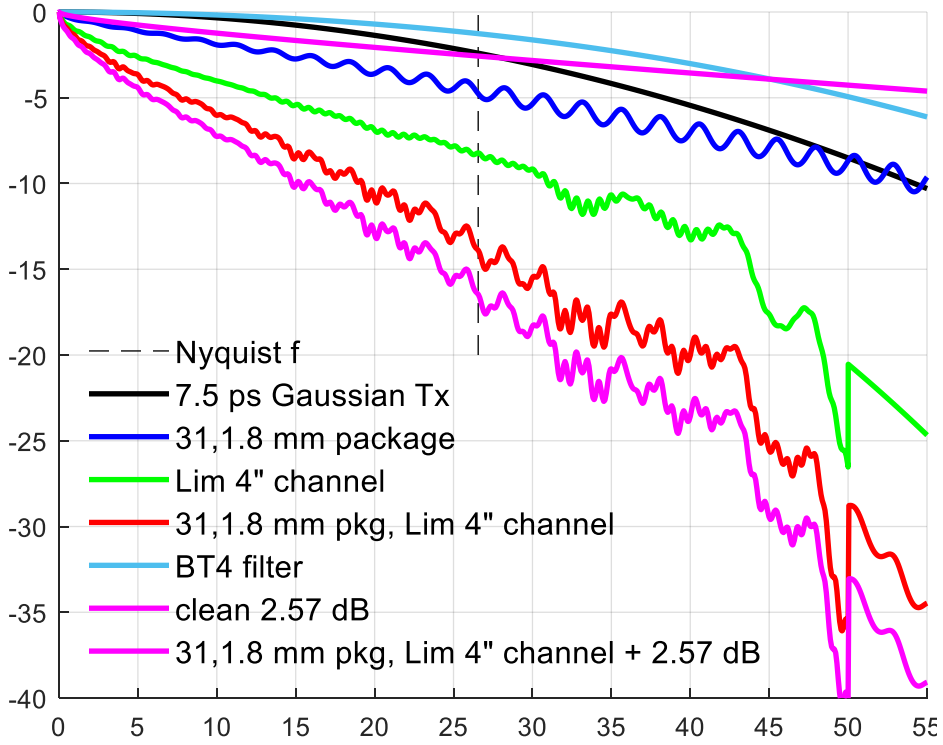


Changed from 0.4 to match the draft

- *vf* is 4% above the spec limit of 0.387 V, for standard Av 0.413 V
- *Rpeak* at 0.365 is different to spec limit of 0.397
- ERL is 10.5? dB; draft spec limit is 7.3. Worse ERL in real product allows worse ISI which reduces *rPeak*

Same package model, smooth TP0 to TP2. Lim 4" + loss

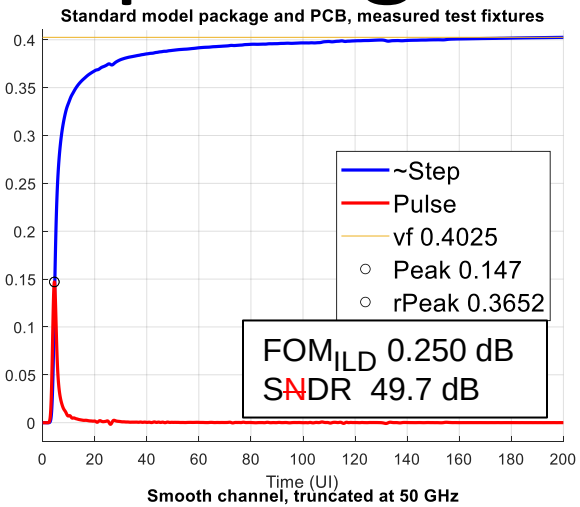


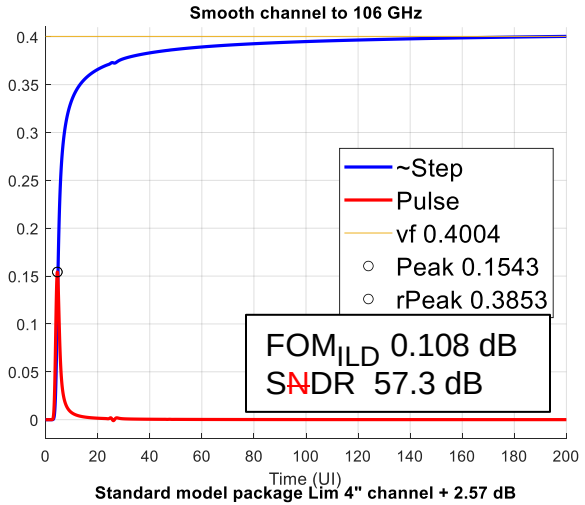


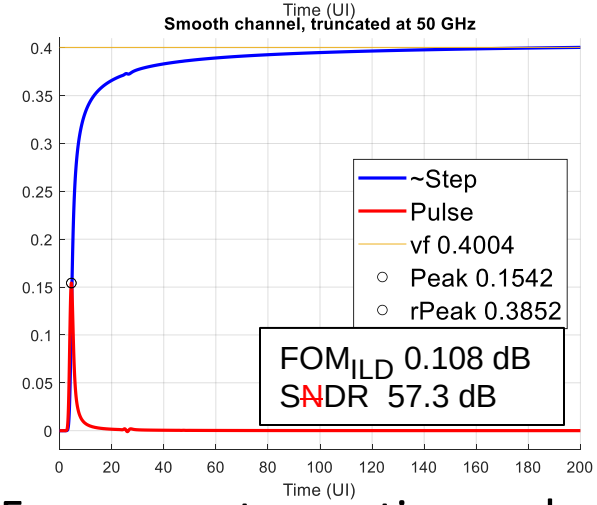
- Magenta: same COM package model with ripple, then smooth channel, TP0 to TP2

- Lim 4" channel
- Loss is different so extra clean loss added, roughness with package is very similar

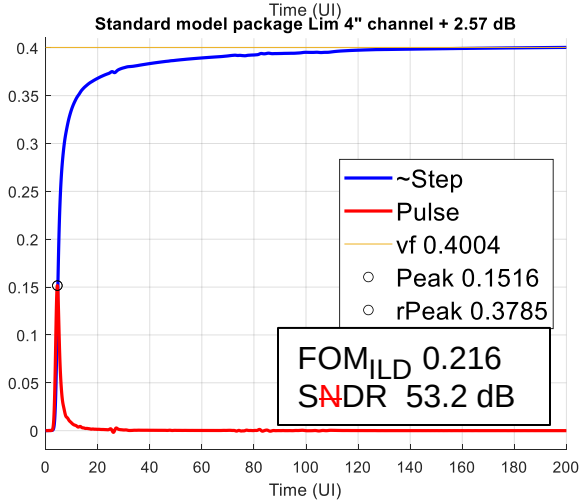
Comparing to clean reference losses





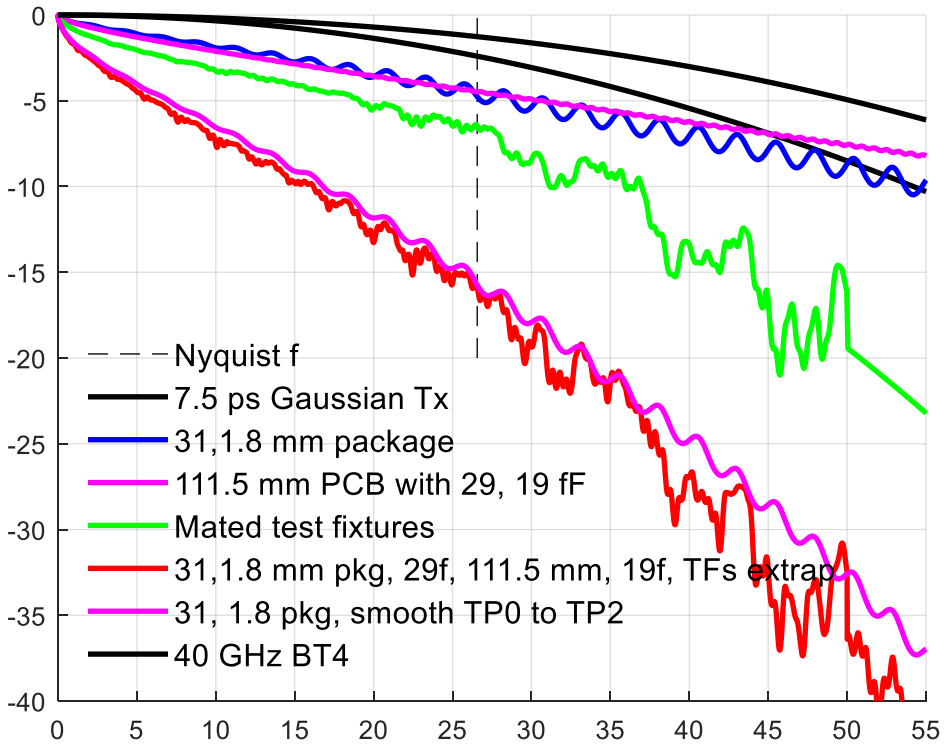


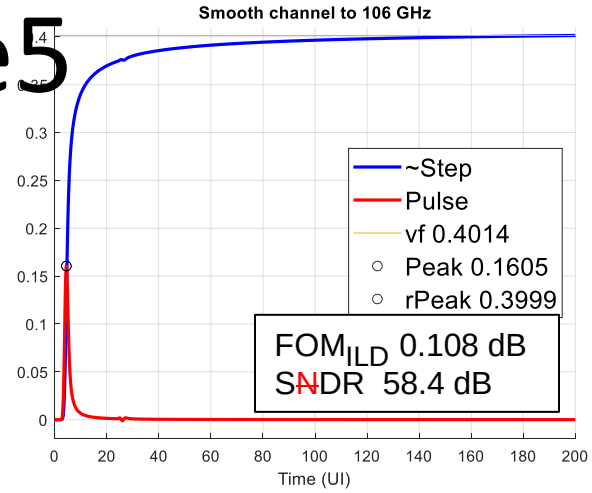
Unofficial FOM_{ILD} based on 7.5 ps



- Frequency truncation makes hardly any difference
- Even the ideally clean channel with optimistic loss above Nyquist gives lower linear fit pulse peak ratio, Rpeak than the 0.397 limit in the draft
- Lim channel + clean loss is between smooth channel and actual test fixtures

Using blue line on slide5





Compare this magenta line with the one on slide 10

- A slightly different channel, better than the COM assumption, gives a higher Rpeak
- A channel for measurement would not be like this, as there is not enough loss at low f for the TP2 test fixture
- The lower Rpeak on earlier slides is a feature of how we do the measurement

Conclusion

- Rpeak is sensitive to both signal "speed" and "roughness" (ISI, ILD)
- Significantly worse ISI and ERL is allowed by the spec
- Link is protected by SNDR and ISI_RES / SNR_ISI, so Rpeak should control for speed assuming reasonable (not ideal) roughness
  - Reasonable ICs and channels made to the usual assumptions that are used for cable compliance
- The Rpeak limit in D3.1 is significantly better than the COM assumptions for the cable including SNR_TX
- Nothing in this presentation affects the cable spec