Normative Annex 200A Proposal

Updates to Clause 1

1.4.245c EQT: The unit of measurement of time for time-related parameters specified in Clause 144 and Clause 200 Multipoint MAC Control. Each EQT is equal to the time required to transmit one EQ between the MCRS and the PCS in the downstream direction. When an EQ is transmitted across 25GMII (Clause 144), the EQT is equal to 2.56 ns. When an EQ is transmitted across XGMII (Clause 200), the EQT is equal to 6.4 ns.

Annex 200A (Normative)

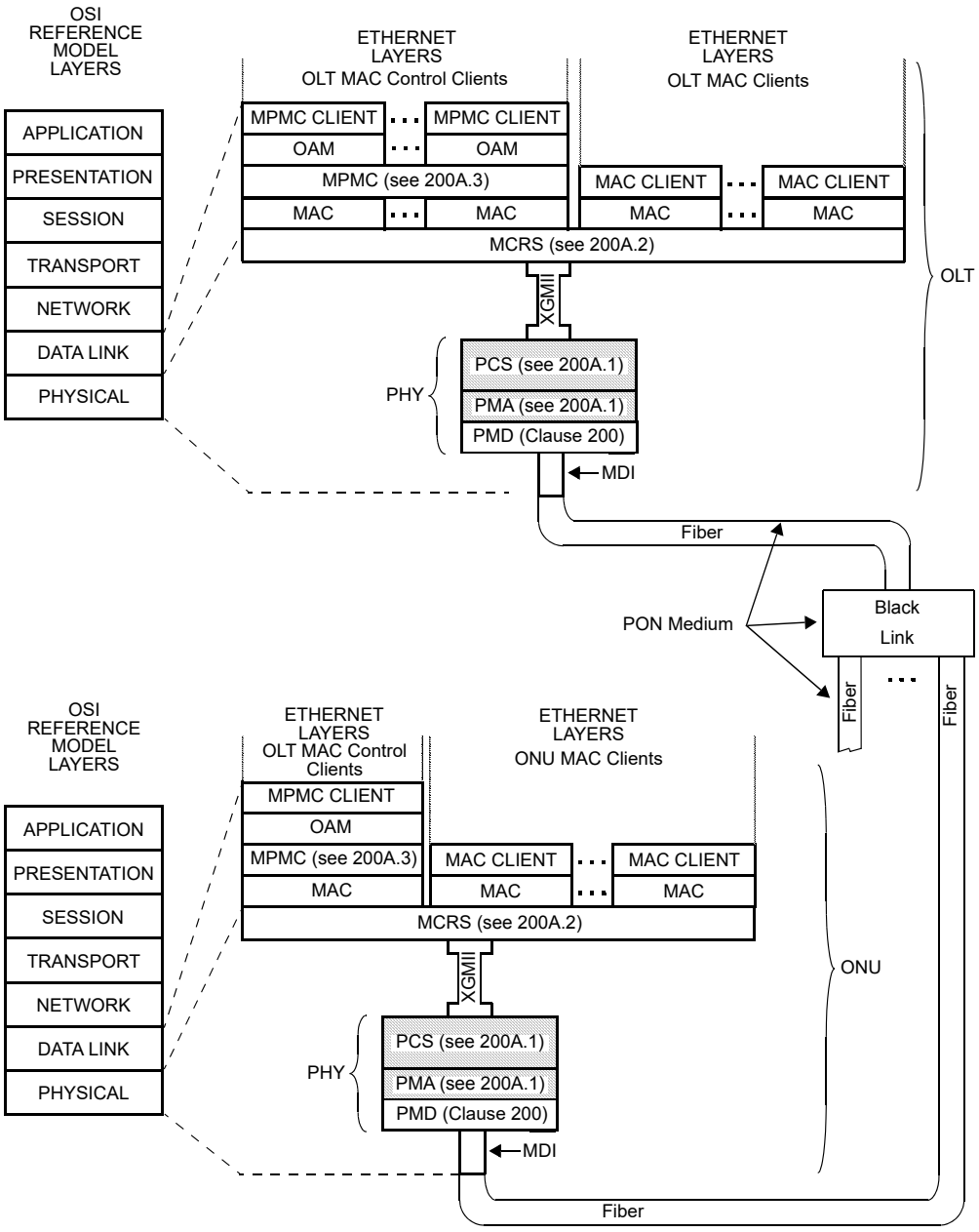
Physical Coding Sublayer, Physical Media Attachment, Reconciliation Sublayer, and Multipoint MAC Control Sublayer for Super-PON

The Super-PON Physical Coding Sublayer, Physical Media Attachment, Reconciliation Sublayer, and Multipoint MAC Control Sublayer are respectively based on the Nx25G-EPON Physical Coding Sublayer and Physical Media Attachment (see clause 142), Reconciliation Sublayer (see clause 143), and Multipoint MAC Control Sublayer (see clause 144). This annex specifies extensions to clause 142, 143, and 144 to make them suitable for Super-PON.

200A.1 Extensions to Nx25G-EPON Physical Coding Sublayer and Physical Media Attachment (clause 142) for Super-PON

200A.1.1 Extensions to subclause 142.1 (Overview)

Replace figure 142-2 with figure 200A-1.



PCS and PMA described in this subclause

XGMII= 210GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A–1—Relationship of EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

The Super-PON PCS supports Super-PON PMDs, where:

- both the receive and transmit paths operate at 10.3125 GBd rate (symmetric Super-PON ONU/OLT), or
- the receive path operates at 10.3125 GBd rate and the transmit path operates at 2.578125 GBd (asymmetric Super-PON ONU), or
- the transmit path operates at 10.3125 GBd rate and the receive path operates at 2.578125 GBd (asymmetric Super-PON OLT).

200A.1.2 Extensions to subclause 142.1.2 (Delay constraints)

The combined delay variation through the transmit path of the Nx25G-EPON PCS and PMA is expected to be less than 6 EQTs (see 1.4.245c) for channels operating at 25.78125 GBd and less than 15 EQTs for channels operating at 10.3125 GBd.

The combined delay variation through the receive path of the Nx25G-EPON PCS and PMA is expected to be less than 2 EQTs for channels operating at 25.78125 GBd and less than 5 EQTs for channels operating at 10.3125 GBd.

The aforementioned delay variation limits are applicable only for the data units (either EQ or the corresponding 257-bit block) located at the fixed offset within the FEC codeword.

200A.1.3 Extensions to subclause 142.2 (PCS transmit data path)

In a Super-PON OLT, the PCS transmit function operates in a continuous mode at the 10.3125 GBd rate.

In a Super-PON ONU, the PCS transmit function operates in burst mode at the 10.3125 GBd rate (symmetric ONU) or at the 2.578125 GBd rate (asymmetric ONU).

200A.1.4 Extensions to subclause 142.3 (PCS receive data path)

In a Super-PON ONU, the PCS receive data path operates in a continuous mode at the 10.3125 GBd rate.

In a Super-PON OLT, the PCS receive data path operates in burst mode at the 10.3125 GBd rate or at the 2.578125 GBd rate.

200A.1.5 Extensions to subclause 142.4.1.1.2 (When generated)

The PCS continuously sends *tx_code_group<256:0>* single data-unit vectors to the PMA according to the PMA transmit clock at either (10.3125/257) GHz or (2.578125/257) GHz as defined in 142.4.4.

200A.1.6 Extensions to subclause 142.4.1.2.2 (When generated)

The PMA continuously sends *rx_code_group<256:0>* single data-unit vectors to the PCS according to the PMA transmit clock at either (10.3125/257) GHz or (2.578125/257) GHz as defined in 142.4.4.

200A.1.7 Extensions to subclause 142.4.4 (PMA transmit clock)

The data conveyed by *PMA_UNITDATA.request()* is a 257-bit vector representing a single data-unit which has been prepared for transmission by the PMA client. For the PMA devices transmitting at 10.3125 GBd, the PMA transmit clock is equal 10.3125 / 257 GHz. For the PMA devices transmitting at 2.578125 GBd, the PMA transmit clock is equal 2.578125 / 257 GHz.

200A.1.8 Extensions to subclause 142.4.4.1 (Loop-timing specifications for ONUs)

For the Super-PON ONUs supporting 2.5G transmission (i.e., asymmetric ONUs), the PMA transmit clock is derived from the PMA receive clock by dividing the latter by 4.

200A.2 Extensions to Nx25G-EPON Reconciliation Sublayer (clause 143) for Super-PON

200A.2.1 Extensions to subclause 143.3.1.1 PLS service primitives

Replace tables 143-1 and 143-2 with tables 200A-1 and 200A-2.

Table 200A–1—Mapping of PLS_DATA.request primitives

MAC operating speed	MCRS channels	Transmit interface	Signals
10 and 2.5 Gb/s	1	XGMII[*0*]	TXD[*0*]<31:0>, TXC[*0*]<3:0> and TX_CLK
25 Gb/s	1	25GMII[*0*]	TXD[*0*]<31:0>, TXC[*0*]<3:0> and TX_CLK
50 Gb/s	2	25GMII[*0*] 25GMII[*1*]	TXD[*0*]<31:0>, TXC[*0*]<3:0> and TX_CLK[a] TXD[*1*]<31:0>, TXC[*1*]<3:0>
Nx25 Gb/s	N	25GMII[*0*] 25GMII[*1*] 25GMII[*2*] ... 25GMII[*N-1*]	TXD[*0*]<31:0>, TXC[*0*]<3:0> and TX_CLK[a] TXD[*1*]<31:0>, TXC[*1*]<3:0> TXD[*2*]<31:0>, TXC[*2*]<3:0> ... TXD[*N-1*]<31:0>, TXC[*N-1*]<3:0>

[a] All transmit 25GMII interfaces share a common clock.

Table 200A–2—Mapping of PLS_DATA.indication primitives

MAC operating speed	MCRS channels	Receive interface	Signals
10 and 2.5 Gb/s	1	XGMII[*0*]	RXD[*0*]<31:0>, RXC[*0*]<3:0> and RX_CLK[*0*]
25 Gb/s	1	25GMII[*0*]	RXD[*0*]<31:0>, RXC[*0*]<3:0> and RX_CLK[*0*]
50 Gb/s	2	25GMII[*0*] 25GMII[*1*]	RXD[*0*]<31:0>, RXC[*0*]<3:0> and RX_CLK[*0*] RXD[*1*]<31:0>, RXC[*1*]<3:0> and RX_CLK[*1*]
Nx25 Gb/s	N	25GMII[*0*] 25GMII[*1*] 25GMII[*2*] ... 25GMII[*N-1*]	RXD[*0*]<31:0>, RXC[*0*]<3:0> and RX_CLK[*0*] RXD[*1*]<31:0>, RXC[*1*]<3:0> and RX_CLK[*1*] RXD[*2*]<31:0>, RXC[*2*]<3:0> and RX_CLK[*2*] .... RXD[*N-1*]<31:0>, RXC[*N-1*]<3:0> and RX_CLK[*N-1*]

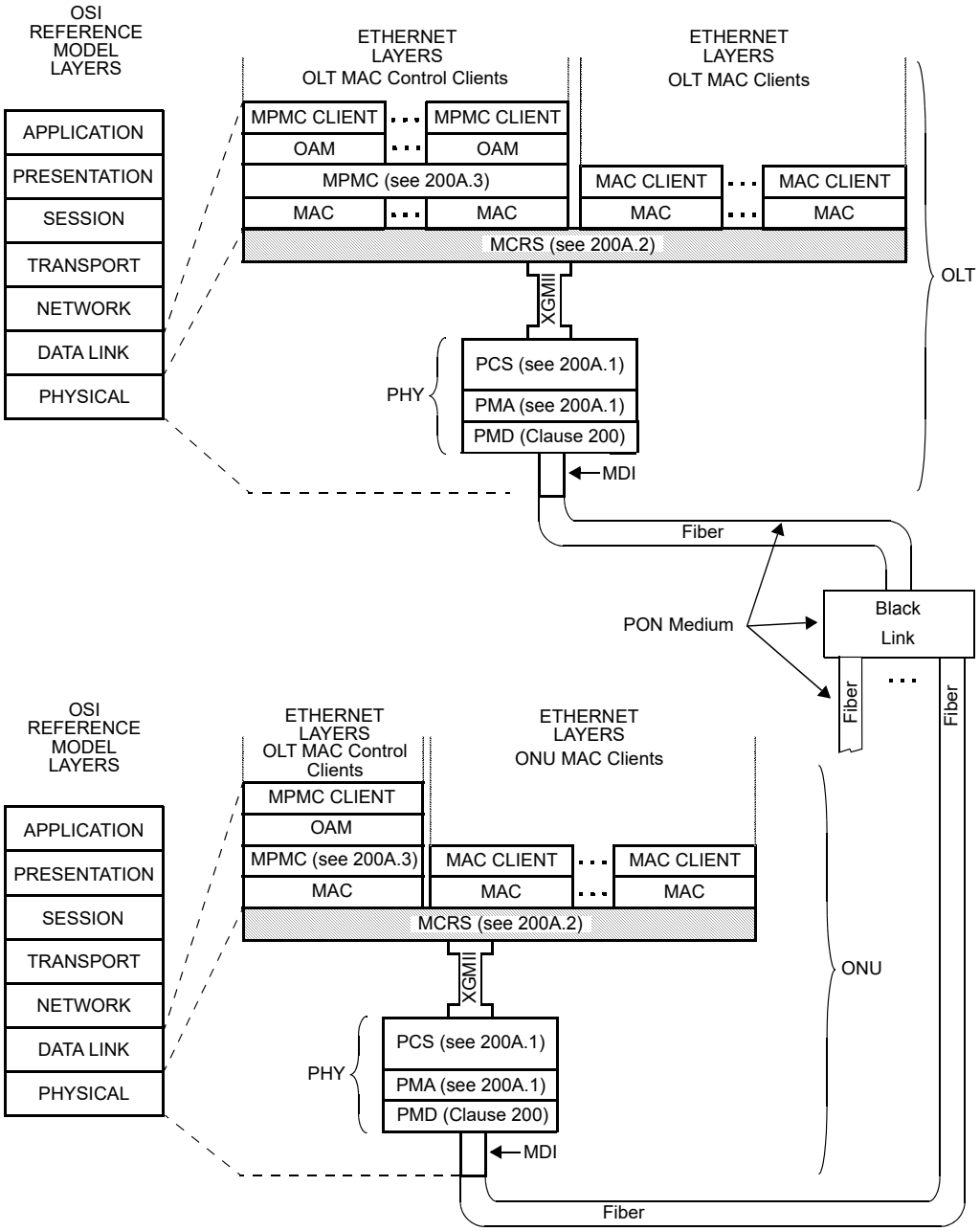
200A.2.2 Extensions to subclause 143.3.1.3 (XGMII interfaces)

The XGMII is specified to support 10 Gb/s and 2.5 Gb/s operation. The structure of each of the XGMII interfaces in an MCRS system is as specified in 46.1.6.

200A.2.3 Super-PON MCRS Requirements (replaces subclause 143.4)

200A.2.3.1 Super-PON architecture

This subclause describes the MCRS requirements for Super-PON networks.



MCRS described in this subclause

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A–2—Relationship of EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

The MCRS is used with Super-PON networks in order to interface one MAC instance with one XGMII channel in each direction. Figure 200A-2 illustrates the relationship of the MCRS and the OSI protocol stack for Super-PON.

200A.2.3.2 MCRS channels

An MCRS channel that carries information from the OLT to the ONU is referred to as the downstream channel, and the channel that carries information from an ONU to the OLT is referred to as the upstream channel.

The Super-PON architecture shall implement a single MCRS channel in each direction. Each MCRS channel is bound to a separate PCS instance via a separate XGMII instance. Thus, for any given system, there is a one-to-one correspondence between the MCRS channel count and the number of XGMII instances supported.

200A.2.3.3 Symmetric and Asymmetric Data Rates

The Super-PON architecture supports symmetric (10G/10G) and asymmetric data rates (10G/2.5G).

In asymmetric systems, the asymmetric data rate is achieved via the MCRS channel rate asymmetry, where a single downstream MCRS channel operates at 10 Gb/s and a single upstream MCRS channel operates at 2.5 Gb/s. Additional details for MCRS implementations supporting the channel rate asymmetry are provided in 200A.2.3.7.

200A.2.3.4 Super-PON application-specific parameters

For definitions of constants, variables, and functions, see 143.3.3 (transmit direction) and 143.3.4 (receive direction).

200A.2.3.4.1 Constants

ADJ_BLOCK_SIZE
: Value: 257

NUM_CH
: Value: 1.

RATE_ADJ_SIZE
: Value: 33

200A.2.3.4.2 Transmit variables

EnvTx
: Description: Since there is no timing jitter or channel skew to be removed at the transmitting device, the size of *EnvTx* buffer may be reduced to only two rows. If this optimization is implemented, the variables *rRow* and *wRow* are represented by 1-bit unsigned integers.

200A.2.3.5 MCRS time synchronization

Same as subclause 143.4.2.

200A.2.3.6 Delay variability constraints

Same as subclause 143.4.3

200A.2.3.7 Asymmetric rate operation

In asymmetric Super-PON systems, downstream transmission uses one channel operating at 10 Gb/s, while the upstream transmission uses one channel operating at 2.5 Gb/s. Figure 200A-3 illustrates the layering diagram of asymmetric Super-PON OLT and ONU. In the OLT, the MCRS sublayer serves MAC entities

supporting the transmit data rate of 10 Gb/s and the receive data rate of 2.5 Gb/s. In the ONU, the MCRS sublayer serves MAC entities supporting the transmit data rate of 2.5 Gb/s and the receive data rate of 10 Gb/s.

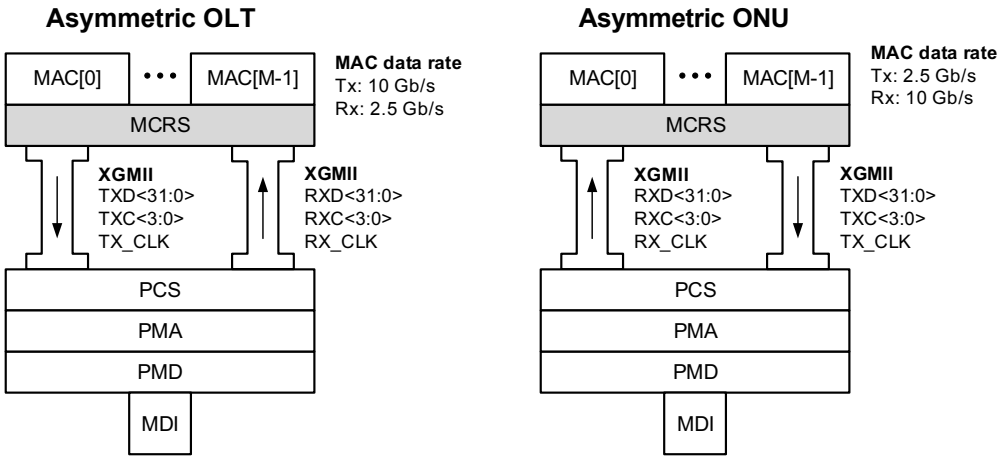


Figure 200A–3—Asymmetric OLT and ONU layering diagram

Because of the required close coupling between the MCRS clock (InClk, see 143.3.3.4 and OutClk, see 143.3.4.3) and MPCP clock (LocalTime, see 144.2.1.2), the MCRS buffer read pointers advance by one every EQT, i.e., both downstream and upstream channels within MCRS operate at a nominal data rate of 10 Gb/s. To adapt the MCRS channel rate to the MAC data rate of 2.5 Gb/s, the MCRS channel is throttled by inserting a padding EQ at the rate of 3 padding EQs per every 4 EQTs. The transfer of information through the 10 Gb/s MCRS channel is illustrated in Figure 200A-4.

The padding EQs are interleaved with information EQs using the following pattern:

<information EQ> <padding EQ> <padding EQ> <padding EQ>.

The usage of the padding EQs is entirely confined to the MCRS sublayer and does not affect the definition of interfaces to either of the adjacent sublayers. Therefore the definition of the padding EQ format and values are left to implementations.

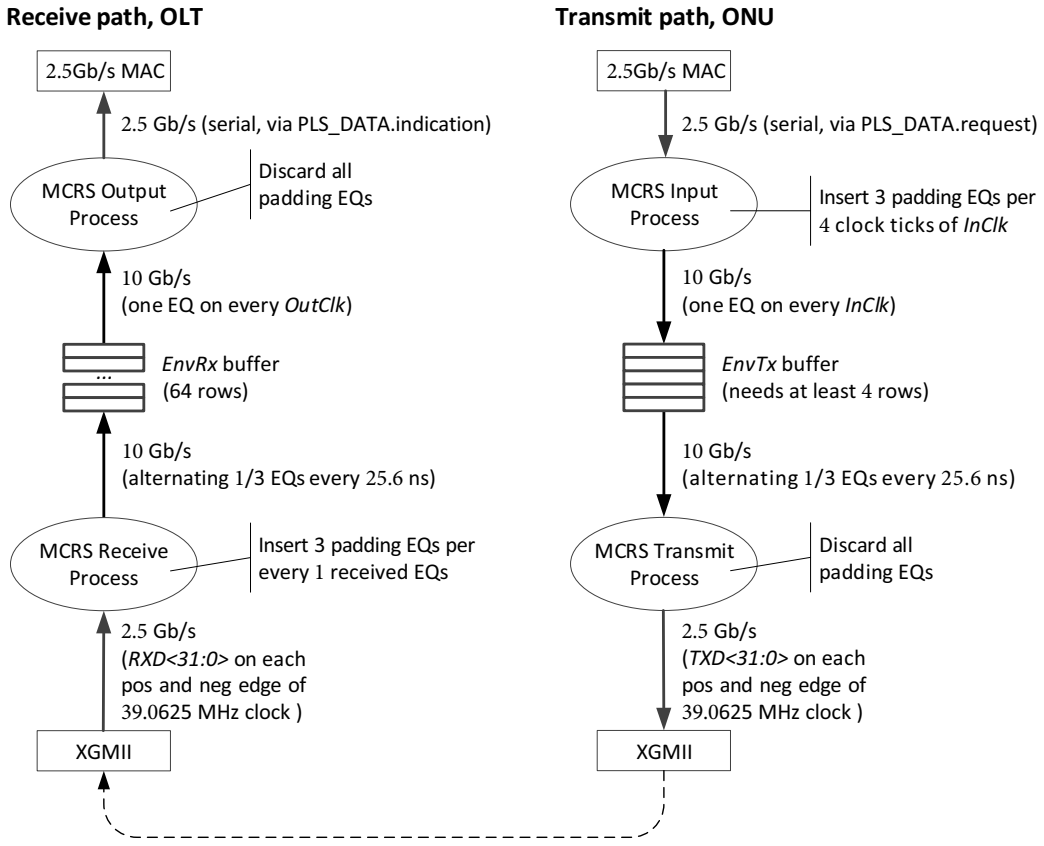
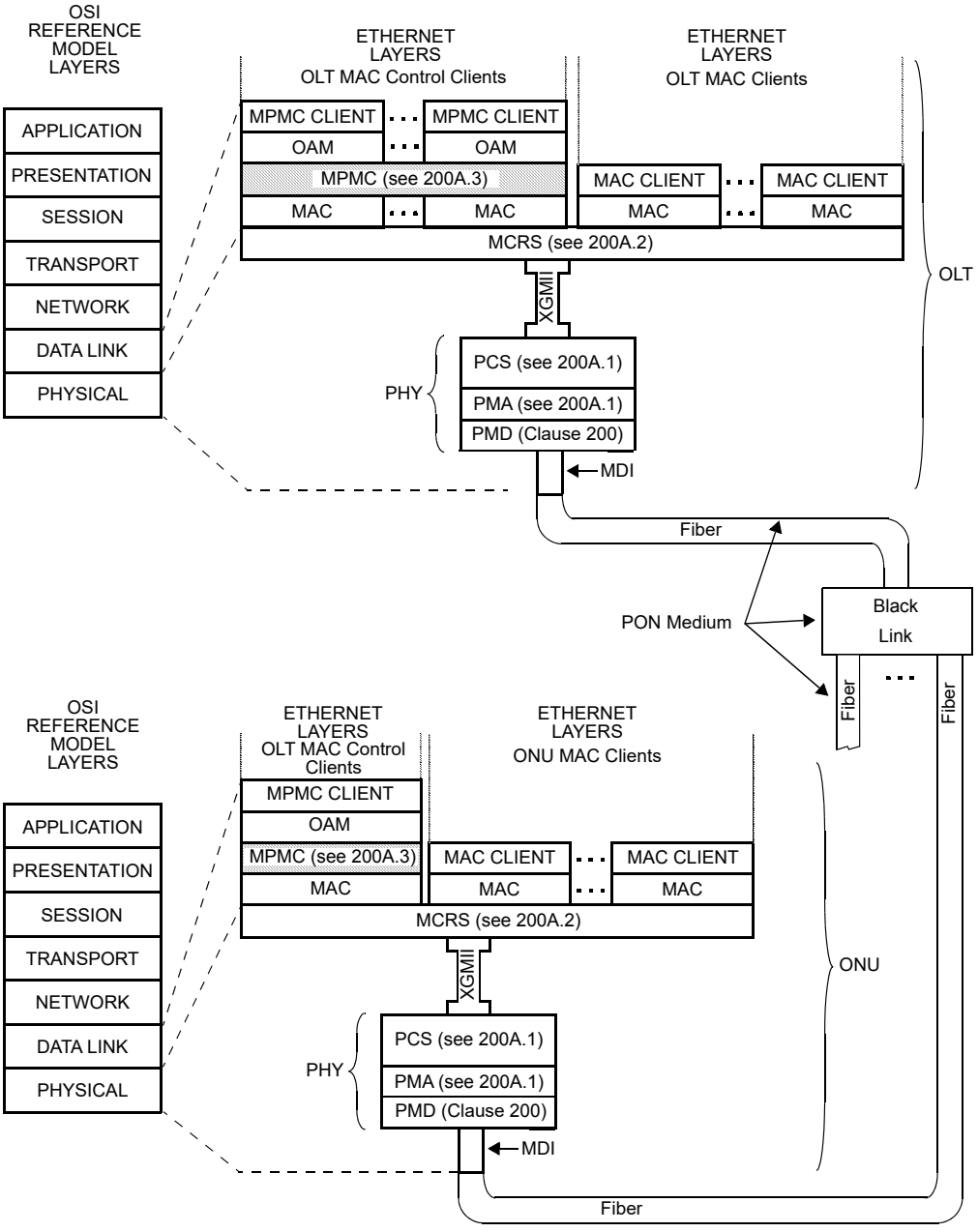


Figure 200A–4—Upstream channel operating at 2.5 Gb/s

200A.3 Extensions to Nx25G-EPON Multipoint MAC Control (clause 144) for Super-PON

200A.3.1 Extensions to subclause 144.1 (Overview)

Replace figure 144-2 with figure 200A-5.



MPMC described in this subclause

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A–5—Relationship of EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

This clause defines the mechanisms and control protocols required in order to reconcile Super-PON networks into the Ethernet framework.

The functions of the Multipoint MAC Control for Super-PON include allocation of transmission resources in EPON, discovery and registration of EPON devices, and reporting queue occupancy to higher layers to facilitate dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

The Multipoint MAC Control (MPMC) sublayer includes two protocols: Multipoint Control Protocol (MPCP) and Channel Control Protocol (CCP). Super-PON does not use the Channel Control Protocol.

200A.3.2 Extensions to subclause 144.2.1.1 (Constants)

DRIFT_THOLD

Type: Integer

Description: This constant holds the maximum amount of drift allowed before a timestamp drift error is declared. Exceeding this drift causes ONU deregistration (either self-deregistration or deregistration by the OLT).

Value: 2 (for the receive channels operating at 10 Gb/s) or 3 (for the receive channels operating at 2.5 Gb/s)

Unit: EQT

200A.3.4 Extensions to subclause 144.2.1.2 (Counters)

LocalTime

Type: 32-bit unsigned

Description: This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 156.25 MHz, and is equivalent to one EQT. At the OLT the counter shall track the XGMII transmit clock, while at the ONU the counter shall track the XGMII receive clock. For accuracy of the receive clock, see 200A.1.8. In the ONU, this variable is updated with the received timestamp value by the Control Parser Process (see 144.2.1.5).

200A.3.5 Extensions to subclause 144.3.1.1 (Ranging Measurement and Time Synchronization)

Both the OLT and the ONU have 32-bit counters (*LocalTime*) that increment by one every EQT. In the OLT, the *LocalTime* counter is synchronized with the OLT XGMII transmit clock and increments synchronously with the *InClk* (see 143.3.3.4). In the ONU, the *LocalTime* counter is synchronized with the XGMII receive clock and increments synchronously with the *OutClk* (see 143.3.3.4). In the ONUs supporting multiple downstream (receive) channels, the *LocalTime* is synchronized with the XGMII receive clock of an active (enabled) channel with the lowest index.

200A.3.6 Extensions to subclause 144.3.3 (Delay variability requirements)

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent; however, a complying implementation shall maintain the combined delay variation through the MAC and PHY of less than one EQT for channels operating at 10.3125 GBd and less than two EQTs for channels operating at 2.578125 GBd.

200A.3.7 Extensions to subclause 144.3.6.3 (REGISTER_REQ description)

Replace table 144-4 with table 200A-3.

Table 200A–3—*RegisterRequestInfo* field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2	ONU is 25G upstream capable	0 – ONU transmitter is not capable of 25 Gb/s 1 – ONU transmitter is capable of 25 Gb/s
3	ONU is 2.5G upstream capable	0 – ONU transmitter is not capable of 2.5 Gb/s 1 – ONU transmitter is capable of 2.5 Gb/s
4	Reserved	Ignored on reception
5	10G registration attempt	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
6	25G registration attempt	0 – ONU transmitter is not capable of 25 Gb/s 1 – ONU transmitter is capable of 25 Gb/s
7	2.5G registration attempt	0 – ONU transmitter is not capable of 2.5 Gb/s 1 – ONU transmitter is capable of 2.5 Gb/s
8:15	Reserved	Ignored on reception

200A.3.8 Extensions to subclause 144.3.6.6 (DISCOVERY description)

Replace table 144-7 with table 200A-4.

Table 200A–4—*DiscoveryInfo* field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	OLT is 10G upstream capable	0 – OLT does not support 10 Gb/s reception 1 – OLT supports 10 Gb/s reception
2	OLT is 25G upstream capable	0 – OLT does not support 25 Gb/s reception 1 – OLT supports 25 Gb/s reception
3	OLT is 2.5G upstream capable	0 – OLT does not support 2.5 Gb/s reception 1 – OLT supports 2.5 Gb/s reception
4	Reserved	Ignored on reception
5	OLT is opening 10G discovery window	0 – OLT cannot receive 10 Gb/s data in this window 1 – OLT can receive 10 Gb/s data in this window
6	OLT is opening 25G discovery window	0 – OLT cannot receive 25 Gb/s data in this window 1 – OLT can receive 25 Gb/s data in this window
7	OLT is opening 2.5G discovery window	0 – OLT cannot receive 2.5 Gb/s data in this window 1 – OLT can receive 2.5 Gb/s data in this window
8:9	Reserved	Ignored on reception
10:13	Channel information	Encodes the channel number the OLT is operating on
14	Coexistence class G	0 – ONUs supporting PMDs coexistence class G are not allowed to register 1 – ONUs supporting PMDs coexistence class G are allowed to register
15	Coexistence class X	0 – ONUs supporting PMDs coexistence class X are not allowed to register 1 – ONUs supporting PMDs coexistence class X are allowed to register

- The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if the bit 5 was set to 0.
- The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 2.5 Gb/s upstream channel if the OLT did not open the 2.5 Gb/s discovery window, i.e., if the bit 7 was set to 0.

The values of the DiscoveryInfo field flags are set by the OLT MPMC client and may change from one discovery attempt to the next. The OLT MPMC client may allow a concurrent registration of ONUs with different rates by setting both bits 5 and 7 to 1. The processing of DiscoveryInfo flags by the ONU and the ONU behavior in dual-rate systems is further specified in 200A.3.11.
Super-PON system do not use bits 14 and 15.

200A.3.9 Extensions to subclause 144.3.7.1 (Constants)

DISCOVERY_MARGIN

Type: Integer
Description: This constant holds the extra margin reserved at the end of a discovery grant to accommodate the largest possible round-trip time on a given ODN. The round-trip time also includes any internal delays in the OLT and ONU, such as FEC encoding and decoding delays.
Value: 78,906 (505 µs for ODN with 50 km reach)
Unit: EQT

200A.3.10 Extensions to subclause 144.3.7.3 (Variables)

Onu10GCapable
Type: Boolean
Description: This variable is set to true if the ONU is capable at transmitting at a line rate of 10.3125 GBd. Otherwise, it is set to false

Onu2.5GCapable
Type: Boolean
Description: This variable is set to true if the ONU is capable at transmitting at a line rate of 2.578125 GBd. Otherwise, it is set to false

RegAllowed
Type: Boolean
Description: This variable is set to true if upon the verification of the various fields of the DISCOVERY MPCPDU, the ONU has determined that it is allowed to transmit a REGISTER_REQ in the current discovery window. The *RegAllowed* is an alias for the following code:

```
RegAllowed =

    // 1) Upstream channel is available
    ((MsgDiscovery.ChannelMap AND ChState) != 0) AND

    // 2) RSSI is within the allowed limits
    OnuRssiLocal ≥ MsgDiscovery.OnuRssiMin AND
    OnuRssiLocal ≤ MsgDiscovery.OnuRssiMax AND
```

```
// 3) 10G discovery is open and ONU is 10G-capable,
// OR (2.5G discovery is open and ONU is 2.5G-capable
// AND the OLT and/or the ONU are not 10G-capable)
// (see Discovery in dual-rate systems, 144.3.7)
((MsgDiscovery.DiscoveryInfo[6] == 1 AND Onu10GCapable) OR
((MsgDiscovery.DiscoveryInfo[5] == 1 AND Onu2.5GCapable) AND
(MsgDiscovery.DiscoveryInfo[2] == 0 OR !Onu10GCapable)));
```

200A.3.11 Discovery Process in dual-rate systems (replaces subclause 144.3.9)

The MPCP Discovery Process (see 144.3.7) facilitates the coexistence of different types of Super-PON ONUs on the same PON. The coexistence mode allows symmetric and asymmetric ONUs to be deployed on the same ODN and to be connected to the same Super-PON OLT.

200A.3.11.1 OLT rate-specific discovery

The DISCOVERY MPCPDU (see 144.3.6.6) includes the *DiscoveryInfo* field, which gives the Super-PON OLT control over the types of ONUs allowed to participate in the given discovery window. Using the *DiscoveryInfo* field, the OLT indicates its receive line rate capabilities (10 Gb/s and/or 2.5 Gb/s) as well as the specific line rate(s) allowed in the given discovery window. The OLT may open separate (non-overlapping) discovery windows for 10 Gb/s and 2.5 Gb/s transmission using two separate DISCOVERY MPCPDUs or it may open a single discovery window for both 10 Gb/s and 2.5 Gb/s line rates using a single DISCOVERY MPCPDU.

Table 200A-5 illustrates the different types of ONUs that may respond to a DISCOVERY MPCPDU with the given settings of the *DiscoveryInfo* sub-fields.

Table 200A-5—DISCOVERY MPCPDUs for Super-PON ONU types

ONU types targeted by DISCOVERY MPCPDU		***DiscoveryInfo* field value**			
		Upstream capable		**Discovery window**	
Symmetric	**Asymmetric**	**10G**	**2.5G**	**10G**	**2.5G**
X		1	0/1	1	0
	X	0/1	1	0	1
X	X	1	1	1	1

200A.3.11.2 ONU rate-specific registration

An unregistered Super-PON ONU is capable of receiving a DISCOVERY MPCPDU transmitted by the OLT on the DISC_PLID. When received by a symmetric Super-PON ONU, the DISCOVERY MPCPDU is parsed, and if a 10 Gb/s discovery window is opened, the ONU may attempt to register, if other conditions are also satisfied (see definition of the RegAllowed variable in 144.3.7.3). When received by an asymmetric Super-PON ONU, the DISCOVERY MPCPDU is parsed, and if a 2.5 Gb/s discovery window is opened, the ONU may attempt to register.

In general, the ONUs attempt to register using the highest upstream transmission rate supported by both the OLT and the ONU. If the OLT advertised itself as 10G-capable, but in the current DISCOVERY MPCPDU it has not enabled the 10 Gb/s discovery window, the 10G-capable ONU skips such discovery attempts and waits for a future discovery window in which 10 Gb/s transmission is enabled.

Table 200A-6 shows the action the ONU shall take based on the ONU transmit capabilities and the received discovery information.

Table 200A-6—ONU action during discovery window

DiscoveryInfo field				ONU upstream capability		ONU action
Upstream capability		Discovery window				
10G	2.5G	10G	2.5G	10G	2.5G	
1	0	1	0	1	0/1	Attempt 10G registration
1	0/1	1	0/1	1	0	Attempt 10G registration
0/1	1	0/1	1	0/1	1	Attempt 2.5G registration
1	1	0	1	1	0	Wait for 10G discovery window
1	1	1	0	0/1	1	Wait for 2.5G discovery window

The ONU transmits the REGISTER_REQ MPCPDU in envelopes with the discovery PLID (DISC_PLID, see 144.3.5).

200A.3.12 Clock tracking (replaces subclause 144.5.4.1)

Item	Feature	Subclause	Value/Comment	Status	Support
CLK1	Clock tracking at OLT	144.2.1.2	*LocalTime* tracks the XGMII transmit clock	OLT:M	Yes [ ] N/A [ ]
CLK2	Clock tracking at ONU	144.2.1.2	*LocalTime* tracks the XGMII receive clock	ONU:M	Yes [ ] N/A [ ]

200A.3.13 MPCP (replaces subclause 144.5.4.4)

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	GATE structure	144.3.6.1	As in Figure 144–12	M	Yes [ ]
MP1a	Grant start time and size	144.3.6.1	Transmission on each channel starts at the ONU's local time equal to the *StartTime* value and has the length as necessary to transmit all allocated envelopes (the sum of all *Env-Length* fields) together with the associated optical and FEC overhead	ONU:M	Yes [ ] N/A [ ]
MP1b	Fragmentation	144.3.6.1	When flag *F* is set to 0, do not fragment new frames	ONU:M	Yes [ ] N/A [ ]
MP1c	Forced report	144.3.6.1	When flag *FR* is set to 1, report the total length of the frames (including IPG and preamble), queued for transmission on this specific LLID	ONU:M	Yes [ ] N/A [ ]
MP1d	MPCPDU fragmentation	144.3.6.1	ONU does not fragment MPCPDU frames, regardless of the value of the *Fragmentation* flag in the *EnvAlloc* structure that allocates a PLID envelope	ONU:M	Yes [ ] N/A [ ]
MP2	REPORT structure	144.3.6.2	As in Figure 144–13	M	Yes [ ]
MP3	REGISTER_REQ structure	144.3.6.3	As in Figure 144–14	M	Yes [ ]
MP4	REGISTER structure	144.3.6.4	As in Figure 144–15	M	Yes [ ]
MP5	REGISTER_ACK structure	144.3.6.5	As in Figure 144–16	M	Yes [ ]
MP6	DISCOVERY structure	144.3.6.6	As in Figure 144–17	M	Yes [ ]
MP6a	Discovery attempt	144.3.6.6	Attempt to register on a single channel only	ONU:M	Yes [ ] N/A [ ]
MP6b	*OnuRssiMin* trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is greater or equal to *OnuRssiMin*	ONU:M	Yes [ ] N/A [ ]
MP6c	*OnuRssiMax* trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is smaller than or equal to *OnuRssiMax*	ONU:M	Yes [ ] N/A [ ]
MP6d	Discovery attempt at 10 Gb/s	144.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if the bit 5 was set to 0	ONU:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MP6e	Discovery attempt at 2.5 Gb/s	144.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 2.5 Gb/s upstream channel if the OLT did not open the 2.5 Gb/s discovery window, i.e., if the bit 7 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP6f	Discovery attempt for ONU supporting coexistence class G	144.3.6.6	ONU does not generate a REGISTER_REQ MPCPDU if the OLT does not allow the G-type coexistence, i.e., if the bit 14 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP6g	Discovery attempt for ONU supporting coexistence class X	144.3.6.6	ONU does not generate a REGISTER_REQ MPCPDU if the OLT does not allow the X-type coexistence, i.e., if the bit 15 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP7	SYNC_PATTERN structure	144.3.6.7	As in Figure 144–18	M	Yes [ ]
MP8	MPCPDU timing on transmit	144.3.1.1	When multiple MPCPDUs are transmitted within a single envelope, all these MPCPDUs have the same *Timestamp* field value, referencing the transmission time of the ESH.	M	Yes [ ]
MP9a	Discovery Initiation in OLT	144.3.7.6	Meets the requirements of Figure 144–20, single instance associated with DISC_PLID	OLT:M	Yes [ ] N/A [ ]
MP9b	Discovery Completion in OLT	144.3.7.7	Meets the requirements of Figure 144–21, one instance for each unicast PLID being registered	OLT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MP9c	Discovery in ONU	144.3.7.8	Meets the requirements of Figure 144–22, single instance	ONU:M	Yes [ ] N/A [ ]
MP10a	GATE Generation	144.3.8.7	Meets the requirements of Figure 144–23, one instance for each registered unicast PLID	OLT:M	Yes [ ] N/A [ ]
MP10b	GATE Reception	144.3.8.8	Meets the requirements of Figure 144–24, single instance	ONU:M	Yes [ ] N/A [ ]
MP11a	Envelope Commitment in OLT	144.3.8.9	Meets the requirements of Figure 144–25, single instance	OLT:M	Yes [ ] N/A [ ]
MP11b	Envelope Commitment in ONU	144.3.8.10	Meets the requirements of Figure 144–26, single instance	ONU:M	Yes [ ] N/A [ ]
MP11c	Envelope Activation	144.3.8.11	Meets the requirements of Figure 144–27, single instance	M	Yes [ ]
MP12	ONU multi-rate discovery	144.3.9.2	ONU takes action based on on the ONU transmit capabilities and the received discovery information, as shown in Table 144–10	ONU:M	Yes [ ] N/A [ ]
MP13	MPCP delay variability	144.3.3	Maintain the combined delay variation through the MAC and PHY of less than three EQT for channels operating at 2.578125 GBd and less than two EQTs for channels operating at 10.3125 GBd	M	Yes [ ]
MP14a	Granting overlapping envelopes to the PLID	144.3.1.2	OLT does not allocate overlapping envelopes to the PLID, except the fully overlapping envelopes (see Figure 143–5)	OLT:M	Yes [ ] N/A [ ]
MP14b	Processing partially overlapping PLID envelope allocations	144.3.1.2	If ONU receives partially overlapping PLID envelope allocations, it chooses only one of these envelopes for MPCPDU transmission, and only if the envelope length is enough for at least one complete MPCPDU	ONU:M	Yes [ ] N/A [ ]