

Normative Annex 200A Proposal

Updates to Clause 1

1.4.245c EQT: The unit of measurement of time for time-related parameters specified in Clause 144 and Clause 200 Multipoint MAC Control. Each EQT is equal to the time required to transmit one EQ between the MCRS and the PCS in the downstream direction. When an EQ is transmitted across 25GMII (Clause 144), the EQT is equal to 2.56 ns. When an EQ is transmitted across XGMII (Clause 200), the EQT is equal to 6.4 ns.

Updates to Clause 200

Replace subclause 200.4.2 with the following:

200.4.2 PMD block diagram

The PMD sublayer is defined at the reference points shown in Figure 200–2 for Super-PON type PMDs, using the ‘black link’ approach.

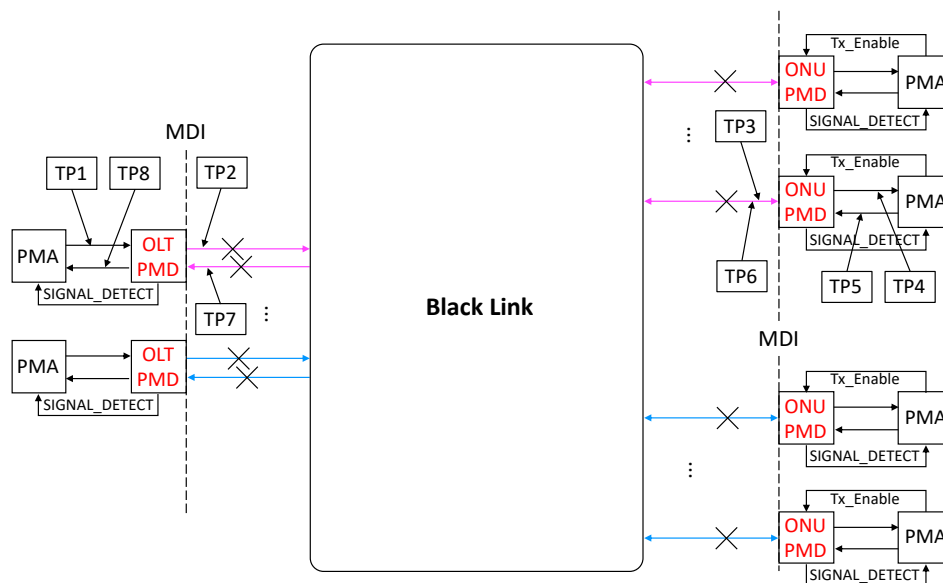


Figure 200-2 – Super-PON PMD test points

Test points TP1, TP2, TP3, and TP4 refer to the downstream channel, while test points TP5, TP6, TP7, and TP8 refer to the upstream channel. In the downstream channel, TP2 and TP3 are compliance points, while in the upstream channel TP6 and TP7 are compliance points. TP1, TP4, TP5, and TP8 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2 for the downstream channel and TP6 for the upstream channel), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 200.9 are made at TP2 or TP6. The optical receive signal is defined at the output of the fiber optic cabling (TP3 for the downstream channel and TP7 for the upstream channel) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 200.9 are made at TP3 or TP7.

The electrical specifications of the PMD service interface (TP1 and TP4 for the downstream channel and TP5 and TP8 for the upstream channel) are not system compliance points (these are not readily testable in a system implementation).

An example of black link implementation is described in Annex 200B.

Annex 200A (Normative)

Physical Coding Sublayer, Physical Media Attachment, Reconciliation Sublayer, and Multipoint MAC Control Sublayer for Super-PON

The Super-PON Physical Coding Sublayer, Physical Media Attachment, Reconciliation Sublayer, and Multipoint MAC Control Sublayer are specified in this annex. They are based on the Nx25G-EPON Physical Coding Sublayer and Physical Media Attachment (see clause 142), Reconciliation Sublayer (see clause 143), and Multipoint MAC Control Sublayer (see clause 144) with scaled down speeds and support for only one ONU channel.

200A.1 Super-PON Physical Coding Sublayer and Physical Media Attachment

200A.1.1 Overview

Subclause 200A.1 describes the Physical Coding Sublayer (PCS) with forward error correction (FEC) and Physical Medium Attachment (PMA) used with Super-PON point-to-multipoint (P2MP) networks (see 200.1). This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in subclause 200A.3 (see Figure 200A-1).

Figure 200A–2 illustrates the functional block diagram of the Super-PON PHY with emphasis placed on the PCS. The Super-PON PCS supports Super-PON PMDs, where:

- both the receive and transmit paths operate at 10.3125 GBd rate (symmetric Super-PON ONU/OLT), or
- the receive path operates at 10.3125 GBd rate and the transmit path operates at 2.578125 GBd (asymmetric Super-PON ONU), or
- the transmit path operates at 10.3125 GBd rate and the receive path operates at 2.578125 GBd (asymmetric Super-PON OLT).

See 46.1.6 for the definition of TXD, TXC, TX_CLK, RXD, RXC, and RX_CLK.

200A.1.1.1 Conventions

See 142.1.1.

200A.1.1.2 Delay constraints

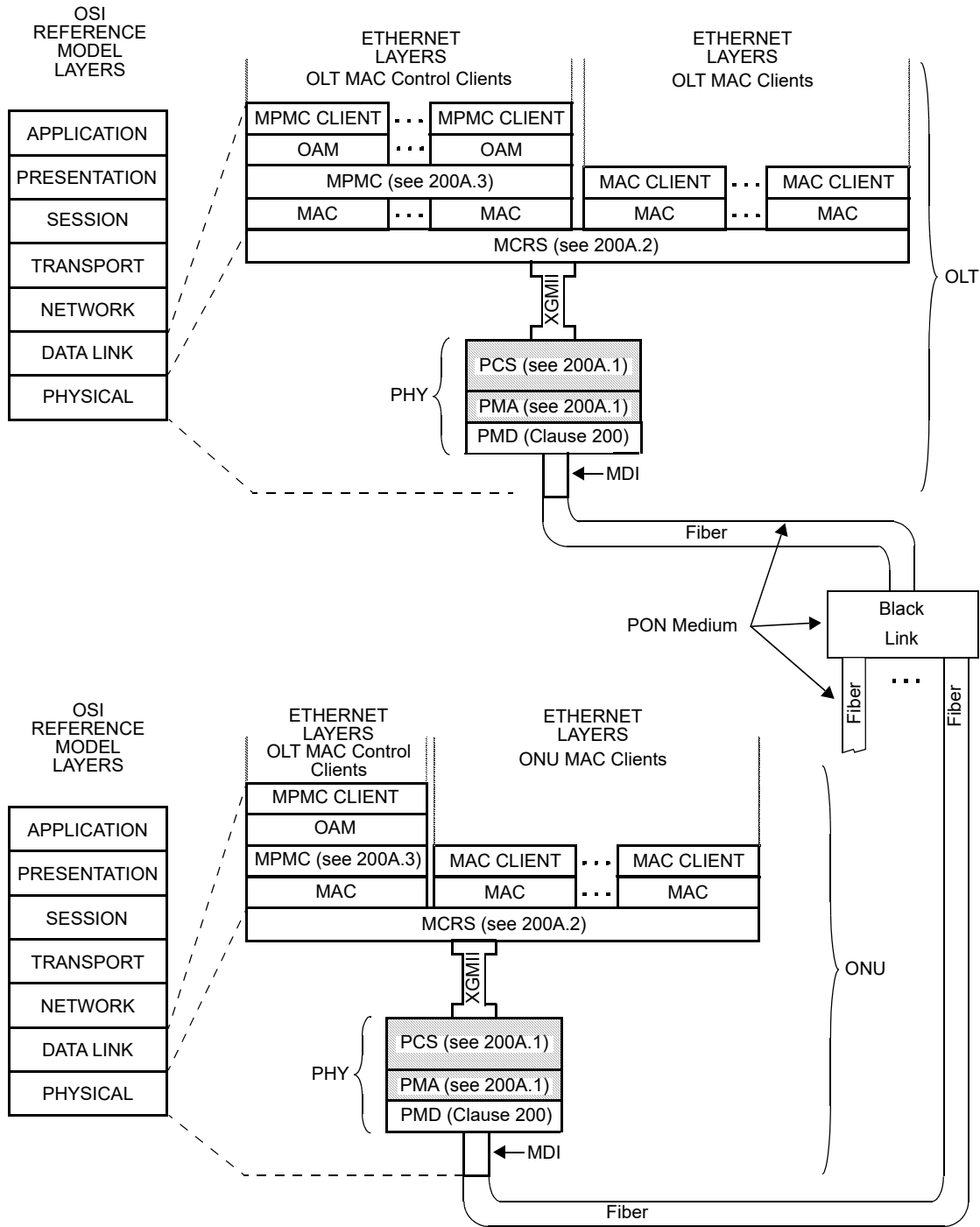
The combined delay variation through the transmit path of the Super-PON PCS and PMA is expected to be less than 6 EQTs (see 1.4.245c) for channels operating at 10.3125 GBd and less than 15 EQTs for channels operating at 2.578125 GBd.

The combined delay variation through the receive path of the Super-PON PCS and PMA is expected to be less than 2 EQTs for channels operating at 10.3125 GBd and less than 5 EQTs for channels operating at 2.578125 GBd.

The aforementioned delay variation limits are applicable only for the data units (either EQ or the corresponding 257-bit block) located at the fixed offset within the FEC codeword.

200A.1.1.3 Burst transmission

See 142.1.3.

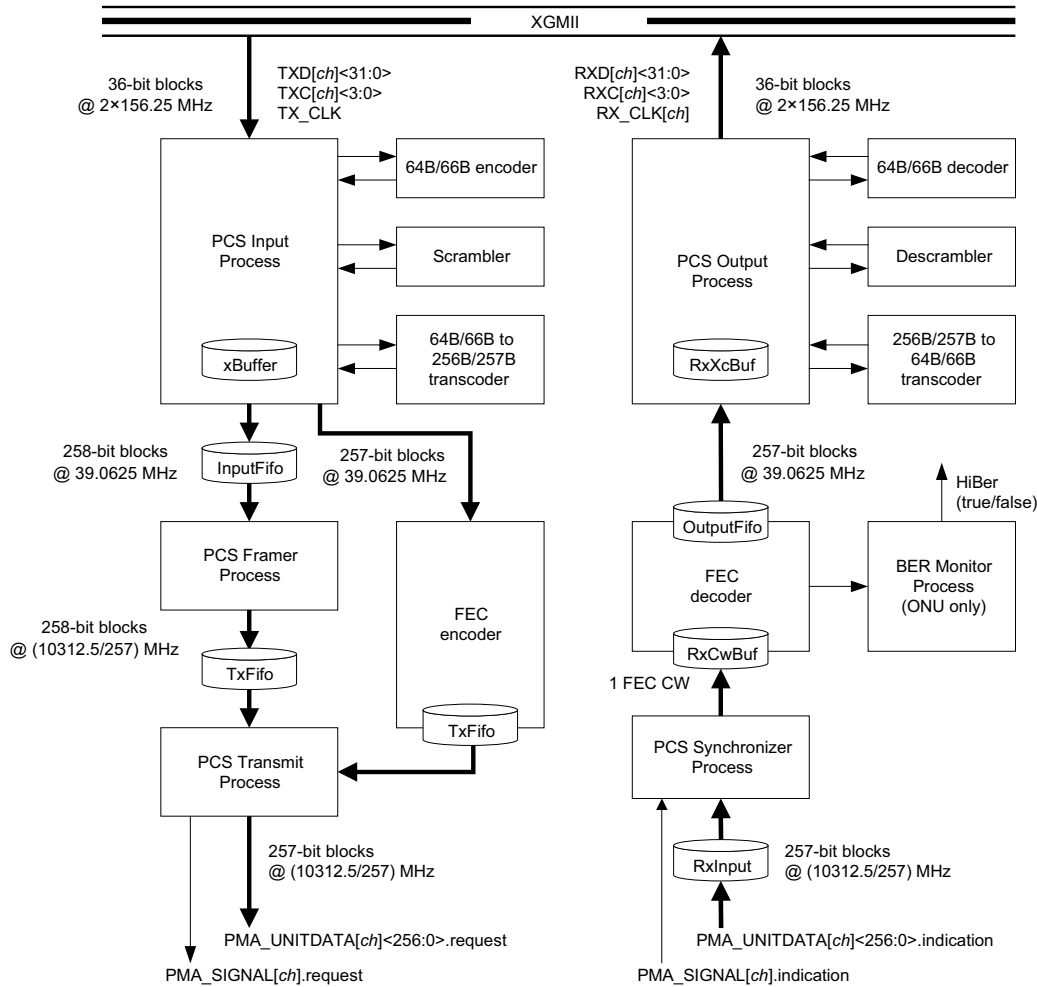


PCS and PMA described in this subclause

- XGMII= 10GIGABIT MEDIA INDEPENDENT INTERFACE
- MDI = MEDIUM DEPENDENT INTERFACE
- OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
- OLT = OPTICAL LINE TERMINAL
- MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
- MPMC= MULTI-POINT MAC CONTROL

- ONU = OPTICAL NETWORK UNIT
- PCS = PHYSICAL CODING SUBLAYER
- PHY = PHYSICAL LAYER DEVICE
- PMA = PHYSICAL MEDIUM ATTACHMENT
- PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A-1—Relationship of the Super-PON PCS and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model



a) PCS transmit path

b) PCS receive path

NOTE—All clock frequencies in this figure are shown for the nominal MAC data rate of 10 Gb/s. For PCS devices supporting the nominal MAC data rate of 2.5 Gb/s, all clock frequencies are scaled down by a multiplicative coefficient of 0.25.

Figure 200A-2—PCS functional block diagram

200A.1.2 PCS transmit data path

The transmit direction of the Super-PON PCS operates as the transmit direction of the Nx25G-EPON PCS specified in subclause 142.2, with the following data rate changes:

- In a Super-PON OLT, the PCS transmit function operates in a continuous mode at the 10.3125 GBd rate;
- In a Super-PON ONU, the PCS transmit function operates in burst mode at the 10.3125 GBd rate (symmetric ONU) or at the 2.578125 GBd rate (asymmetric ONU).

200A.1.3 PCS receive data path

The receive direction of the Super-PON PCS operates as the receive direction of the Nx25G-EPON PCS specified in subclause 142.3, with the following data rate changes:

- In a Super-PON ONU, the PCS receive data path operates in a continuous mode at the 10.3125 GBd rate;
- In a Super-PON OLT, the PCS receive data path operates in burst mode at the 10.3125 GBd rate or at the 2.578125 GBd rate.

200A.1.4 Super-PON PMA

The PMA adapts the serial PMD service interface (PMD_UNITDATA, see 141.3.3 and 141.3.4) to the 257-bit wide interface of the PCS (PMA_UNITDATA, see 142.4.1). The Super-PON PMA sublayer operates over only one channel, therefore it includes only one instance of the transmit data path and/or the receive data path.

In the downstream direction (from the OLT to the ONUs), the PMA includes a differential encoding option (see 142.4.2 and 142.4.3). This encoding technique facilitates the use of lower bandwidth receivers at the ONUs.

200A.1.4.1 Service Interface

The PMA provides a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of 257-bit single data-unit vectors between PCS entities. The PMA converts 257-bit single data-unit vectors into bits and passes these to the PMD, and vice versa.

The following primitives are defined:

- PMA_UNITDATA[*i*].request(tx_code_group<256:0>)
- PMA_UNITDATA[*i*].indication(rx_code_group<256:0>)
- PMA_SIGNAL[*i*].request(tx_enable)
- PMA_SIGNAL[*i*].indication(SIGNAL_OK)

where “[*i*]” is always set to zero to indicate the PMA sublayer operates over only one channel.

200A.1.4.1.1 PMA_UNITDATA[*i*].request

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PCS to the PMA by the PCS Transmit process, see 142.2.

200A.1.4.1.1.1 Semantics of the service primitive

See 142.4.1.1.1

200A.1.4.1.1.2 When generated

The PCS continuously sends *tx_code_group*<256:0> single data-unit vectors to the PMA according to the PMA transmit clock at either (10.3125/257) GHz or (2.578125/257) GHz as defined in 142.4.4.

200A.1.4.1.1.3 Effect of receipt

See 142.4.1.1.3

200A.1.4.1.2 PMA_UNITDATA[*i*]. indication

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PMA to the PCS. PMA_UNITDATA[*i*].indication is used by the PCS receive path processes, see 142.3.5.

200A.1.4.1.2.1 Semantics of the service primitive

See 142.4.1.2.1

200A.1.4.1.2.2 When generated

The PMA continuously sends *rx_code_group*<256:0> single data-unit vectors to the PCS according to the PMA transmit clock at either (10.3125/257) GHz or (2.578125/257) GHz as defined in 142.4.4.

200A.1.4.1.2.3 Effect of receipt

See 142.4.1.2.3.

200A.1.4.1.3 PMA_SIGNAL[j].request

See 142.4.1.3.

200A.1.4.1.4 PMA_SIGNAL[j].indication

See 142.4.1.4.

200A.1.4.2 Differential encoder

See 142.4.2.

200A.1.4.3 Differential decoder

See 142.4.3.

200A.1.4.4 PMA transmit clock

The data conveyed by *PMA_UNITDATA.request()* is a 257-bit vector representing a single data-unit which has been prepared for transmission by the PMA client. For the PMA devices transmitting at 10.3125 GBd, the PMA transmit clock is equal 10.3125 / 257 GHz. For the PMA devices transmitting at 2.578125 GBd, the PMA transmit clock is equal 2.578125 / 257 GHz.

200A.1.4.4.1 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU PMA transmit clock tracks the ONU PMA receive clock. For the Super-PON ONUs supporting 2.5G transmission (i.e., asymmetric ONUs), the PMA transmit clock is derived from the PMA receive clock by dividing the latter by 4.

200A.1.4.5 T_{CDR} measurement**200A.1.4.5.1 Definitions**

Clock and data recovery (CDR) lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when the electrical signal after the PMD at TP8 (see 200.4.2), as illustrated in Figure 200–3, reaches the conditions specified in 200.9.14 for receiver settling time to the moment when the signal phase is recovered and jitter is maintained for an input signal with BER of no worse than 10⁻².

A PMA instantiated in an OLT shall become synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8.

200A.1.4.5.2 Test specification

The test of the OLT PMA receiver T_{CDR} time assumes that there is an optical PMD transmitter at the ONU with a well-known T_{on} time as defined in 200.7.13, and an optical PMD receiver at the OLT with a well-known T_{Rx_settling} time as defined in 200.7.14. After the T_{on} + T_{Rx_settling} time, the parameters at TP8 reach within 15 % of their steady-state values.

Set up the test ONU/OLT test system for 10^{-2} BER. Assuming a 3-zone SP1, SP2, and SP3 upstream ONU burst structure as shown in Figure 142–3, program the ONU SP1 TX pattern length so that the SP1 pattern ends at the precise end of the well-known OLT receiver settling time (within one 257-bit block of SP1, or ~ 10 ns granularity). Starting with the SP2 pattern of zero length (zero 257-bit blocks), test for SP3 detection. If the detection fails, increase the SP2 length by one and repeat the test until SP3 pattern is detected reliably. The number of 257-bit SP2 blocks times the length of each block is the T_{CDR} time, with a margin of error of one 257-bit block time. To reduce hysteresis, increase the number of 257-bit SP2 blocks several hundred nanoseconds beyond this point (20 to 30 additional 257-bit SP2 blocks), and then start decrementing the number of 257-bit SP2 blocks, testing for the SP3 detection at each decrement, until the SP3 SBD is not detected at the OLT. If the SP2 block time counting both forward and backward is less than the specified T_{CDR} maximum time of 400 ns, then the CDR performance meets the requirement.

200A.1.5 Protocol implementation conformance statement (PICS) proforma for subclause 200A.1, Super-PON Physical Coding Sublayer and Physical Media Attachment

The supplier of a protocol implementation that is claimed to conform to subclause 200A.1, Super-PON Physical Coding Sublayer and Physical Media Attachment, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

200A.1.5.2 Identification

200A.1.5.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
<p>NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).</p>	

200A.1.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cs-202x, Subclause 200A.1, Super-PON Physical Coding Sublayer and Physical Media Attachment
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [] Yes [] (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3cs-202x.)	
Date of Statement	

200A.1.5.3 PCS capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Transmission bit order	142.2	Per Figure 142–4	M	Yes []
PCS2	Control code values treated as errors	142.2.1	All control code values that do not appear in Table 142–2 are not to be transmitted and are treated as an error if received	M	Yes []
*OLT	OLT functionality		Device supports functionality required for OLT	O/1	Yes [] No []
*ONU	ONU functionality		Device supports functionality required for ONU	O/1	Yes [] No []

200A.1.5.4 PCS processes

Item	Feature	Subclause	Value/Comment	Status	Support
PSD1	FEC encoder	142.2.4	Encodes the transmitted data stream using a quasi-cyclic QC-LDPC FEC, defined in 142.2.4.1	M	Yes []
PSD1a	FEC codeword shortening	142.2.4.2	Supports FEC shortening	M	Yes []
PSD1b	FEC encoding process	142.2.4.2	Per 142.2.4.2	M	Yes []
PSD2	Input process	142.2.5.4.1	As depicted in Figure 142–9	M	Yes []
PSD3	Framer process	142.2.5.4.2	As depicted in Figure 142–10	M	Yes []
PSD4	Transmit process	142.2.5.4.3	As depicted in Figure 142–11	M	Yes []
PSD5	64B/66B decoder	142.3.4	As depicted in Figure 49–17	M	Yes []
PSD6a	Synchronizer process in OLT	142.3.5.4	As depicted in Figure 142–14, for every enabled receive channel	OLT:M	Yes [] N/A []
PSD6b	Synchronizer process in ONU	142.3.5.5	As depicted in Figure 142–15, for every enabled receive channel	ONU:M	Yes [] N/A []
PSD7	Output process	142.3.5.7	As depicted in Figure 142–17, for every enabled receive channel	M	Yes []
PSD8	PCS ONU BER Monitor process	142.3.5.6	As depicted in Figure 142–16 for every enabled receive channel	ONU:M	Yes [] N/A []

200A.1.5.5 PMA processes

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Differential encoder in OLT	142.4.2	As depicted in Figure 142–18	OLT:M	Yes [] N/A []
PMA2a	Differential decoder in ONU	142.4.3	As depicted in Figure 142–19	ONU:M	Yes [] N/A []
PMA2b	Automatic detection of differential encoding	142.4.3	ONU implements automatic detection of Rx path differential encoding and enables decoder as appropriate	ONU:M	Yes [] N/A []
PMA3	ONU loop-timing	200A.1.4.4.1	ONU PMA transmit clock tracks the ONU PMA receive clock	ONU:M	Yes [] N/A []
PMA4	OLT PMA CDR synchronization time	200A.1.4.5.1	OLT PMA becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8	OLT:M	Yes [] N/A []
PMA5	PMA_SIGNAL[<i>i</i>].request, value in OLT	142.4.1.3	In OLT, this primitive always takes on the value of ON	OLT:M	Yes [] N/A []

200A.2 Super-PON Reconciliation Sublayer

200A.2.1 Overview

The Super-PON Reconciliation Sublayer enables multiple MACs to interface with one XGMII. The Super-PON Reconciliation Sublayer is the same as the Nx25G-EPON Multi-Channel Reconciliation Sublayer (MCRS) using only one xMII interface. Figure 200A-3 shows the relationship between this MCRS and the ISO/IEC OSI reference model.

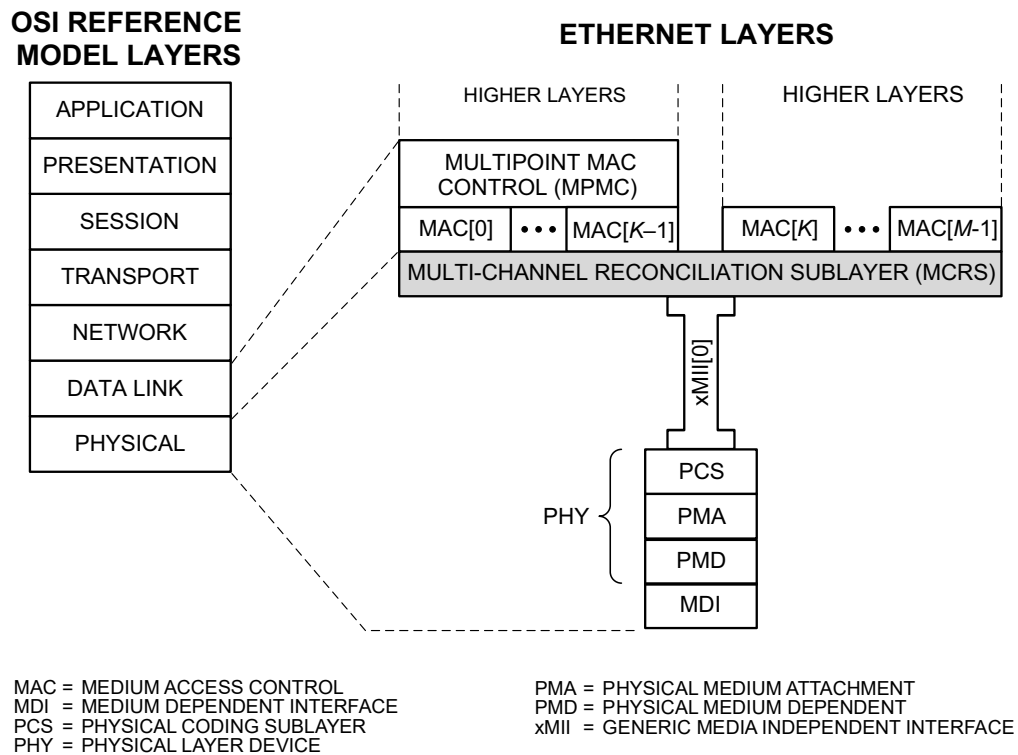


Figure 200A-3—Relationship of MCRS to the OSI reference model

The MCRS adapts the bit-serial protocols of the MAC to the parallel format of the Physical Coding Sublayer (PCS) service interface. Subclause 200A.2 defines an MCRS as an interface between the MAC sublayer and one xMII, where xMII is used as a generic term for the XGMII interface operating at the 10 Gb/s or 2.5 Gb/s speeds.

200A.2.2 Summary of major concepts

See 143.2.

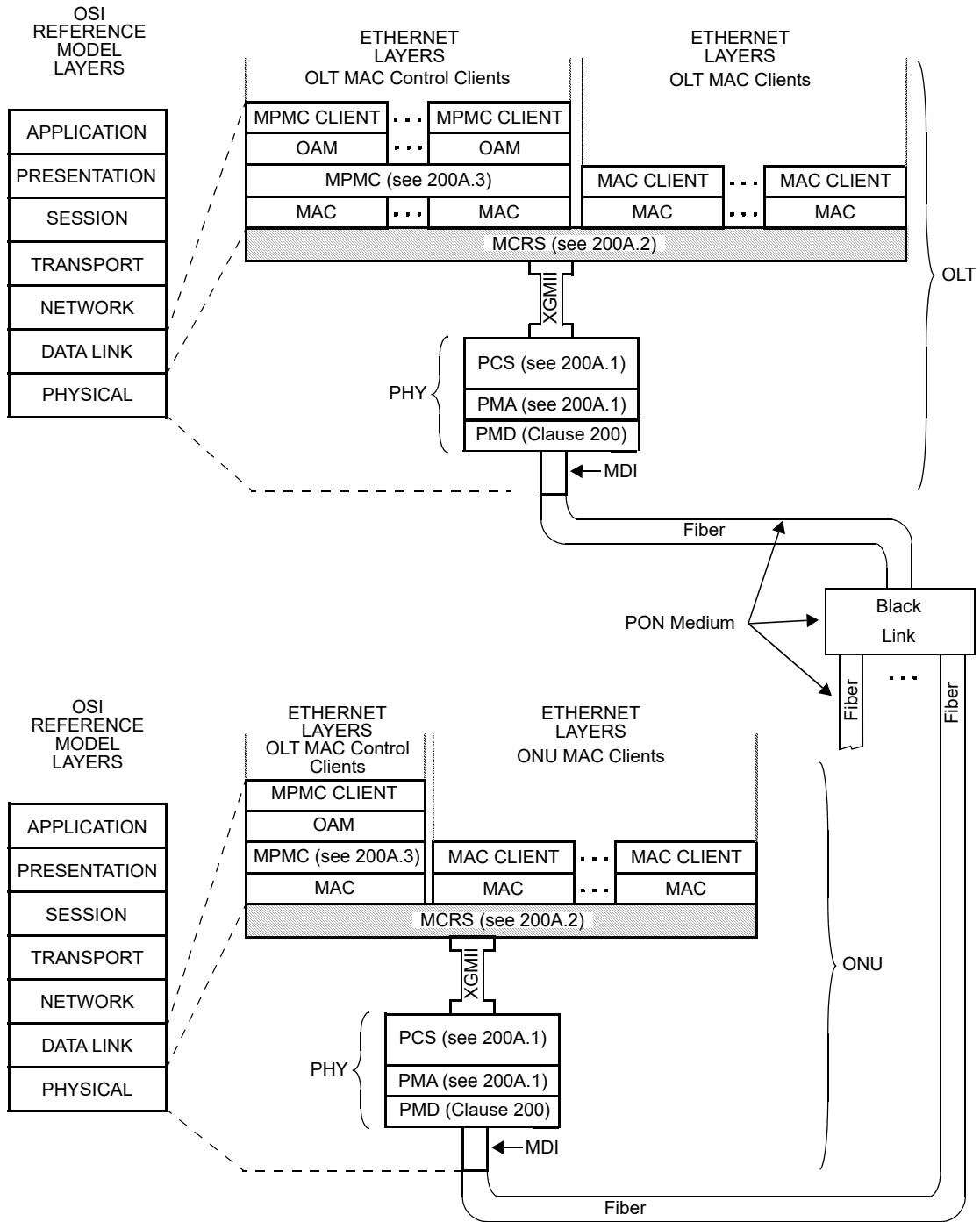
200A.2.3 MCRS functional specifications

See 143.3.

200A.2.4 Super-PON MCRS requirements

200A.2.4.1 Super-PON architecture

This subclause describes the MCRS requirements for Super-PON networks. The MCRS is used with Super-PON networks in order to interface one MAC instance with one XGMII channel in each direction. Figure 200A-4 illustrates the relationship of the MCRS and the OSI protocol stack for Super-PON.



MCRS described in this subclause

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
 MDI = MEDIUM DEPENDENT INTERFACE
 OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
 OLT = OPTICAL LINE TERMINAL
 MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
 MPMC= MULTI-POINT MAC CONTROL

ONU = OPTICAL NETWORK UNIT
 PCS = PHYSICAL CODING SUBLAYER
 PHY = PHYSICAL LAYER DEVICE
 PMA = PHYSICAL MEDIUM ATTACHMENT
 PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A-4—Relationship of Super-PON MCRS to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

200A.2.4.2 MCRCs channels

An MCRCs channel that carries information from the OLT to the ONU is referred to as the downstream channel, and the channel that carries information from an ONU to the OLT is referred to as the upstream channel.

The Super-PON architecture shall implement a single MCRCs channel in each direction. Each MCRCs channel is bound to a separate PCS instance via a separate XGMII instance. Thus, for any given system, there is a one-to-one correspondence between the MCRCs channel count and the number of XGMII instances supported.

200A.2.4.3 Symmetric and Asymmetric Data Rates

The Super-PON architecture supports symmetric (10G/10G) and asymmetric data rates (10G/2.5G).

In asymmetric systems, the asymmetric data rate is achieved via the MCRCs channel rate asymmetry, where a single downstream MCRCs channel operates at 10 Gb/s and a single upstream MCRCs channel operates at 2.5 Gb/s. Additional details for MCRCs implementations supporting the channel rate asymmetry are provided in 200A.2.3.7.

200A.2.4.4 Super-PON application-specific parameters

For definitions of constants, variables, and functions, see 143.3.3 (transmit direction) and 143.3.4 (receive direction).

200A.2.4.4.1 Constants

ADJ_BLOCK_SIZE
Value: 257

NUM_CH
Value: 1.

RATE_ADJ_SIZE
Value: 33

200A.2.4.4.2 Transmit variables

EnvTx

Description: Since there is no timing jitter or channel skew to be removed at the transmitting device, the size of *EnvTx* buffer may be reduced to only two rows. If this optimization is implemented, the variables *rRow* and *wRow* are represented by 1-bit unsigned integers.

200A.2.4.5 MCRCs time synchronization

See 143.4.2.

200A.2.4.6 Delay variability constraints

See 143.4.3.

200A.2.4.7 Asymmetric rate operation

In asymmetric Super-PON systems, downstream transmission uses one channel operating at 10 Gb/s, while the upstream transmission uses one channel operating at 2.5 Gb/s. Figure 200A-5 illustrates the layering diagram of asymmetric Super-PON OLT and ONU. In the OLT, the MCRCs sublayer serves MAC entities supporting the transmit data rate of 10 Gb/s and the receive data rate of 2.5 Gb/s. In the ONU, the MCRCs sublayer serves MAC entities supporting the transmit data rate of 2.5 Gb/s and the receive data rate of 10 Gb/s.

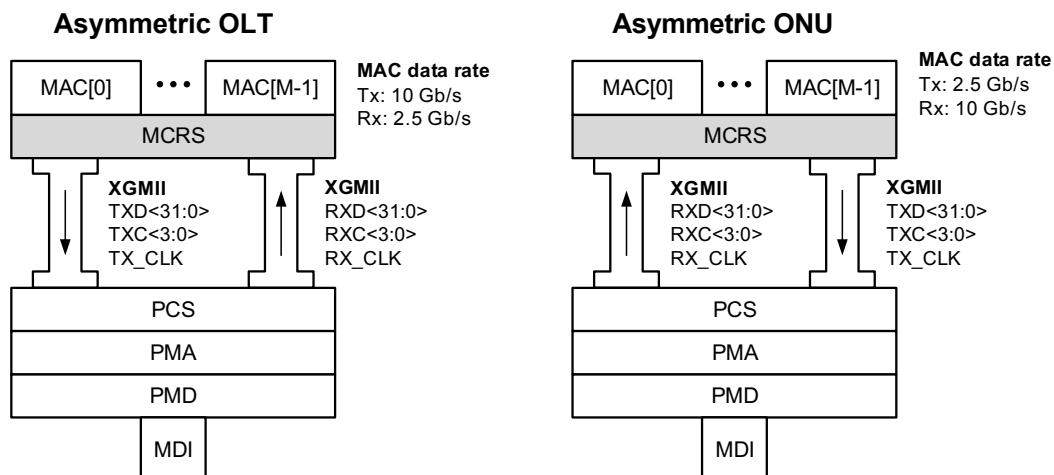


Figure 200A-5—Asymmetric OLT and ONU layering diagram

Because of the required close coupling between the MCRS clock (InClk, see 143.3.3.4 and OutClk, see 143.3.4.3) and MPCP clock (LocalTime, see 144.2.1.2), the MCRS buffer read pointers advance by one every EQT, i.e., both downstream and upstream channels within MCRS operate at a nominal data rate of 10 Gb/s. To adapt the MCRS channel rate to the MAC data rate of 2.5 Gb/s, the MCRS channel is throttled by inserting a padding EQ at the rate of 3 padding EQs per every 4 EQTs. The transfer of information through the 10 Gb/s MCRS channel is illustrated in Figure 200A-6.

The padding EQs are interleaved with information EQs using the following pattern:

<information EQ> <padding EQ> <padding EQ> <padding EQ>.

The usage of the padding EQs is entirely confined to the MCRS sublayer and does not affect the definition of interfaces to either of the adjacent sublayers. Therefore the definition of the padding EQ format and values are left to implementations.

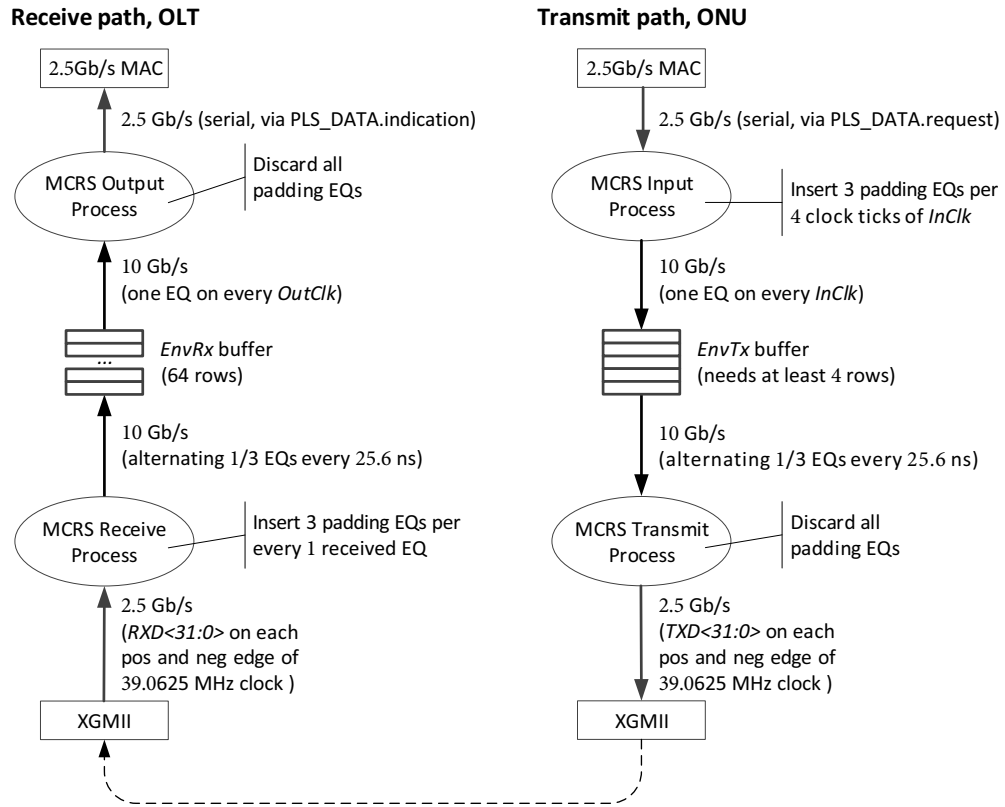


Figure 200A-6—Upstream channel operating at 2.5 Gb/s

200A.2.5 Protocol implementation conformance statement (PICS) proforma for subclause 200A.2, Super-PON Reconciliation Sublayer

The supplier of a protocol implementation that is claimed to conform to subclause 200A.2, Super-PON Reconciliation Sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

200A.2.5.2 Identification

200A.2.5.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
<p>NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).</p>	

200A.2.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cs-202x, Subclause 200A.2, Super-PON Reconciliation Sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No <input type="checkbox"/> Yes <input type="checkbox"/> (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3cs-202x.)	
Date of Statement	

200A.2.5.3 Generic MCRS

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	Envelope header structure	143.3.2	Uses the format shown in Figure 143–10	M	Yes []
MC2	Input process	143.3.3.6.1	Implements the state diagram as depicted in Figure 143–12	M	Yes []
MC3	Transmit process	143.3.3.6.2	Implements the state diagram as depicted in Figure 143–13	M	Yes []
MC4	Receive process	143.3.4.5.1	Implements the state diagram as depicted in Figure 143–15	M	Yes []
MC5	Output process	143.3.4.5.2	Implements the state diagram as depicted in Figure 143–16	M	Yes []

200A.2.5.4 MCRS in Super-PON**200A.2.5.4.1 Major capabilities/option**

Item	Feature	Subclause	Value/Comment	Status	Support
*102.5G	10/2.5G-EPON functionality	200A.2.4.3.	Device supports functionality required for 10/2.5G-EPON	O.1	Yes [] No []
*1010G	10/10G-EPON functionality	200A.2.4.3	Device supports functionality required for 10/10G-EPON	O.1	Yes [] No []

200A.2.5.4.2 MCRS implementation in Super-PON

Item	Feature	Subclause	Value/Comment	Status	Support
EPON1	Number of MCRS channels	200A.2.4.2	Implement a single channel in downstream direction and a single channel in upstream direction	102.5G:M or 1010G:M	Yes [] N/A []

200A.3 Super-PON Multipoint MAC Control Sublayer

200A.3.1 Overview

Subclause 200A.3 defines the mechanisms and control protocols required in order to reconcile Super-PON point-to-multipoint (P2MP) networks (see 200.1) into the Ethernet framework.

The Multipoint MAC Control (MPMC) sublayer defined in subclause 200A.3 includes the Multipoint Control Protocol (MPCP) responsible for arbitration of TDM-based access to the point-to-multipoint (P2MP) medium. The MPMC functionality shall be implemented for subscriber access devices containing point-to-multipoint (P2MP) Physical Layer devices defined in Clause 200.

Figure 200A–7 illustrates the functional block diagram of Super-PON OLT and ONUs with emphasis placed on the MPMC.

200A.3.1.1 Principles of point-to-multipoint operation

See 144.1.1.

200A.3.1.2 Position of Multipoint MAC Control (MPMC) within the IEEE 802.3 hierarchy

Figure 200A–7 depicts the architectural positioning of the MPMC sublayer with respect to the MAC and the MPMC client. The MPMC sublayer extends the MAC Control sublayer to support multiple clients and additional MAC control functionality.

200A.3.1.3 Functional block diagram

See 144.1.3.

Note: Super-PON does not use the Channel Control Protocol (CCP) defined for Nx25G-EPON.

200A.3.1.4 Service interfaces

See 144.1.4.

200A.3.1.5 Conventions

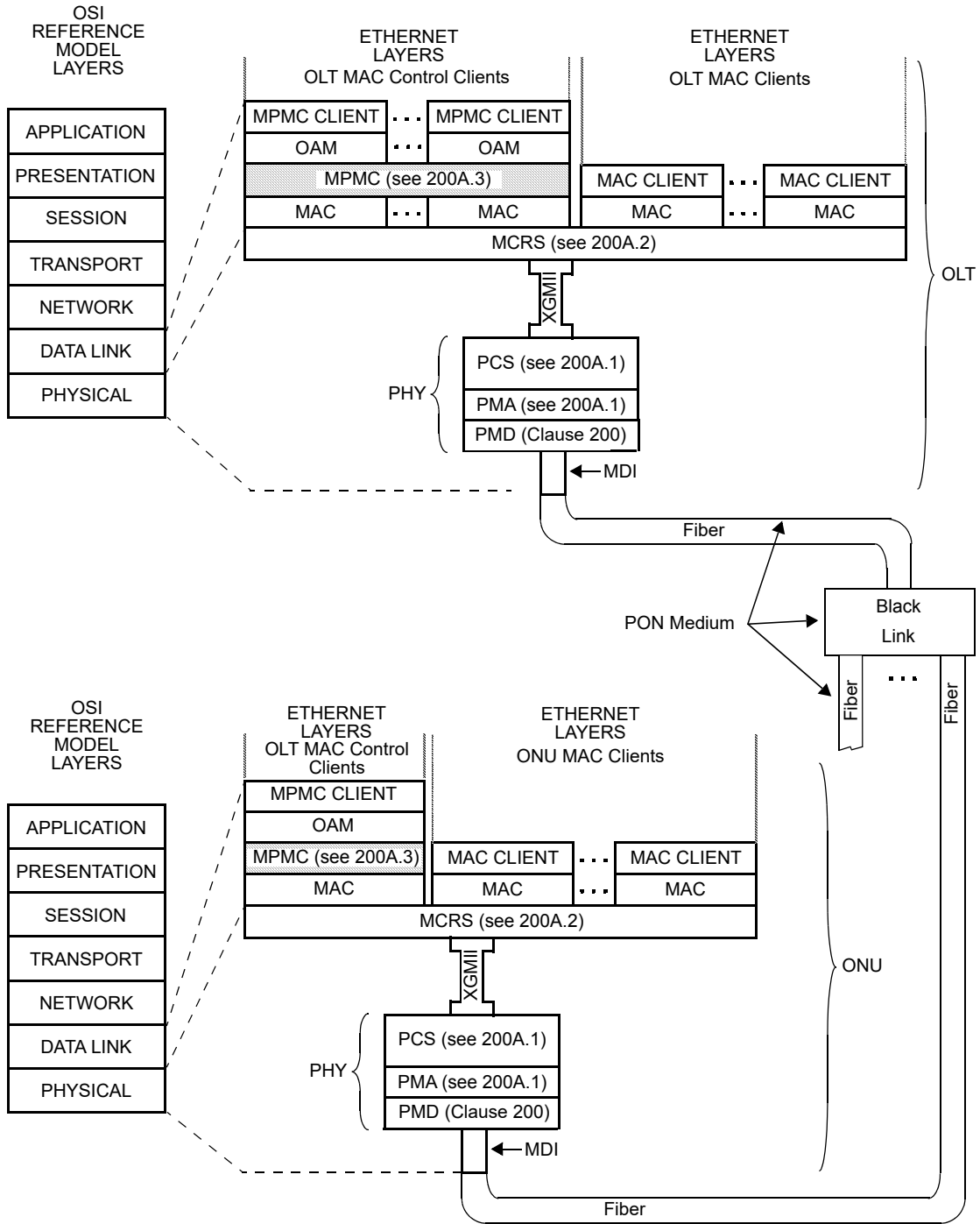
See 142.1.1.

200A.3.2 Protocol-independent operation

200A.3.2.1 Control Parser and Control Multiplexer

The Control Parser (see Figure 144–5) is responsible for opcode-independent parsing of MAC frames and forwarding these frames to other processes for opcode-specific operations. The Control Parser also extracts the value of the Timestamp field from all MPCPDUs that contain this field and checks whether the timestamp drift value is within the acceptable range. There are no interfaces connecting the Control Parser to MAC Clients.

The Control Multiplexer (see Figure 144–6) is responsible for forwarding frames received from multiple opcode-specific processes to the underlying MAC sublayer. The Control Multiplexer inserts the timestamp value into all MPCPDUs that carry the Timestamp field. There are no interfaces connecting the Control Multiplexer to MAC Clients.



MPMC described in this subclause

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
 MDI = MEDIUM DEPENDENT INTERFACE
 OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
 OLT = OPTICAL LINE TERMINAL
 MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
 MPMC= MULTI-POINT MAC CONTROL

ONU = OPTICAL NETWORK UNIT
 PCS = PHYSICAL CODING SUBLAYER
 PHY = PHYSICAL LAYER DEVICE
 PMA = PHYSICAL MEDIUM ATTACHMENT
 PMD = PHYSICAL MEDIUM DEPENDENT

Figure 200A-7—Relationship of Super-PON MPMC to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

200A.3.2.1.1 Constants**DRIFT_THOLD**

Type: Integer

Description: This constant holds the maximum amount of drift allowed before a timestamp drift error is declared. Exceeding this drift causes ONU deregistration (either self-deregistration or deregistration by the OLT).

Value: 2 (for the receive channels operating at 10 Gb/s) or 3 (for the receive channels operating at 2.5 Gb/s)

Unit: EQT

200A.3.2.1.2 Counters**LocalTime**

Type: 32-bit unsigned

Description: This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 156.25 MHz, and is equivalent to one EQT. At the OLT the counter shall track the XGMII transmit clock, while at the ONU the counter shall track the XGMII receive clock. For accuracy of the receive clock, see 200A.1.4.4.1. In the ONU, this variable is updated with the received timestamp value by the Control Parser Process (see 144.2.1.5).

200A.3.2.1.3 Variables

See 144.2.1.3.

200A.3.2.1.4 Functions

See 144.2.1.4.

200A.3.2.1.5 Control Parser state diagram

See 144.2.1.5.

200A.3.2.1.6 Control Multiplexer state diagram

See 144.2.1.6.

200A.3.3 Multipoint Control Protocol (MPCP)**200A.3.3.1 Principles of Multipoint Control Protocol (MPCP)**

See 144.3.1.

200A.3.3.1.1 Ranging measurement and time synchronization

Ranging measurement and time synchronization are specified in 144.3.1.1. For Super-PON:

- In the OLT, the LocalTime counter is synchronized with the OLT XGMII transmit clock and increments synchronously with InClk (see 143.3.3.4).
- In the ONU, the LocalTime counter is synchronized with the XGMII receive clock and increments synchronously with OutClk (see 143.3.3.4).

200A.3.3.1.2 Granting access to the PON media by the OLT

See 144.3.1.2.

200A.3.3.2 MPCP block diagram

See 144.3.2.

200A.3.3.3 Delay variability requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent; however, a complying implementation shall maintain the combined delay variation through the MAC and PHY of less than one EQT for channels operating at 10.3125 GBd and less than two EQTs for channels operating at 2.578125 GBd.

200A.3.3.4 Logical link identifier (LLID) types

See 144.3.4.

200A.3.3.5 Allocation of LLID values

See 144.3.5.

200A.3.3.6 MPCPDU structure and encoding

See 144.3.6.

200A.3.3.6.1 GATE description

The GATE message is specified in 144.3.6.1. Super-PON uses only upstream channel 0 in the ChannelMap bits (see Table 144-2).

200A.3.3.6.2 REPORT description

See 144.3.6.2.

200A.3.3.6.3 REGISTER_REQ description

The REGISTER_REQ message is specified in 144.3.6.3. For Super-PON the RegisterRequestInfo field has the structure shown in Table 200A-1.

Table 200A-1—RegisterRequestInfo field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2	Reserved	Ignored on reception
3	ONU is 2.5G upstream capable	0 – ONU transmitter is not capable of 2.5 Gb/s 1 – ONU transmitter is capable of 2.5 Gb/s
4	Reserved	Ignored on reception
5	10G registration attempt	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
6	Reserved	Ignored on reception
7	2.5G registration attempt	0 – ONU transmitter is not capable of 2.5 Gb/s 1 – ONU transmitter is capable of 2.5 Gb/s
8:15	Reserved	Ignored on reception

200A.3.3.6.4 REGISTER description

See 144.3.6.4.

200A.3.3.6.5 REGISTER_ACK description

See 144.3.6.5.

200A.3.3.6.6 DISCOVERY description

The DISCOVERY message is specified in 144.3.6.6. For Super-PON the DiscoveryInfo field has the structure shown in Table 200A-2.

Table 200A-2—DiscoveryInfo field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	OLT is 10G upstream capable	0 – OLT does not support 10 Gb/s reception 1 – OLT supports 10 Gb/s reception
2	Reserved	Ignored on reception
3	OLT is 2.5G upstream capable	0 – OLT does not support 2.5 Gb/s reception 1 – OLT supports 2.5 Gb/s reception
4	Reserved	Ignored on reception
5	OLT is opening 10G discovery window	0 – OLT cannot receive 10 Gb/s data in this window 1 – OLT can receive 10 Gb/s data in this window
6	Reserved	Ignored on reception
7	OLT is opening 2.5G discovery window	0 – OLT cannot receive 2.5 Gb/s data in this window 1 – OLT can receive 2.5 Gb/s data in this window
8:9	Reserved	Ignored on reception
10:13	Super-PON Channel information	Encodes the channel number (see Table 200-4) the OLT is operating on
14:15	Reserved	Ignored on reception

The flags in the DiscoveryInfo field allow the OLT to exercise discovery admission control over the unregistered ONUs. Specifically, the following ONU behavior is defined:

- The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if bit 5 was set to 0.
- The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 2.5 Gb/s upstream channel if the OLT did not open the 2.5 Gb/s discovery window, i.e., if bit 7 was set to 0.

The values of the DiscoveryInfo field flags are set by the OLT MPMC client and may change from one discovery attempt to the next. The OLT MPMC client may allow a concurrent registration of ONUs with different rates by setting both bits 5 and 7 to 1. The processing of DiscoveryInfo flags by the ONU and the ONU behavior in dual-rate systems is further specified in 200A.3.3.9.

200A.3.3.6.7 SYNC_PATTERN description

See 144.3.6.7.

200A.3.3.7 Discovery process

See 144.3.7.

200A.3.3.7.1 Constants

ACK_GATE_LIMIT

As defined in 144.3.7.2.

DISCOVERY_MARGIN

Type: Integer

Description: This constant holds the extra margin reserved at the end of a discovery grant to accommodate the largest possible round-trip time on a given ODN. The round-trip time also includes any internal delays in the OLT and ONU, such as FEC encoding and decoding delays.

Value: 78,906 (505 μ s for ODN with 50 km reach)

Unit: EQT

MISSED_REPORT_LIMIT

As defined in 144.3.7.2.

REQ_LENGTH

As defined in 144.3.7.2.

SP_COUNT

As defined in 144.3.7.2.

200A.3.3.7.2 Counters

See 144.3.7.2.

200A.3.3.7.3 Variables

BEGIN

As defined in 144.3.7.3.

ChState

Type: Array of eight Boolean values

Description: The value of this variable represents a binary-encoded status of upstream channels at the ONU. Super-PON uses only one channel at the ONU, therefore bit 0 shall be always set to 1 (i.e., channel enabled) and bits 1 through 7 shall be set to 0. The value of each bit has the following meaning:

1 = channel is enabled

0 = channel is disabled

DeregistrationTrigger

As defined in 144.3.7.3.

GrantEndTime

As defined in 144.3.7.3.

GrantMargin

As defined in 144.3.7.3.

MaxDelay

As defined in 144.3.7.3.

MissedReportCount

As defined in 144.3.7.3

Onu10GCapable

Type: Boolean

Description: This variable is set to true if the ONU is capable at transmitting at a line rate of 10.3125 GBd. Otherwise, it is set to false

Onu2_5GCapable

Type: Boolean

Description: This variable is set to true if the ONU is capable at transmitting at a line rate of 2.578125 GBd. Otherwise, it is set to false

OnuRssiLocal

As defined in 144.3.7.3.

RegAllowed

Type: Boolean

Description: This variable is set to true if upon the verification of the various fields of the DISCOVERY MPCPDU, the ONU has determined that it is allowed to transmit a REGISTER_REQ in the current discovery window. The *RegAllowed* is an alias for the following code:

RegAllowed =

```

// 1) Upstream channel is available
((MsgDiscovery.ChannelMap AND ChState) != 0) AND

// 2) RSSI is within the allowed limits
OnuRssiLocal ≥ MsgDiscovery.OnuRssiMin AND
OnuRssiLocal ≤ MsgDiscovery.OnuRssiMax AND

// 3) 10G discovery is open and ONU is 10G-capable,
// OR (2.5G discovery is open and ONU is 2.5G-capable
// AND the OLT and/or the ONU are not 10G-capable)
// (see Discovery in dual-rate systems, 200A.3.3.9)
((MsgDiscovery.DiscoveryInfo[6] == 1 AND Onu10GCapable) OR
(MsgDiscovery.DiscoveryInfo[5] == 1 AND Onu2_5GCapable) AND
(MsgDiscovery.DiscoveryInfo[2] == 0 OR !Onu10GCapable));

```

Registered

As defined in 144.3.7.3.

RegStart

As defined in 144.3.7.3.

SpSeq

As defined in 144.3.7.3.

200A.3.3.7.4 Functions

See 144.3.7.4.

200A.3.3.7.5 Messages

See 144.3.7.5.

200A.3.3.7.6 Discovery Initiation state diagram

See 144.3.7.6.

200A.3.3.7.7 Registration Completion state diagram

See 144.3.7.7.

200A.3.3.7.8 ONU Registration state diagram

See 144.3.7.8.

200A.3.3.8 Granting process

See 144.3.8.

200A.3.3.9 Discovery process in dual-rate systems

The MPCP Discovery Process (see 200A.3.3.7) facilitates the coexistence of different types of Super-PON ONUs on the same PON. The coexistence mode allows symmetric and asymmetric ONUs to be deployed on the same ODN and to be connected to the same Super-PON OLT.

200A.3.3.9.1 OLT rate-specific discovery

The DISCOVERY MPCPDU (see 200A.3.3.6.6) includes the *DiscoveryInfo* field, which gives the Super-PON OLT control over the types of ONUs allowed to participate in the given discovery window. Using the *DiscoveryInfo* field, the OLT indicates its receive line rate capabilities (10 Gb/s and/or 2.5 Gb/s) as well as the specific line rate(s) allowed in the given discovery window. The OLT may open separate (non-overlapping) discovery windows for 10 Gb/s and 2.5 Gb/s transmission using two separate DISCOVERY MPCPDUs or it may open a single discovery window for both 10 Gb/s and 2.5 Gb/s line rates using a single DISCOVERY MPCPDU.

Table 200A-3 illustrates the different types of ONUs that may respond to a DISCOVERY MPCPDU with the given settings of the *DiscoveryInfo* sub-fields.

Table 200A-3—DISCOVERY MPCPDUs for Super-PON ONU types

ONU types targeted by DISCOVERY MPCPDU		<i>DiscoveryInfo</i> field value			
		Upstream capable		Discovery window	
Symmetric	Asymmetric	10G	2.5G	10G	2.5G
X		1	0/1	1	0
	X	0/1	1	0	1
X	X	1	1	1	1

200A.3.3.9.2 ONU rate-specific registration

An unregistered Super-PON ONU is capable of receiving a DISCOVERY MPCPDU transmitted by the OLT on the DISC_PLID. When received by a symmetric Super-PON ONU, the DISCOVERY MPCPDU is parsed, and if a 10 Gb/s discovery window is opened, the ONU may attempt to register, if other conditions are also satisfied (see definition of the RegAllowed variable in 200A.3.3.7.3). When received by an asymmetric Super-PON ONU, the DISCOVERY MPCPDU is parsed, and if a 2.5 Gb/s discovery window is opened, the ONU may attempt to register.

In general, the ONUs attempt to register using the highest upstream transmission rate supported by both the OLT and the ONU. If the OLT advertised itself as 10G-capable, but in the current DISCOVERY MPCPDU it has not enabled the 10 Gb/s discovery window, the 10G-capable ONU skips such discovery attempts and waits for a future discovery window in which 10 Gb/s transmission is enabled.

Table 200A-4 shows the action the ONU shall take based on the ONU transmit capabilities and the received discovery information.

Table 200A-4—ONU action during discovery window

<i>DiscoveryInfo</i> field				ONU upstream capability		ONU action
Upstream capability		Discovery window		10G	2.5G	
10G	2.5G	10G	2.5G			
1	0	1	0	1	0/1	Attempt 10G registration
1	0/1	1	0/1	1	0	Attempt 10G registration
0/1	1	0/1	1	0/1	1	Attempt 2.5G registration
1	1	0	1	1	0	Wait for 10G discovery window
1	1	1	0	0/1	1	Wait for 2.5G discovery window

The ONU transmits the REGISTER_REQ MPCPDU in envelopes with the discovery PLID (DISC_PLID, see 144.3.5).

200A.3.4 Protocol implementation conformance statement (PICS) proforma for subclause 200A.3, Super-PON Multipoint MAC Control Sublayer

The supplier of a protocol implementation that is claimed to conform to subclause 200A.3, Super-PON Multipoint MAC Control Sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

200A.3.4.2 Identification

200A.3.4.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

200A.3.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cs-202x, Subclause 200A.3, Super-PON Multipoint MAC Control Sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No <input type="checkbox"/> Yes <input type="checkbox"/> (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3cs-202x.)	
Date of Statement	

200A.3.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	144.1	Device supports functionality required for OLT	O/1	Yes <input type="checkbox"/> No <input type="checkbox"/>
*ONU	ONU functionality	144.1	Device supports functionality required for ONU	O/1	Yes <input type="checkbox"/> No <input type="checkbox"/>

200A.3.4.4 PICS proforma tables for Multipoint MAC Control**200A.3.4.4.1 Clock tracking**

Item	Feature	Subclause	Value/Comment	Status	Support
CLK1	Clock tracking at OLT	200A.3.2.1.2	<i>LocalTime</i> tracks the XGMII transmit clock	OLT:M	Yes [] N/A []
CLK2	Clock tracking at ONU	200A.3.2.1.2	<i>LocalTime</i> tracks the XGMII receive clock	ONU:M	Yes [] N/A []

200A.3.4.4.2 LLID

Item	Feature	Subclause	Value/Comment	Status	Support
LL1a	Reserved LLID values, transmit	144.3.5	Do not transmit envelopes with ESC_LLID or a reserved value in the LLID field	M	Yes []
LL1b	Reserved LLID values, receive	144.3.5	Ignore envelopes with ESC_LLID or a reserved value in the LLID field	M	Yes []
LL2a	Unregistered ONU, accept envelopes	144.3.5	Accept only the envelopes containing the DISC_PLID value in the LLID field	ONU:M	Yes [] N/A []
LL2b	Unregistered ONU, ignore envelopes	144.3.5	Ignore envelopes containing values other than DISC_PLID in the LLID field	ONU:M	Yes [] N/A []
LL3a	Registered ONU, accept envelopes	144.3.5	Accept envelopes containing the following values in the LLID field: <ul style="list-style-type: none"> — The specific PLID value assigned to this ONU during registration — The specific MLID value assigned to this ONU during registration — Broadcast PLID (BCAST_PLID) — Broadcast MLID (BCAST_MLID) — Any ULID or GLID assigned to this ONU by management 	ONU:M	Yes [] N/A []
LL3b	Registered ONU, ignore envelopes	144.3.5	Ignore envelopes containing the DISC_PLID value in the LLID field	ONU:M	Yes [] N/A []

200A.3.4.4.3 Protocol-independent state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Control Parser	144.2.1.5	Meets the requirements of Figure 144–5	M	Yes []
SM2	Control Multiplexer	144.2.1.6	Meets the requirements of Figure 144–6	M	Yes []

200A.3.4.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	GATE structure	144.3.6.1	As in Figure 144–12	M	Yes []
MP1a	Grant start time and size	144.3.6.1	Transmission on each channel starts at the ONU's local time equal to the <i>StartTime</i> value and has the length as necessary to transmit all allocated envelopes (the sum of all <i>EnvLength</i> fields) together with the associated optical and FEC overhead	ONU:M	Yes [] N/A []
MP1b	Fragmentation	144.3.6.1	When flag <i>F</i> is set to 0, do not fragment new frames	ONU:M	Yes [] N/A []
MP1c	Forced report	144.3.6.1	When flag <i>FR</i> is set to 1, report the total length of the frames (including IPG and preamble), queued for transmission on this specific LLID	ONU:M	Yes [] N/A []
MP1d	MPCPDU fragmentation	144.3.6.1	ONU does not fragment MPCPDU frames, regardless of the value of the <i>Fragmentation</i> flag in the <i>EnvAlloc</i> structure that allocates a PLID envelope	ONU:M	Yes [] N/A []
MP2	REPORT structure	144.3.6.2	As in Figure 144–13	M	Yes []
MP3	REGISTER_REQ structure	144.3.6.3	As in Figure 144–14	M	Yes []
MP4	REGISTER structure	144.3.6.4	As in Figure 144–15	M	Yes []
MP5	REGISTER_ACK structure	144.3.6.5	As in Figure 144–16	M	Yes []
MP6	DISCOVERY structure	144.3.6.6	As in Figure 144–17	M	Yes []
MP6a	Discovery attempt	144.3.6.6	Attempt to register on a single channel only	ONU:M	Yes [] N/A []
MP6b	<i>OnuRssiMin</i> trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is greater or equal to <i>OnuRssiMin</i>	ONU:M	Yes [] N/A []
MP6c	<i>OnuRssiMax</i> trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is smaller than or equal to <i>OnuRssiMax</i>	ONU:M	Yes [] N/A []
MP6d	Discovery attempt at 10 Gb/s	200A.3.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if the bit 5 was set to 0	ONU:M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
MP6e	Discovery attempt at 2.5 Gb/s	200A.3.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 2.5 Gb/s upstream channel if the OLT did not open the 2.5 Gb/s discovery window, i.e., if the bit 7 was set to 0	ONU:M	Yes [] N/A []
MP7	SYNC_PATTERN structure	144.3.6.7	As in Figure 144–18	M	Yes []
MP8	MPCPDU timing on transmit	144.3.1.1	When multiple MPCPDUs are transmitted within a single envelope, all these MPCPDUs have the same <i>Timestamp</i> field value, referencing the transmission time of the ESH.	M	Yes []
MP9a	Discovery Initiation in OLT	144.3.7.6	Meets the requirements of Figure 144–20, single instance associated with DISC_PLID	OLT:M	Yes [] N/A []
MP9b	Discovery Completion in OLT	144.3.7.7	Meets the requirements of Figure 144–21, one instance for each unicast PLID being registered	OLT:M	Yes [] N/A []
MP9c	Discovery in ONU	144.3.7.8	Meets the requirements of Figure 144–22, single instance	ONU:M	Yes [] N/A []
MP10a	GATE Generation	144.3.8.7	Meets the requirements of Figure 144–23, one instance for each registered unicast PLID	OLT:M	Yes [] N/A []
MP10b	GATE Reception	144.3.8.8	Meets the requirements of Figure 144–24, single instance	ONU:M	Yes [] N/A []
MP11a	Envelope Commitment in OLT	144.3.8.9	Meets the requirements of Figure 144–25, single instance	OLT:M	Yes [] N/A []
MP11b	Envelope Commitment in ONU	144.3.8.10	Meets the requirements of Figure 144–26, single instance	ONU:M	Yes [] N/A []
MP11c	Envelope Activation	144.3.8.11	Meets the requirements of Figure 144–27, single instance	M	Yes []
MP12	ONU multi-rate discovery	200A.3.3.9.2	ONU takes action based on on the ONU transmit capabilities and the received discovery information, as shown in Table 200A-4	ONU:M	Yes [] N/A []
MP13	MPCP delay variability	200A.3.3.3	Maintain the combined delay variation through the MAC and PHY of less than three EQT for channels operating at 2.578125 GBd and less than two EQTs for channels operating at 10.3125 GBd	M	Yes []
MP14a	Granting overlapping envelopes to the PLID	144.3.1.2	OLT does not allocate overlapping envelopes to the PLID, except the fully overlapping envelopes (see Figure 143–5)	OLT:M	Yes [] N/A []
MP14b	Processing partially overlapping PLID envelope allocations	144.3.1.2	If ONU receives partially overlapping PLID envelope allocations, it chooses only one of these envelopes for MPCPDU transmission, and only if the envelope length is enough for at least one complete MPCPDU	ONU:M	Yes [] N/A []