45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change rows for 1.1003 through 1.1099 in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.1000 through 1.1002	Nx25G-EPON PMA/PMD extended ability	45.2.1.134a
1.1003	Super-PON PMA/PMD extended ability	45.2.1.134b
~~1.1003~~1.1004 through 1.1099	Reserved	
…		

Update subclause 45.2.1.23a as follows:

45.2.1.23a PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–26a.

45.2.1.23a.1 Downstream differential encoding (1.29.15)

Downstream differential encoding is selected using bit 1.29.15. This bit is read/write in the OLT and read only in the ONU with the default value of 0 (indicating that downstream differential encoding is not enabled).

In the OLT, this bit controls whether downstream differential encoding is selected for the transmit PMA output.

In the ONU, this bit indicates whether the downstream differential decoding is enabled in the ONU receive PMA.

45.2.1.23.a.2 Super-PON PMA/PMD transmit channel

The Super-PON PMA/PMD operating transmit channel (see 200.2.2) is selected using bits 9 to 6. The channel interval supported by the PMA/PMD is advertised in the Super-PON PMA/PMD extended ability register (register 1.1003, see 45.2.1.134b).

45.2.1.23a.~~2~~3 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD for Nx25G-EPON are advertised in the Nx25G-EPON PMA/PMD extended ability registers (Registers 1.1000 through 1.1002, see 45.2.1.134a). The PMA/PMD type abilities of the PMA/PMD for Super-PON are advertised in the Super-PON PMA/PMD extended ability register (register 1.1003, see 45.2.1.134b). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

Table 45–26a—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.29.15	Downstream differential encoding	1 = Downstream differential encoding enabled 0 = Downstream differential encoding disabled	R/W in OLT RO in ONU
1.29.14:~~6~~10	Reserved	Value always 0	RO
1.29.9:6	Super-PON PMA/PMD transmit channel	Super-PON PMA/PMD operating transmit channel	R/W
1.29.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = Reserved ~~1 0 1 x x x = Reserved~~ 1 0 1 1 x x = Reserved 1 0 1 0 1 1 = 10GBASE-SP1-D 1 0 1 0 1 0 = 10GBASE-SP1-U 1 0 1 0 0 1 = 10/2.5GBASE-SP1-D 1 0 1 0 0 0 = 10/2.5GBASE-SP1-U 1 0 0 1 1 1 = 50GBASE-PQX-U3 1 0 0 1 1 0 = 50GBASE-PQX-U2 1 0 0 1 0 1 = 50GBASE-PQX-D3 1 0 0 1 0 0 = 50GBASE-PQX-D2 1 0 0 0 1 1 = 50GBASE-PQG-U3 1 0 0 0 1 0 = 50GBASE-PQG-U2 1 0 0 0 0 1 = 50GBASE-PQG-D3 1 0 0 0 0 0 = 50GBASE-PQG-D2 0 1 1 1 1 1 = 50/25GBASE-PQX-U3 0 1 1 1 1 0 = 50/25GBASE-PQX-U2 0 1 1 1 0 1 = 50/25GBASE-PQX-D3 0 1 1 1 0 0 = 50/25GBASE-PQX-D2 0 1 1 0 1 1 = 50/25GBASE-PQG-U3 0 1 1 0 1 0 = 50/25GBASE-PQG-U2 0 1 1 0 0 1 = 50/25GBASE-PQG-D3 0 1 1 0 0 0 = 50/25GBASE-PQG-D2 0 1 0 1 1 1 = 50/10GBASE-PQX-U3 0 1 0 1 1 0 = 50/10GBASE-PQX-U2 0 1 0 1 0 1 = 50/10GBASE-PQX-D3 0 1 0 1 0 0 = 50/10GBASE-PQX-D2 0 1 0 0 1 1 = 50/10GBASE-PQG-U3 0 1 0 0 1 0 = 50/10GBASE-PQG-U2 0 1 0 0 0 1 = 50/10GBASE-PQG-D3 0 1 0 0 0 0 = 50/10GBASE-PQG-D2 0 0 1 1 1 1 = 25GBASE-PQX-U3 0 0 1 1 1 0 = 25GBASE-PQX-U2 0 0 1 1 0 1 = 25GBASE-PQX-D3 0 0 1 1 0 0 = 25GBASE-PQX-D2 0 0 1 0 1 1 = 25GBASE-PQG-U3 0 0 1 0 1 0 = 25GBASE-PQG-U2 0 0 1 0 0 1 = 25GBASE-PQG-D3 0 0 1 0 0 0 = 25GBASE-PQG-D2 0 0 0 1 1 1 = 25/10GBASE-PQX-U3 0 0 0 1 1 0 = 25/10GBASE-PQX-U2 0 0 0 1 0 1 = 25/10GBASE-PQX-D3 0 0 0 1 0 0 = 25/10GBASE-PQX-D2 0 0 0 0 1 1 = 25/10GBASE-PQG-U3 0 0 0 0 1 0 = 25/10GBASE-PQG-U2 0 0 0 0 0 1 = 25/10GBASE-PQG-D3 0 0 0 0 0 0 = 25/10GBASE-PQG-D2	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.134b after 45.2.1.134a as follows:

45.2.1.134b Super-PON PMA/PMD extended ability register (Register 1.1003)

The assignment of bits in the Super-PON PMA/PMD extended ability register is shown in Table 45–103b.

Table 45–103b—Super-PON PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1003.15	10GBASE-SP1-D	1 = PMA/PMD is able to perform 10GBASE-SP1-Dxy 0 = PMA/PMD is not able to perform 10GBASE-SP1-Dxy	RO
1.1003.14	10GBASE-SP1-U	1 = PMA/PMD is able to perform 10GBASE-SP1-Uxy 0 = PMA/PMD is not able to perform 10GBASE-SP1-Uxy	RO
1.1003.13	10/2.5GBASE-SP1-D	1 = PMA/PMD is able to perform 10/2.5GBASE-SP1-Dxy 0 = PMA/PMD is not able to perform 10/2.5GBASE-SP1-Dxy	RO
1.1003.12	10/2.5GBASE-SP1-U	1 = PMA/PMD is able to perform 10G/2.5BASE-SP1-Uxy 0 = PMA/PMD is not able to perform 10/2.5GBASE-SP1-Uxy	RO
1.1003.11:8	Reserved	Value always 0	RO
1.1003.7:4	Super-PON channel y	PMA/PMD last transmit channel supported	RO
1.1003.3:0	Super-PON channel x	PMA/PMD first transmit channel supported	RO

[a]RO = Read only

45.2.1.134b.1 10GBASE-SP1-D (1.1003.15)

When read as a one, bit 1.1003.15 indicates that the PMA/PMD is able to support a 10GBASE-SP1-Dxy PMA/PMD type, able to operate on any of the Super-PON FSR Set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.15 indicates that the PMA/PMD is not able to support a 10GBASE-SP1-Dxy PMA/PMD type.

45.2.1.134b.2 10GBASE-SP1-U (1.1003.14)

When read as a one, bit 1.1003.14 indicates that the PMA/PMD is able to support a 10GBASE-SP1-Uxy PMA/PMD type, able to operate on any of the Super-PON FSR Set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.14 indicates that the PMA/PMD is not able to support a 10GBASE-SP1-Uxy PMA/PMD type.

45.2.1.134b.3 10/2.5GBASE-SP1-D (1.1003.13)

When read as a one, bit 1.1003.13 indicates that the PMA/PMD is able to support a 10/2.5GBASE-SP1-Dxy PMA/PMD type, able to operate on any of the Super-PON FSR Set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.13 indicates that the PMA/PMD is not able to support a 10/2.5GBASE-SP1-Dxy PMA/PMD type.

45.2.1.134b.4 10/2.5GBASE-SP1-U (1.1003.12)

When read as a one, bit 1.1003.12 indicates that the PMA/PMD is able to support a 10/2.5GBASE-SP1-Uxy PMA/PMD type, able to operate on any of the Super-PON FSR Set 1 channels x (1.1003.3:0) to y (1.1003.7:4). When read as a zero, bit 1.1003.12 indicates that the PMA/PMD is not able to support a 10/2.5GBASE-SP1-Uxy PMA/PMD type.

45.2.1.134b.5 Super-PON channel y (1.1003.7:4)

This 4-bit field indicates the highest numbered Super-PON transmit channel supported by the PMA/PMD (see 200.2.2).

45.2.1.134b.6 Super-PON channel x (1.1003.3:0)

This 4-bit field indicates the lowest numbered Super-PON transmit channel supported by the PMA/PMD (see 200.2.2).

45.2.3 PCS registers

Change the rows for registers 3.76 through 3.199 in Table 45–176 (as modified by IEEE Std 802.3ca-2020) as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.76, 3.77	10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON corrected FEC codewords counter	45.2.3.41
3.78, 3.79	10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON uncorrected FEC codewords counter	45.2.3.42
3.80	10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor interval control	45.2.3.43
3.81	10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor status	45.2.3.44
3.82	10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor threshold control	45.2.3.45
3.83 through 3.134	Nx25G-EPON and Super-PON synchronization pattern	45.2.3.45a
3.135 through 3.199	Reserved	
…		

45.2.3.1 PCS control 1 register (Register 3.0)

Change the row for bits 3.0.5:2 in Table 45–177 (as modified by IEEE Std 802.cd-2018 and IEEE Std 802.3ca-2020) as follows (unchanged rows not shown):

Table 45–177— PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.0.5:2	Speed selection	5 4 3 2 ~~1 1 x x = Reserved~~ 1 1 1 x = Reserved 1 1 0 1 = Reserved 1 1 0 0 = 10/2.5 Gb/s 1 0 1 1 = 25/10 Gb/s 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–180 (as modified by IEEE Std 802.3cb-2018, IEEE Std 802.cd-2018, and IEEE Std 802.3ca-2020) as follows (unchanged rows not shown):

Table 45–180— PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:5	Reserved	Value always 0	RO
3.7.4:0	PCS type selection	4 3 2 1 0 1 1 x x x = reserved ~~1 0 1 x x = reserved~~ 1 0 1 1 x = reserved 1 0 1 0 1 = Select 10GBASE-SP PCS type 1 0 1 0 0 = Select 10/2.5GBASE-SP PCS type 1 0 0 1 1 = Select 25GBASE-PQ PCS type 1 0 0 1 0 = Select 25/10GBASE-PQ PCS type 1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only 1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only 0 1 1 1 1 = Select 5GBASE-R PCS type 0 1 1 1 0 = Select 2.5GBASE-X PCS type 0 1 1 0 1 = Select 400GBASE-R PCS type 0 1 1 0 0 = Select 200GBASE-R PCS type 0 1 0 1 1 = Select 5GBASE-T PCS type 0 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 0 1 = Select 25GBASE-T PCS type 0 1 0 0 0 = Select 50GBASE-R PCS type 0 0 1 1 1 = Select 25GBASE-R PCS type 0 0 1 1 0 = Select 40GBASE-T PCS type 0 0 1 0 1 = Select 100GBASE-R PCS type 0 0 1 0 0 = Select 40GBASE-R PCS type 0 0 0 1 1 = Select 10GBASE-T PCS type 0 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

Change the title and text of 45.2.3.6.1 as follows:

45.2.3.6.1 PCS type selection (3.7.4:0)

The PCS type shall be selected using bits 4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.13:12, 3.8.9:0 and 3.9.~~7~~9:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register or the PCS status 3 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.8 PCS status 3 register (Register 3.9)

Change the row for bits 3.9.15:4 in Table 45–182 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.3ca-2020) as follows (unchanged rows not shown):

Table 45–182— PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.9.15:~~8~~10	Reserved	Value always 0	RO
3.9.9	10GBASE-SP capable	1 = PCS is able to support 10GBASE-SP PCS type 0 = PCS is not able to support 10GBASE-SP PCS type	RO
3.9.8	10/2.5GBASE-SP capable	1 = PCS is able to support 10/2.5GBASE-SP PCS type 0 = PCS is not able to support 10/2.5GBASE-SP PCS type	RO
3.9.7	25GBASE-PQ capable	1 = PCS is able to support 25GBASE-PQ PCS type 0 = PCS is not able to support 25GBASE-PQ PCS type	RO
3.9.6	25/10GBASE-PQ capable	1 = PCS is able to support25/10GBASE-PQ PCS type 0 = PCS is not able to support 25/10GBASE-PQ PCS type	RO
3.9.5	25GBASE-PQ Rx only capable	1 = PCS is able to support 25GBASE-PQ Rx only PCS type 0 = PCS is not able to support 25GBASE-PQ Rx only PCS type	RO
3.9.4	25GBASE-PQ Tx only capable	1 = PCS is able to support 25GBASE-PQ Tx only PCS type 0 = PCS is not able to support 25GBASE-PQ Tx only PCS type	RO
…			

[a]RO = Read only

Insert 45.2.3.8.ba through 45.2.3.8.bb (before 45.2.3.8.aa as inserted by IEEE Std 802.3ca-2020) as follows:

45.2.3.8.ba 10GBASE-SP capable (3.9.9)

When read as a one, bit 3.9.9 indicates that the PCS is able to support the 10GBASE-SP PCS type. When read as a zero, bit 3.9.9 indicates that the PCS is not able to support the 10GBASE-SP PCS type.

45.2.3.8.bb 10/2.5GBASE-SP capable (3.9.8)

When read as a one, bit 3.9.8 indicates that the PCS is able to support the 25/10GBASE-SP PCS type. When read as a zero, bit 3.9.8 indicates that the PCS is not able to support the 25/10GBASE-SP PCS type.

Change the title, text and tables for 45.2.3.41 through 45.2.3.45 (as modified by IEEE Std 802.3ca-2020) as follows:

45.2.3.41 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON corrected FEC codewords counter register is shown in Table 45–213. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON and Super-PON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–213— 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected FEC codewords lower	corrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected FEC codewords upper	corrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.42 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON uncorrected FEC codewords counter register is shown in Table 45–214. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25- EPON and Super-PON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–214— 10G-EPON, ~~and~~ Nx25G-EPON, and Super-PON uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected FEC codewords upper	uncorrected_FEC_codewords_counter[3~~2~~1:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.43 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor interval control register (Register 3.80)

The assignment of bits in the 10GBASE-PR and, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor interval control register is shown in Table 45–215. This register is defined only when 10GBASE-PR, or 10/1GBASE-PRX, ~~or~~ Nx25G-EPON, or Super-PON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON and Super-PON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–215— 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor interval control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:8	Reserved	Value always 0	RO
3.80.7:0	EPON BER monitor interval	For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 microseconds) of the timer used by the BER monitor function. Default value is 25 (i.e., 125 microseconds). A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON and Super-PON: QC-LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER Monitor function. Default value is 12 (i.e., 192 codewords).	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.44 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor status (Register 3.81)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor status register is shown in Table 45–216. This register is defined only when 10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G-EPON, or Super-PON ONU capability is supported.

Table 45–216— 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:2	Reserved	Value always 0	RO
3.81.1	Latched high BER	10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G-EPON, or Super-PON PCS: 1 = reported a high BER. 0 = did not report a high BER.	RO, LH
3.81.0	high BER	10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G-EPON, or Super-PON PCS: 1 = reporting a high BER. 0 = not reporting a high BER.	RO

[a]RO = Read only, LH = Latching high

45.2.3.41.1 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON PCS high BER (3.81.0)

In the 10GBASE-PR,10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and, 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G-EPON and Super-PON.

45.2.3.44.2 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON PCS latched high BER (3.81.1)

In the 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON high BER status bit (3.81.0).

45.2.3.45 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor threshold control (Register 3.82)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor threshold control register is shown in Table 45–217. This register is defined only when 10GBASE-PR, 10/1GBASE-PRX, ~~or~~ Nx25G-EPON, or Super-PON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON and Super-PON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–217— 10GBASE-PR, 10/1GBASE-PRX, ~~and~~ Nx25G-EPON, and Super-PON BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	EPON BER monitor threshold	For 10G-EPON: number of sync header errors within a timer interval that triggers a high BER condition for the BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON and Super-PON: number of invalid QC-LDPC codeword parity checks within a BER monitor interval that triggers a high BER condition for the BER Monitor function. Default value is 18. A value of zero indicates that the BER Monitor function is disabled.	R/W

[a]R/W = Read/Write

Change the title and text for 45.2.3.45a as follows:

45.2.3.45a Nx25G-EPON and Super-PON synchronization pattern registers (Registers 3.83 through 3.134)

The assignment of bits in registers 3.83 through 3.134 is shown in Table 45–217a. The Nx25G-EPON synchronization pattern (see 142.1.3 and 144.3.6.7) is used in the upstream data transmissions to facilitate the OLT in locking to the incoming data burst.

45.2.3.45a.1 SP3 bit 257 (3.83.5)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.5 indicates the value to be used for the 257th bit of SP3. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.2 SP3 balanced (3.83.4)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.4 indicates that repeating SP3 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP3 is to remain unbalanced, i.e., SP3 is always transmitted using the values from 3.83.5 and 3.118.0 through 3.133.15. When this bit is set to a one SP3 is to be balanced, i.e., each 257-bit block of SP3 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.3 SP2 bit 257 (3.83.3)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.3 indicates the value to be used for the 257th bit of SP2. See 142.1.3 and144.3.6.7 for additional details.

45.2.3.45a.4 SP2 balanced (3.83.2)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.2 indicates that repeating SP2 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP2 is to remain unbalanced, i.e., SP2 is always transmitted using the values from 3.83.3 and 3.101.0 through 3.116.15. When this bit is set to a one SP2 is to be balanced, i.e., each 257-bit block of SP2 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.5 SP1 bit 257 (3.83.1)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.1 indicates the value to be used for the 257th bit of SP1. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.6 SP1 balanced (3.83.0)

In the Nx25G-EPON and Super-PON PCS, bit 3.83.0 indicates that repeating SP1 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP1 is to remain unbalanced, i.e., SP1 is always transmitted using the values from 3.83.1 and 3.84.0 through 3.99.15. When this bit is set to a one SP1 is to be balanced, i.e., each 257-bit block of SP1 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.7 SP1 pattern (3.84.0 through 3.99.15)

In the Nx25G-EPON and Super-PON PCS, bits 3.84.0 through 3.99.15 indicate the value to be used for the lower 256 bits of the initial SP1 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP1 are determined by bit 3.83.0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.8 SP1 length (3.100.15:0)

In the Nx25G-EPON and Super-PON PCS, bits 3.100.15:0 indicate the number of times the 257-bit SP1 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.9 SP2 pattern (3.101.0 through 3.116.15)

In the Nx25G-EPON and Super-PON PCS, bits 3.101.0 through 3.116.15 indicate the value to be used for the lower 256 bits of the initial SP2 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP2 are determined by bit 3.100.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.10 SP2 length (3.117.15:0)

In the Nx25G-EPON and Super-PON PCS, bits 3.117.15:0 indicate the number of times the 257-bit SP2 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.11 SP3 pattern (3.118.0 through 3.133.15)

In the Nx25G-EPON and Super-PON PCS, bits 3.118.0 through 3.133.15 indicate the value to be used for the lower 256 bits of the initial SP3 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP3 are determined by bit 3.117.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.12 SP3 length (3.134.15:0)

In the Nx25G-EPON and Super-PON PCS, bits 3.134.15:0 indicate the number of times the 257-bit SP3 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details