Jitter corner in 100GBASE-ZR

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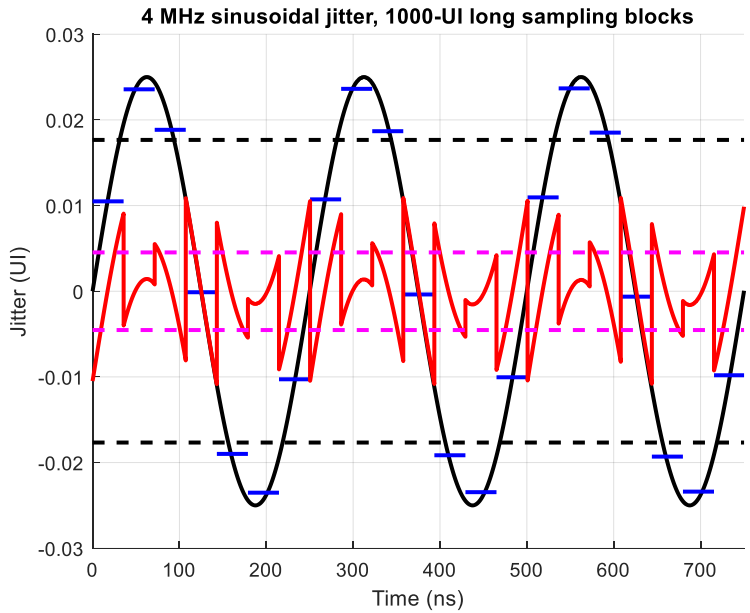
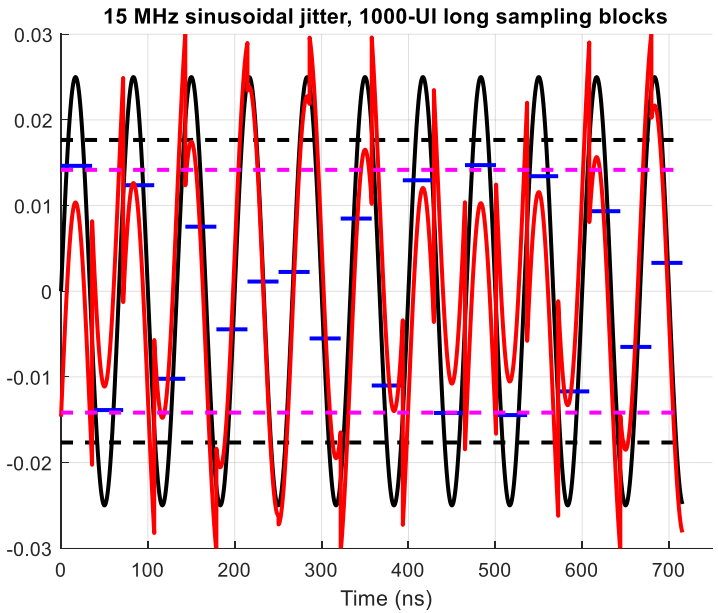
Problem statement

- Draft spec 100GBASE-ZR does not have the usual clock recovery unit in measurement or sinusoidal jitter component in stressed receiver sensitivity definition
  - D3.0 comment 85 and D3.1 comments 69 and 79, comments to D3.2
- So, what does it have?

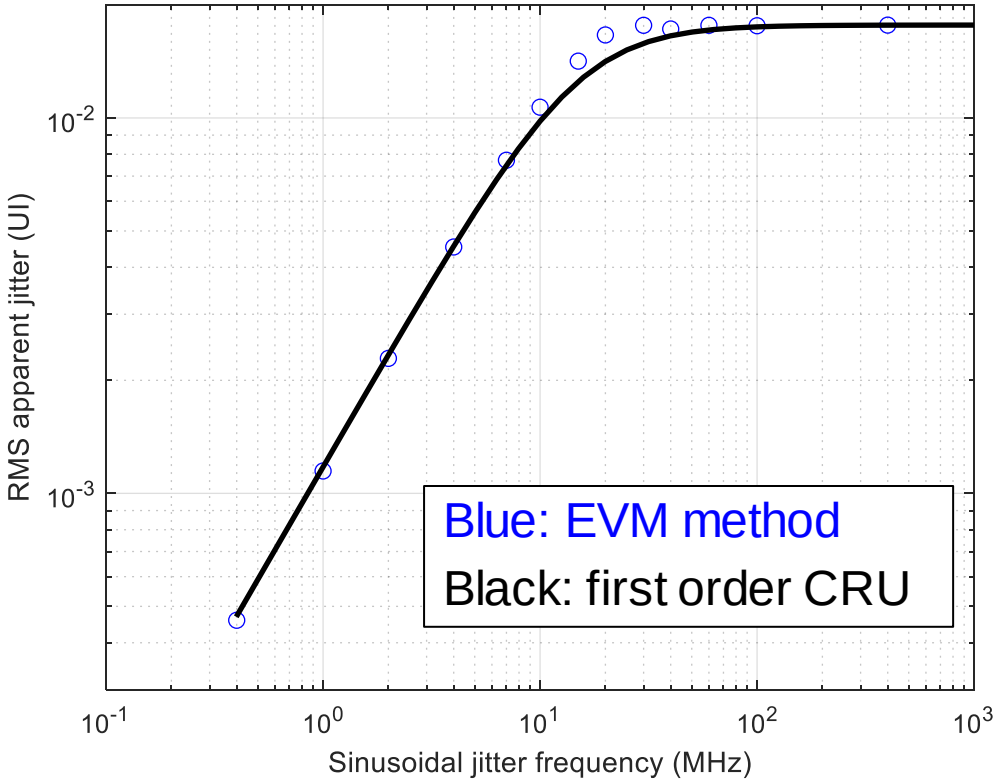
For EVM, a signal is measured in 1000-UI blocks





- In each block, the average phase of the data (blue bars) is removed, so the apparent jitter is the red line
- Dashed lines show +/- 1 standard deviation

Apparent SJ after EVM sampling



- Effective jitter corner of the default EVM method is 15.2 MHz
  - based on the LF roll-off, which is first order (20 dB/decade). The -3 dB point is 12.8 GHz
- Either way, it's far too high for a DSP receiver, and transmitters can do better

Choosing a better corner frequency

- Changing the block size for symbol phase correction changes the effective jitter corner in inverse proportion
- The 802.3 family of 100 Gb/s PAM4 optical transmitters are specified with a clock recovery unit (CRU) with a corner frequency of 4 MHz (Jpkpk*fJitter=3.76e-6 s.Hz) and a slope of 20 dB/decade. The corner should be set lower than 4 MHz for this DSP-heavy PHY
- The same Jpkpk*fJitter for the 100GBASE-ZR signalling rate of 27.9525 gives 2.1 MHz
- If we choose 2.17 MHz, a block size for symbol phase correction of 7000 UI can be used to give the effect of the CRU. 7000 is an integral multiple of the 1000 UI block size used for optical phase correction

For balance, we should make the related change to the receiver spec

- Should include the usual sinusoidal jitter to a normative receiver spec
  - e.g. the equivalent of stressed receiver sensitivity (here, 154.9.15 Receiver OSNR)
  - with the same jitter corner frequency
  - In the proposed remedy, this is rounded to 2.2 MHz
  - 0.05 UI of SJ is small as compared with the noise that takes the BER to the spec 4.62e-3, so not proposing changing the OSNR numbers for this, though that could be done

Conclusion

1. Include the effect of a CRU in the definition EVM for 100GBASE-ZR
   - 2.2 MHz seems a suitable choice
   - This may be implemented by a block size of 7000 UI for symbol phase correction only

2. Consider including the usual SJ in 154.9.15 Receiver OSNR, with the same jitter corner frequency