			DTE								Repeater				MAU										
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	MultiGBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Energy-Efficient Ethernet (optional)	Auto-Negotiation Package (mandatory)
oMAU managed object class (30.5.1)																									
aFalseCarriers	ATTRIBUTE	GET																			X				
aBIPErrorCount	ATTRIBUTE	GET																			X				
aLaneMapping	ATTRIBUTE	GET																			X				
aRSFECBIPErrorCount	ATTRIBUTE	GET																			X				
aRSFECLaneMapping	ATTRIBUTE	GET																			X				
aSCFECLaneMapping	ATTRIBUTE	GET																			X				
aIdleErrorCount	ATTRIBUTE	GET																			X				

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

This subclause formally defines the behaviours for the oMAU managed object class, attributes, actions, and notifications.

The sublayer that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayers as a group. Therefore in this clause, the term MAU will include PMA and PMD sublayers, as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

30.5.1.1 MAU attributes

30.5.1.1.15 aFECAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown initializing, true state not yet known

supported	FEC supported
not supported	FEC not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction at the MDI (see 65.2, Clause 74, Clause 91, and Clause 108).

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC capability register (see 45.2.10.2 or 45.2.1.101).;

Option 1:

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
BASE-R enabled	BASE-R FEC enabled
RS-FEC enabled	RS-FEC enabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value for a PHY that supports an optional FEC sublayer that indicates the mode of operation of the FEC sublayer for forward error correction in use at the MDI (see 65.2, Clause 74, Clause 91, and Clause 108).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. The enumerations “BASE-R enabled” and “RS-FEC enabled” are only used for 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs where operation in the no-FEC mode maps to the enumerations “disabled”, operation in the BASE-R FEC mode maps to the enumerations “BASE-R enabled”, and operation in the RS-FEC mode maps to the enumerations “RS-FEC enabled” (see 110.6 and 111.6).

When Clause 73 Auto-Negotiation is enabled for a 25GBASE-R PHY, a SET operation is not allowed and a GET operation maps to the variables FEC_enable in Clause 74 and FEC_enable in Clause 108. When Clause 73 Auto-Negotiation is enabled for a non-25GBASE-R PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable in Clause 74.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC control register (see 45.2.10.3) for 1000BASE-PX, to the BASE-R FEC control register (see 45.2.1.102) and the 25G RS-FEC Enable bit in the RS-FEC control register (see 45.2.1.110) for 25GBASE-R, or FEC enable bit in BASE-R FEC control register (see 45.2.1.102).;

Option 2:

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
BASE-R enabled	BASE-R FEC enabled
RS-FEC enabled	RS-FEC enabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the FEC sublayer for forward error correction in use at the MDI (see 65.2, Clause 74, Clause 91, ~~and~~ Clause 108, and Clause 153).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. A SET operation has no effect on the mode of operation of the PHY if FEC is mandatory for the PHY.

The enumerations “BASE-R enabled” and “RS-FEC enabled” are only used for 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs where operation in the no-FEC mode maps to the enumerations “disabled”, operation in the BASE-R FEC mode maps to the enumerations “BASE-R enabled”, and operation in the RS-FEC mode maps to the enumerations “RS-FEC enabled” (see 110.6 and 111.6).

When Clause 73 Auto-Negotiation is enabled for a 25GBASE-R PHY, a SET operation is not allowed and a GET operation maps to the variables FEC_enable in Clause 74 and FEC_enable in Clause 108. When Clause 73 Auto-Negotiation is enabled for a non-25GBASE-R PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable in Clause 74.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC control register (see 45.2.10.3) for 1000BASE-PX, to the BASE-R FEC control register (see 45.2.1.102) and the 25G RS-FEC Enable bit in the RS-FEC control register (see 45.2.1.110) for 25GBASE-R, or FEC enable bit in BASE-R FEC control register (see 45.2.1.102).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/50/40/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs that support FEC at the MDI, an array of corrected FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the

FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for all lanes. Each element of this array contains a count of corrected FEC blocks for that FEC sublayer instance.

Increment the counter by one for each ~~received~~ FEC block received at the MDI that is corrected by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.10.5 and 45.2.1.103 for 10GBASE-R, 45.2.3.41 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.125 for BASE-R, 45.2.1.112 for RS-FEC, ~~and~~ 45.2.3.61 for PCS FEC, and 45.2.1.186al for SC-FEC).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs that support FEC at the MDI, an array of uncorrectable FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for all lanes. Each element of this array contains a count of uncorrectable FEC blocks for that FEC sublayer instance.

Increment the counter by one for each FEC block received at the MDI that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC uncorrectable blocks counter(s) (see 45.2.10.6 and 45.2.1.104 for 10GBASE-R, 45.2.3.42 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.133 for BASE-R, 45.2.1.113 for RS-FEC, ~~and~~ 45.2.3.62 for PCS FEC, and 45.2.1.186am for SC-FEC).;

30.5.1.1.26 aRSFECBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R and 100GBASE-P PHYs that support RS-FEC at the MDI, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane.

Increment the counter by one for each BIP error at the MDI detected during alignment marker removal in the PCS for the corresponding lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the BIP error counters (see 45.2.1.117 and 45.2.1.118).;

30.5.1.1.27 aRSFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For 50GBASE-R, 100GBASE-R and 100GBASE-P PHYs that support RS-FEC at the MDI, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane at the MDI that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.119 and 45.2.1.120).;

45.2.1.117 and 45.2.1.118).;

30.5.1.1.27a aSCFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For a 100GBASE-R PHYs that support SC-FEC at the MDI, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane at the MDI that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.186aj and 45.2.1.186ak).;

30.5.1.1.28 aRSFECBypassAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC bypass ability supported
not supported	FEC bypass ability not supported

BEHAVIOUR DEFINED AS:
A read-only value that indicates if ~~the~~ a PHY that support RS-FEC at the MDI supports ~~an~~ the optional RS-FEC bypass ability.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.111).;

30.5.1.1.29 aRSFECBypassIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC error indication bypass ability supported
not supported	FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if ~~the~~ a PHY that support RS-FEC at the MDI supports ~~an~~ the optional RS-FEC error indication bypass ability (see 91.5.3.3).
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.111).;

30.5.1.1.30 aRSFECBypassEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC bypass disabled
enabled	FEC bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC bypass function (see 91.5.3.3).
A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.110).;

30.5.1.1.31 aRSFECBypassIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC error indication bypass disabled
enabled	FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function.
A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.110).;

30.5.1.1.32 aPCSFECBypassIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	PCS FEC error indication bypass ability supported
not supported	PCS FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if ~~the~~ a PHY that support RS-FEC at the MDI supports ~~an~~ the optional PCS FEC error indication bypass ability (see 119.2.5.3).
If a Clause 45 MDIO Interface is present, then this attribute maps to the PCS FEC status register (see 45.2.3.60).;

30.5.1.1.33 aPCSFECBypassIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	PCS FEC error indication bypass disabled
enabled	PCS FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the PCS FEC error indication bypass function (see 119.2.5.3).
A GET operation returns the current mode of operation of the PCS FEC. A SET operation changes the mode of operation of the PCS FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the PCS FEC control register (see 45.2.3.59).;