SC-FEC sublayer lane alignment process comments and remedies

In support of comments against IEEE 802.3ct D1.2

Comment #: 6, 11, 15, 17, 18, 19, 20 , 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 34, 35, 36

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References

- 100GBASE ZR Draft 802.3ct_D1p1.pdf, Private Area
- ITU-T G.709 - Interfaces for the optical transport network
- ITU-T G.798 - Characteristics of optical transport network hierarchy equipment functional blocks
- trowbridge_3cn_01a_0119.pdf, IEEE P802.3cn Task Force, Long Beach, March 2019
- bruckman_3ct_01a_200213, IEEE P802.3ct Task Force, teleconference February 13th, 2020
- bruckman_3ct_02a_200213, IEEE P802.3ct Task Force, teleconference February 13th, 2020

General

- During the February 13th, 2020 Teleconference I presented 2 contributions related with the alignment process and indication behavior in D1.2:
  - bruckman_3ct_01a_200213
  - bruckman_3ct_02a_200213
- As a conclusion of the technical discussions during the Teleconference I made some fine-tuning to the requested changes.
  - I removed the request to change to a fixed FAS subset for alignment/alignment loss monitoring.
- In this contribution I present the detailed changes to D1.2 related with my comments.
- The reason and advantages of the proposed changes are described in the above mentioned contributions.

Summary of changes to D1.2

- Lane synchronization (comments: 15, 18, 21, 22, 23, 24, 25, 26, 27, 30):
  - Separate the lane identification from the lane synchronization process
  - Keep frame start location during re-synchronization
  - Changes:
    - Update the synchronization and synchronization loss state diagrams and related variables and counters
    - New lane identification state diagram and related variables and counters
- Deskew (comments: 19, 31, 32):
  - Fix deskew state diagram
    - Update the state diagram and related variables
- SIGNAL_OK indication (comments: 11, 17, 20, 28, 29):
  - Add stability counter
    - New fec_align_indication state diagram and related variables and counters
- Related changes to clause 153.2.3.3.1 and MDIO (comments: 6, 34, 35, 36)

SC-FEC frame synchronization

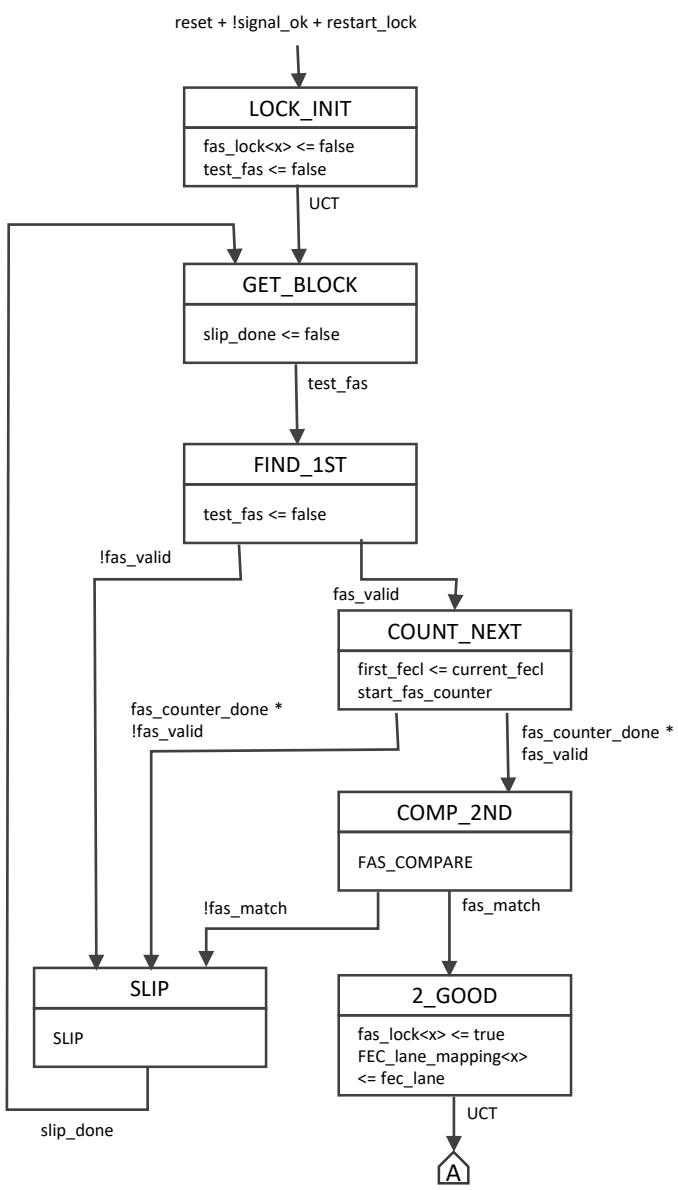
- Change
  - fas_valid
    - Boolean variable that is set to true if the received 6-octet sequence is a valid frame alignment signal. The frame alignment signal consists of 40 known bits and 8 variable bits. The sequence is considered to be valid if four of the first five octets match the known bits of the pattern described in 153.2.3.2.4~~, and the 6th octet represents a numerical value in the range 0 to 239 with the most-significant bit transmitted first~~.
- Remove
  - FAS_COMPARE function and fas_match variable
- Add
  - fas_in_counter
    - Counts the 16 320 octets between the starting position of one FAS and the expected starting position of the next FAS on a FEC lane for the alignment verification state machine.
      - Note: This counter has been added so that the FAS position is kept during alignment loss until a new FAS position is discovered by the alignment state machine.

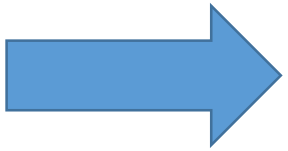
SC-FEC synchronization state diagram details

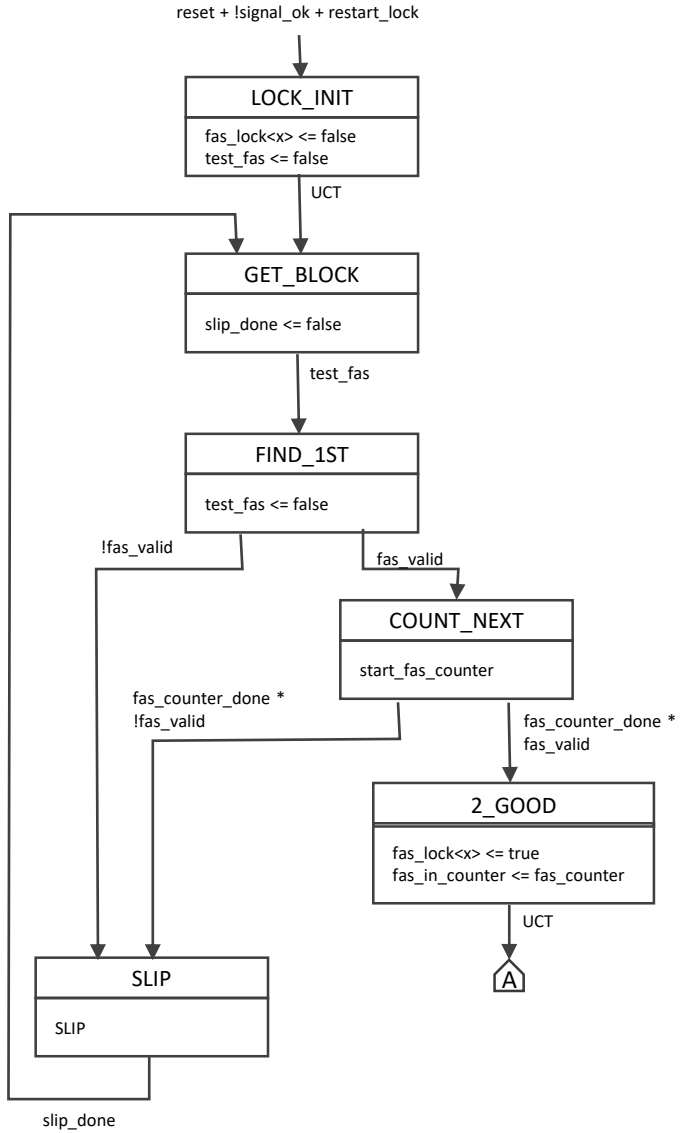
- Synchronization (1):
  - Lane identification variables set removed from states COUNT_NEXT and 2_GOOD.
  - COMP_2ND state removed to simplify the state machine since the FAS_COMPARE function is not required now.
  - fas_in_counter used by the SC-FEC synchronization loss detection state machine is set to the fas_counter value only once a new FAS location is identified.

- Synchronization loss (2):
  - FAS_COMPARE state removed to simplify the state machine since the FAS_COMPARE function is not required now.
  - Use fas_in_counter instead of fas_counter, so that during a re-synchronization the FAS location is retained until a new FAS location is identified by the synchronization state machine.
  - Note that if the synchronization loss was due to BER, the new FAS location will be equal to the previous one.

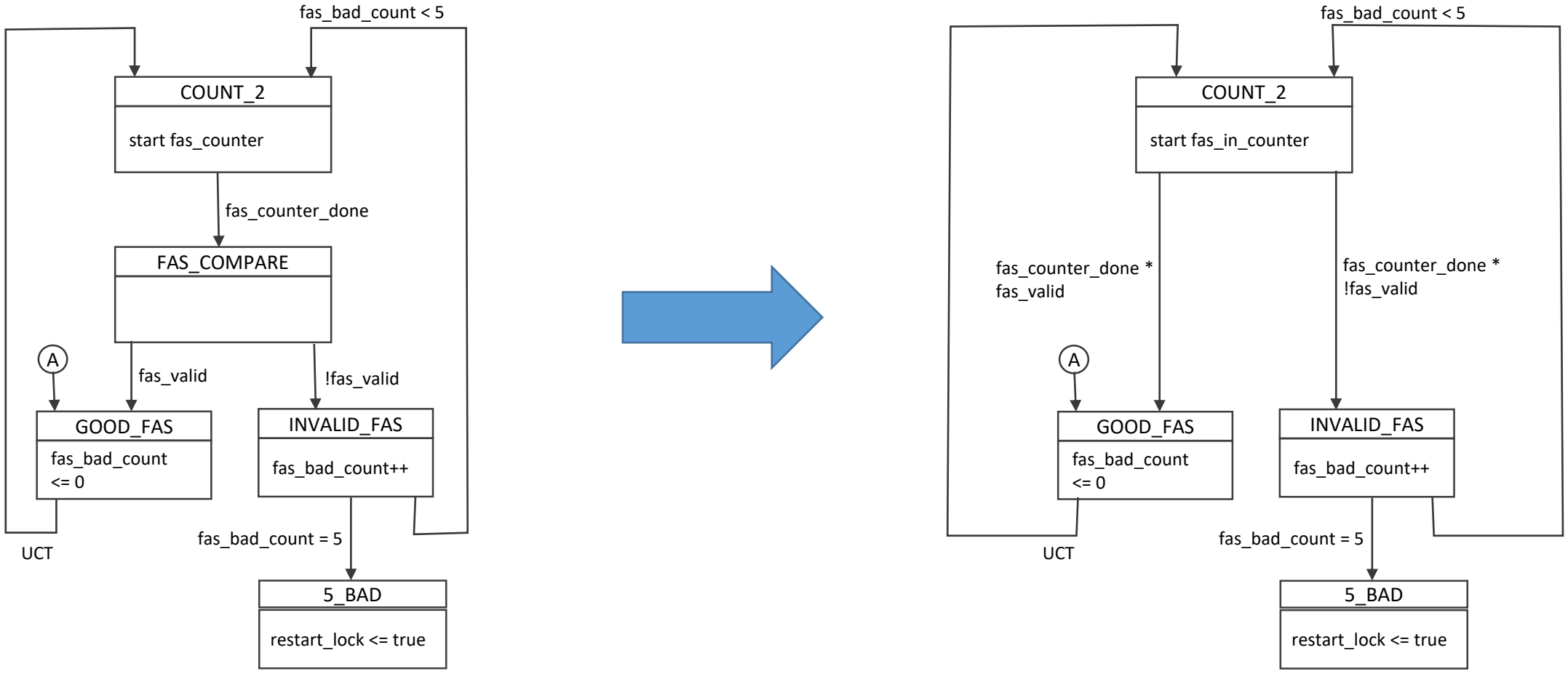
SC-FEC synchronization state diagram (1) - Change







SC-FEC synchronization state diagram (2) - Change



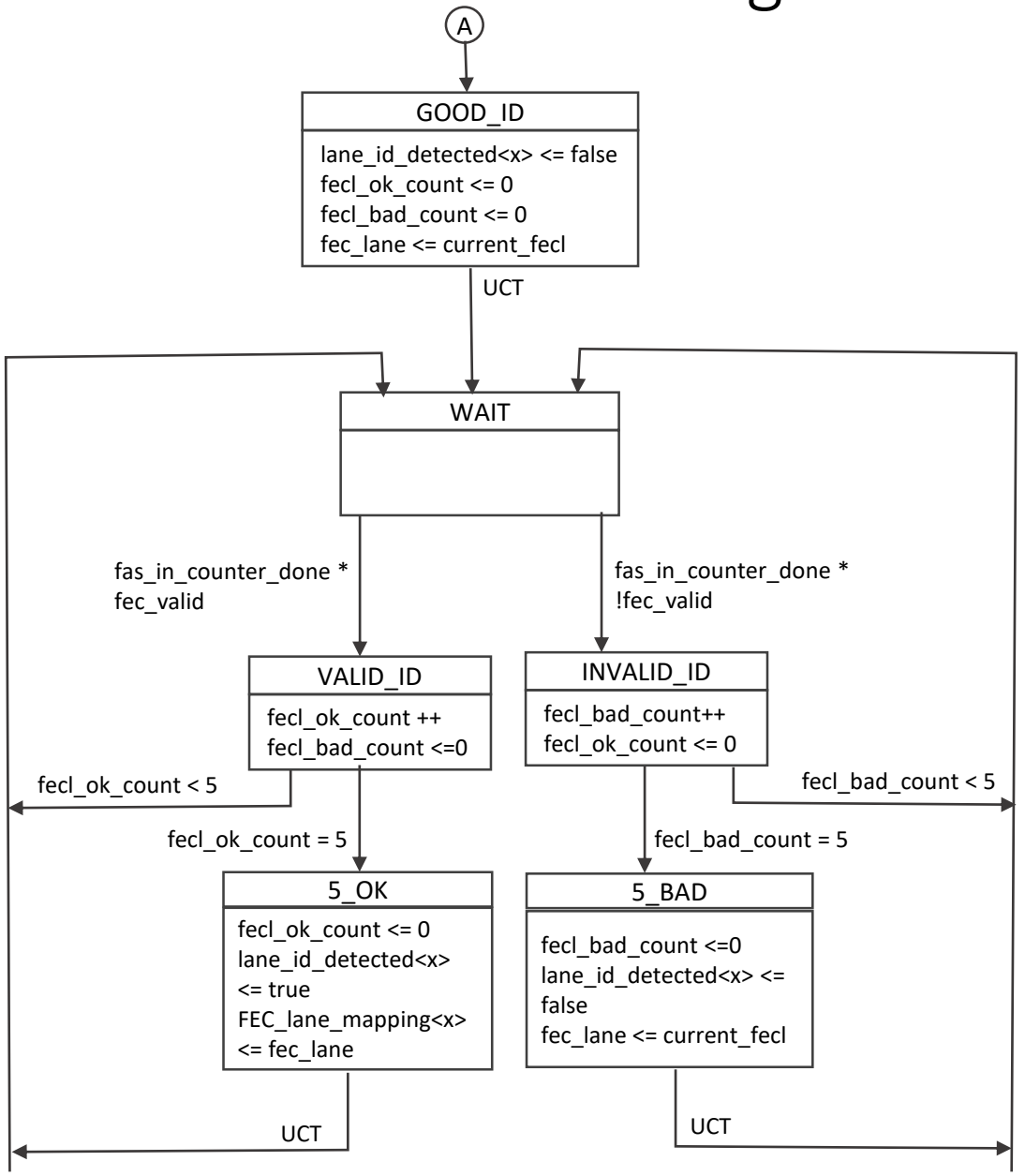
Lane identification

- Change
  - current_fecl
    - A variable that holds the FEC lane number corresponding to the current FAS that is recognized on a given lane of the PMA service interface. ~~It is compared to the variable first_fecl to confirm that the location of the FAS has been detected.~~
  - fec_lane
    - A variable that holds the FEC lane number (0 to 19) received on lane x of the PMA service interface ~~when fas_lock<x>=true~~. The FEC lane number is determined by the 6th octet of the FAS, interpreted with the most significant bit transmitted first, modulo 20.
- Add
  - fecl_valid
    - Boolean variable that is set to true if the received 6th FAS octet represents a numerical value in the range 0 to 239 with the most-significant bit transmitted first, and its modulo 20 value is equal to the variable fec_lane.
  - lane_id_detected<x>
    - Boolean variable that is set to true when the receiver has detected the lane identification for a given lane on the PMA service interface, where x = 0:19.
  - fecl_ok_count
    - Counts the number of consecutive 6th FAS octets that match the expected value for a given FEC lane.
  - fecl_bad_count
    - Counts the number of consecutive 6th FAS octets that don’t match the expected value for a given FEC lane.
  - Note: This process keeps the last known FEC_lane_mapping until a new fec_lane is discovered by the lane identification state machine.

Line identification state diagram details

- Start only after synchronization acquired.
- New lane_id_detected<x> x=0:19 variable added
  - Added also as an input to MDIO
- New Lane ID accepted if the same Lane ID value is detected 5 frames in a row.
  - New value written to FEC_lane_mapping<x> for the deskew state machine and the MDIO.
  - Correspondent lane_id_detected<x> set to “TRUE”.
- If a different value than the accepted Lane ID value is detected 5 frames in a row.
  - Test new value for acceptance.
  - Correspondent lane_id_detected<x> set to “FALSE”.
- The accepted Lane ID is retained until a new Lane ID is detected.
- Note that if the Lane ID loss was due to BER, the new Lane ID will be equal to the previous one.

Lane identification state diagram - New



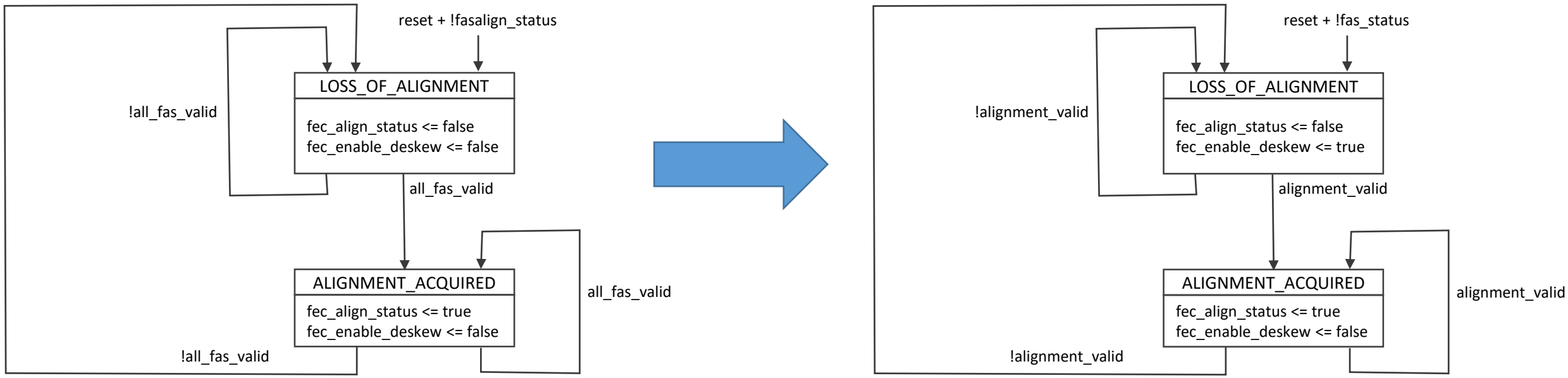
SC-FEC Deskew

- Add
  - fas_status
    - A Boolean variable that is true when all lanes are in fas_lock and false when at least one lane is not in fas_lock.
  - alignment_valid
    - Boolean variable that is set true if all lanes are aligned. It is true when each lane is in fas_lock, with each lane locked to a unique FEC lane number, and when all lanes are deskewed. Otherwise, alignment_valid is false.
  - fec_enable_deskew
    - A Boolean variable that enables and disables the deskew process. ~~Received bits may be discarded whenever deskew is enabled.~~ The alignment start shall be maintained when fec_align_status is false. It is set to true when deskew is enabled and set to false when deskew is disabled.

SC-FEC Deskew state diagram details

- Replace all_fas_valid (not defined) with alignment_valid.
- Replace fasalign_status (not defined) with fas_status.
- Set fec_enable_deskew to “TRUE” in the LOSS_OF_ALIGNMENT state to start deskew process.
- Note that these changes make the Deskew state diagram similar to Figure 82–14: PCS deskew state diagram.
- Define fec_enable_deskew in a similar way as defined in clause 91.5.4.2.1, but do not allow bits to be discarded during the deskew process.
  - The deskew process may be frequently started due to high pre-FEC BER, if we allow discarding bits during the process communication will be impaired.

SC-FEC deskew state diagram - Change



SIGNAL_OK indication

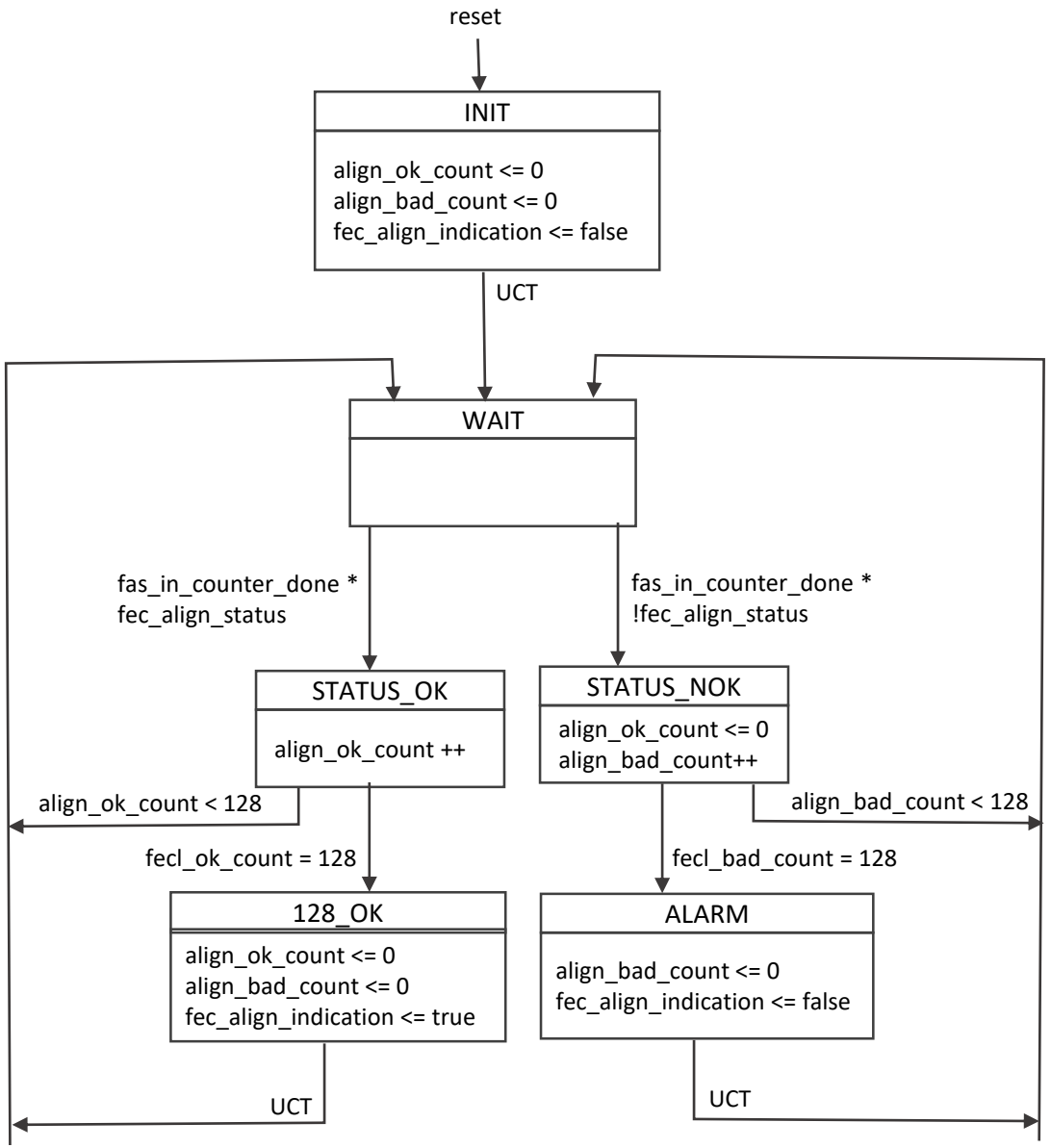
- Change
  - The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by ~~fec_align_status~~ fec_align_indication equal to true, and block delineation has been acquired as indicated by rx_block_lock equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by ~~fec_align_status~~ fec_align_indication equal to false, or rx_block_lock equal to false. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_i.indication primitives are undefined.
- Add
  - fecl_align_indication
    - Boolean variable that is set to true if the variable fec_align_status was true for the last 128 FEC lane frames. Otherwise it is set to false.
  - align_ok_count
    - Counts the number of consecutive FEC lane frames for which fecl_align_status was true.
  - align_bad_count
    - Counts the number of FEC lane frames for which fecl_align_status was false.

  - Note: This process provides a stable SIGNAL_OK even for high pre-FEC scenarios. To provide for the case of intermittent out-of-locks (fec_align_status is false), the integrating timer is not reset to zero until an in-lock (fec_align_status is true) condition persists continuously for 128 SC-FEC frames (~3 msec).

SIGNAL_OK monitor state diagram details

- State machine runs continuously and monitors fec_align_status.
- New fec_align_indication variable defined to contain the “debounced” fec_align_status value.
  - fec_align_indication drives the SIGNAL_OK parameter
- fec_align_indication is set to “TRUE” when align_ok_count reaches 128 and to “FALSE” when align_bad_count reaches 128.
- align_ok_count cleared each time a loss of alignment is detected.
- align_bad_count cleared only if align_ok_count reaches 128.
- The scheme provides for intermittent losses and is similar to the scheme defined in ITU-T G.798.
  - Note that ITU-T G.798 defines a 3 msec integration time per lane, while the proposed scheme is one process for the whole signal.

SIGNAL_OK monitor state diagram - New



Other clauses updates

- 45.2.1.186aj SC-FEC lane mapping, lane 0 register (Register 1.2250)

  The assignment of bits in the SC-FEC lane mapping, lane 0 register is shown in Table 45–150ai. When the SC-FEC described in Clause 153 detects ~~and locks the FAS~~ the lane identification on PMA service interface lane 0, the detected SC-FEC lane number is recorded in this register. The contents of the SC-FEC lane mapping, lane 0 register is valid when the SC-FEC ~~FAS lock 0 bit (1.2246.0)~~ lane identification 0 bit (1.xxxx.0) is set to one and is invalid otherwise ~~(see 45.2.1.186ah.9)~~ (see 45.2.1.186ai.8).

- 153.2.3.3.1 Lane lock and deskew

  The SC-FEC receive function forms 20 bit streams by concatenating the bits from each of the 20 PMA:IS_UNITDATA_i.indication primitives in the order they are received. It obtains lock to the FAS as specified by the SC-FEC synchronization state diagram shown in Figure 153–7 and detects the lane identification as specified by the lane identification state diagram shown in Figure 153-x. After frame alignment lock and lane identification is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 153–8. The FEC receive function shall support a maximum Skew of TBD ns between FEC lanes and a maximum Skew Variation of TBD ns.

  Alignment loss events are expected frequently in cases for which the pre-FEC BER is high. To provide a stable alarm indication to the upper layers, the SC-FEC sublayer alarm indication generation is shown in Figure 153-y.

- Table 153–2—MDIO/SC-FEC Status variable mapping
  - In row 2 column 4 change: fec_align_status to fec_align_indication
  - Add the following row after the second row:

SC-FEC line identification x, x=0 to 19	SC-FEC line identification status 1 and 2 registers	1.xxxx.7:0 1.zzzz.11:0	lane_id_detected<x>

MDIO additions (1)

45.2.1.186ai SC-FEC lane identification status 1 register (Register 1.xxxx)

The assignment of bits in the SC-FEC lane identification status 1 register is shown in Table 45–150xx.

Table 45–150xx—SC-FEC lane identification status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.xxxx.15:8	Reserved	Value always 0	RO
1.xxxx.7	SC-FEC lane identification 7	1 = Lane 7 lane identified 0 = Lane 7 lane not identified	RO
1.xxxx.6	SC-FEC lane identification 6	1 = Lane 6 lane identified 0 = Lane 6 lane not identified	RO
1.xxxx.5	SC-FEC lane identification 5	1 = Lane 5 lane identified 0 = Lane 5 lane not identified	RO
1.xxxx.4	SC-FEC lane identification 4	1 = Lane 4 lane identified 0 = Lane 4 lane not identified	RO
1.xxxx.3	SC-FEC lane identification 3	1 = Lane 3 lane identified 0 = Lane 3 lane not identified	RO
1.xxxx.2	SC-FEC lane identification 2	1 = Lane 2 lane identified 0 = Lane 2 lane not identified	RO
1.xxxx.1	SC-FEC lane identification 1	1 = Lane 1 lane identified 0 = Lane 1 lane not identified	RO
1.xxxx.0	SC-FEC lane identification 0	1 = Lane 0 lane identified 0 = Lane 0 lane not identified	RO

[a]RO = Read only

MDIO additions (2)

45.2.1.186ai.1 SC-FEC lane identification 7 (1.xxxx.7)

When read as a one, bit 1.xxxx.7 indicates that the SC-FEC receiver has acquired the identification of lane 7 of the PMA service interface. When read as a zero, bit 1.xxxx.7 indicates that the SC-FEC receiver has not acquired the identification of lane 7 of the PMA service interface. This bit reflects the state of lane_id_detected<7> (see 153.2.4.1.1).

45.2.1.186ai.2 SC-FEC lane identification 6 (1.xxxx.6)

When read as a one, bit 1.xxxx.6 indicates that the SC-FEC receiver has acquired the identification of lane 6 of the PMA service interface. When read as a zero, bit 1.xxxx.6 indicates that the SC-FEC receiver has not acquired the identification of lane 6 of the PMA service interface. This bit reflects the state of lane_id_detected<6> (see 153.2.4.1.1).

45.2.1.186ai.3 SC-FEC lane identification 5 (1.xxxx.5)

When read as a one, bit 1.xxxx.5 indicates that the SC-FEC receiver has acquired the identification of lane 5 of the PMA service interface. When read as a zero, bit 1.xxxx.5 indicates that the SC-FEC receiver has not acquired the identification of lane 5 of the PMA service interface. This bit reflects the state of lane_id_detected<5> (see 153.2.4.1.1).

45.2.1.186ai.4 SC-FEC lane identification 4 (1.xxxx.4)

When read as a one, bit 1.xxxx.4 indicates that the SC-FEC receiver has acquired the identification of lane 4 of the PMA service interface. When read as a zero, bit 1.xxxx.4 indicates that the SC-FEC receiver has not acquired the identification of lane 4 of the PMA service interface. This bit reflects the state of lane_id_detected<4> (see 153.2.4.1.1).

45.2.1.186ai.5 SC-FEC lane identification 3 (1.xxxx.3)

When read as a one, bit 1.xxxx.3 indicates that the SC-FEC receiver has acquired the identification of lane 3 of the PMA service interface. When read as a zero, bit 1.xxxx.3 indicates that the SC-FEC receiver has not acquired the identification of lane 3 of the PMA service interface. This bit reflects the state of lane_id_detected<3> (see 153.2.4.1.1).

45.2.1.186ai.6 SC-FEC lane identification 2 (1.xxxx.2)

When read as a one, bit 1.xxxx.2 indicates that the SC-FEC receiver has acquired the identification of lane 2 of the PMA service interface. When read as a zero, bit 1.xxxx.2 indicates that the SC-FEC receiver has not acquired the identification of lane 2 of the PMA service interface. This bit reflects the state of lane_id_detected<2> (see 153.2.4.1.1).

45.2.1.186ai.7 SC-FEC lane identification 1 (1.xxxx.1)

When read as a one, bit 1.xxxx.1 indicates that the SC-FEC receiver has acquired the identification of lane 1 of the PMA service interface. When read as a zero, bit 1.xxxx.1 indicates that the SC-FEC receiver has not acquired the identification of lane 1 of the PMA service interface. This bit reflects the state of lane_id_detected<1> (see 153.2.4.1.1).

45.2.1.186ai.8 SC-FEC lane identification 0 (1.xxxx.0)

When read as a one, bit 1.xxxx.0 indicates that the SC-FEC receiver has acquired the identification of lane 0 of the PMA service interface. When read as a zero, bit 1.xxxx.0 indicates that the SC-FEC receiver has not acquired the identification of lane 0 of the PMA service interface. This bit reflects the state of lane_id_detected<0> (see 153.2.4.1.1).

MDIO additions (3)

45.2.1.186aj SC-FEC lane identification status 2 register (Register 1.zzzz)

The assignment of bits in the SC-FEC lane identification status 2 register is shown in Table 45–150zz.

Table 45–150zz—SC-FEC lane identification status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.zzzz.15:12	Reserved	Value always 0	RO
1.zzzz.11	SC-FEC lane identification 19	1 = Lane 19 lane identified 0 = Lane 19 lane not identified	RO
1.zzzz.10	SC-FEC lane identification 18	1 = Lane 18 lane identified 0 = Lane 18 lane not identified	RO
1.zzzz.9	SC-FEC lane identification 17	1 = Lane 17 lane identified 0 = Lane 17 lane not identified	RO
1.zzzz.8	SC-FEC lane identification 16	1 = Lane 16 lane identified 0 = Lane 16 lane not identified	RO
1.zzzz.7	SC-FEC lane identification 15	1 = Lane 15 lane identified 0 = Lane 15 lane not identified	RO
1.zzzz.6	SC-FEC lane identification 14	1 = Lane 14 lane identified 0 = Lane 14 lane not identified	RO
1.zzzz.5	SC-FEC lane identification 13	1 = Lane 13 lane identified 0 = Lane 13 lane not identified	RO
1.zzzz.4	SC-FEC lane identification 12	1 = Lane 12 lane identified 0 = Lane 12 lane not identified	RO
1.zzzz.3	SC-FEC lane identification 11	1 = Lane 11 lane identified 0 = Lane 11 lane not identified	RO
1.zzzz.2	SC-FEC lane identification 10	1 = Lane 10 lane identified 0 = Lane 10 lane not identified	RO
1.zzzz.1	SC-FEC lane identification 9	1 = Lane 9 lane identified 0 = Lane 9 lane not identified	RO
1.zzzz.0	SC-FEC lane identification 8	1 = Lane 8 lane identified 0 = Lane 8 lane not identified	RO

[a]RO = Read only

MDIO additions (4)

45.2.1.186aj.1 SC-FEC lane identification 19 (1.zzzz.19)

When read as a one, bit 1.zzzz.19 indicates that the SC-FEC receiver has acquired the identification of lane 19 of the PMA service interface.
When read as a zero, bit 1.zzzz.19 indicates that the SC-FEC receiver has not acquired the identification of lane 19 of the PMA service interface.
This bit reflects the state of lane_id_detected<19> (see 153.2.4.1.1).

45.2.1.186aj.2 SC-FEC lane identification 18 (1.zzzz.18)

When read as a one, bit 1.zzzz.18 indicates that the SC-FEC receiver has acquired the identification of lane 18 of the PMA service interface.
When read as a zero, bit 1.zzzz.18 indicates that the SC-FEC receiver has not acquired the identification of lane 18 of the PMA service interface.
This bit reflects the state of lane_id_detected<18> (see 153.2.4.1.1).

45.2.1.186aj.3 SC-FEC lane identification 17 (1.zzzz.17)

When read as a one, bit 1.zzzz.17 indicates that the SC-FEC receiver has acquired the identification of lane 17 of the PMA service interface.
When read as a zero, bit 1.zzzz.17 indicates that the SC-FEC receiver has not acquired the identification of lane 17 of the PMA service interface.
This bit reflects the state of lane_id_detected<17> (see 153.2.4.1.1).

45.2.1.186aj.4 SC-FEC lane identification 16 (1.zzzz.16)

When read as a one, bit 1.zzzz.16 indicates that the SC-FEC receiver has acquired the identification of lane 16 of the PMA service interface.
When read as a zero, bit 1.zzzz.16 indicates that the SC-FEC receiver has not acquired the identification of lane 16 of the PMA service interface.
This bit reflects the state of lane_id_detected<16> (see 153.2.4.1.1).

45.2.1.186aj.5 SC-FEC lane identification 15 (1.zzzz.15)

When read as a one, bit 1.zzzz.15 indicates that the SC-FEC receiver has acquired the identification of lane 15 of the PMA service interface.
When read as a zero, bit 1.zzzz.15 indicates that the SC-FEC receiver has not acquired the identification of lane 15 of the PMA service interface.
This bit reflects the state of lane_id_detected<15> (see 153.2.4.1.1).

45.2.1.186aj.6 SC-FEC lane identification 14 (1.zzzz.14)

When read as a one, bit 1.zzzz.14 indicates that the SC-FEC receiver has acquired the identification of lane 14 of the PMA service interface.
When read as a zero, bit 1.zzzz.14 indicates that the SC-FEC receiver has not acquired the identification of lane 14 of the PMA service interface.
This bit reflects the state of lane_id_detected<14> (see 153.2.4.1.1).

MDIO additions (5)

45.2.1.186aj.7 SC-FEC lane identification 13 (1.zzzz.13)

When read as a one, bit 1.zzzz.13 indicates that the SC-FEC receiver has acquired the identification of lane 13 of the PMA service interface. When read as a zero, bit 1.zzzz.13 indicates that the SC-FEC receiver has not acquired the identification of lane 13 of the PMA service interface. This bit reflects the state of lane_id_detected<13> (see 153.2.4.1.1).

45.2.1.186aj.8 SC-FEC lane identification 12 (1.zzzz.12)

When read as a one, bit 1.zzzz.12 indicates that the SC-FEC receiver has acquired the identification of lane 12 of the PMA service interface. When read as a zero, bit 1.zzzz.12 indicates that the SC-FEC receiver has not acquired the identification of lane 12 of the PMA service interface. This bit reflects the state of lane_id_detected<12> (see 153.2.4.1.1).

45.2.1.186aj.9 SC-FEC lane identification 11 (1.zzzz.11)

When read as a one, bit 1.zzzz.11 indicates that the SC-FEC receiver has acquired the identification of lane 11 of the PMA service interface. When read as a zero, bit 1.zzzz.11 indicates that the SC-FEC receiver has not acquired the identification of lane 11 of the PMA service interface. This bit reflects the state of lane_id_detected<11> (see 153.2.4.1.1).

45.2.1.186aj.10 SC-FEC lane identification 10 (1.zzzz.10)

When read as a one, bit 1.zzzz.10 indicates that the SC-FEC receiver has acquired the identification of lane 18 of the PMA service interface. When read as a zero, bit 1.zzzz.10 indicates that the SC-FEC receiver has not acquired the identification of lane 10 of the PMA service interface. This bit reflects the state of lane_id_detected<10> (see 153.2.4.1.1).

45.2.1.186aj.11 SC-FEC lane identification 9 (1.zzzz.9)

When read as a one, bit 1.zzzz.9 indicates that the SC-FEC receiver has acquired the identification of lane 9 of the PMA service interface. When read as a zero, bit 1.zzzz.9 indicates that the SC-FEC receiver has not acquired the identification of lane 9 of the PMA service interface. This bit reflects the state of lane_id_detected<9> (see 153.2.4.1.1).

45.2.1.186aj.12 SC-FEC lane identification 8 (1.zzzz.8)

When read as a one, bit 1.zzzz.8 indicates that the SC-FEC receiver has acquired the identification of lane 8 of the PMA service interface. When read as a zero, bit 1.zzzz.8 indicates that the SC-FEC receiver has not acquired the identification of lane 8 of the PMA service interface. This bit reflects the state of lane_id_detected<8> (see 153.2.4.1.1).