

Approved Responses

IEEE P802.3cy D2.1 10G+ Auto Task Force 1st Working Group recirculation ballot comments

CI 00 SC 0 P L # 785

Dawe, Piers Nvidia

Comment Type E Comment Status A

"groups of 130 65B blocks": elsewhere there are 64B/65B block and 65-bit block

SuggestedRemedy

Change "65B block" to "64B/65B block" or "65-bit block" as appropriate, throughout

Response Response Status C

ACCEPT IN PRINCIPLE.

Change "65B block" to "64B/65B block" throughout the text of the draft. Usage in figures to remain "65B block" consistent with IEEE Std 802.3-2022.

CI 45 SC 45.2.1.245.1 P27 L20 # 791

Wienckowski, Natalie General Motors

Comment Type E Comment Status A EZ

SuggestedRemedy

Delete red Editorial note.

Response Response Status C

ACCEPT.

CI 78 SC 78.5 P30 L10 # 804

Graba, Jim Broadcom

Comment Type T Comment Status A late

Tphy\_shrink\_tx and Tw\_sys\_rx numbers are incorrect. Case-4 Tw\_sys\_tx and Tw\_phy latencies are in also incorrect.

SuggestedRemedy

Change the incorrect numbers as indicated on page 6 of graba\_3cy\_01\_0920.pdf.

Response Response Status C

ACCEPT IN PRINCIPLE.

Change the incorrect numbers as highlighted on page 6 of graba\_3cy\_01a\_0920.pdf.

CI 105 SC 105.1.2 P33 L42 # 792

McClellan, Brett Marvell

Comment Type E Comment Status A EZ

typo in editor's instruction

SuggestedRemedy

change 'Insert a new bullet e) in 10.5.2 as shown below.' to 'Insert a new bullet e) in 105.1.2 as shown below.'

Response Response Status C

ACCEPT.

CI 165 SC 165.1.3 P37 L35 # 784

Dawe, Piers Nvidia

Comment Type E Comment Status A EZ

14 062.5 MBd - as the number is more than 10,000 and the space in a number with a decimal part is hard to parse, ...

SuggestedRemedy

It would be better to put this as 14.0625 GBd throughout. 8 changes.

Response Response Status C

ACCEPT.

CI 165 SC 165.1.3 P37 L35 # 793

McClellan, Brett Marvell

Comment Type E Comment Status A EZ

D2.0 comment 637 instruction was not followed: delete 'rates'

SuggestedRemedy

implement as instructed

Response Response Status C

ACCEPT IN PRINCIPLE.

Change "transmitted at a 14 062.5 MBd rate" to "transmitted at 14 062.5 MBd"

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Cl 165 SC 165.2.2.9.1 P48 L42 # 798  
 Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marvell  
 Comment Type E Comment Status A EZ  
 the description of FALSE refers to the PCS where it should refer to the PHY (TRUE refers to the PHY)  
 SuggestedRemedy  
 Change "FALSE PCS is not in state PCS\_Data" to "FALSE PHY is not in state PCS\_Data"  
 Response Response Status C  
 ACCEPT.

Cl 165 SC 165.3.5 P64 L21 # 802  
 Jonsson, Ragnar Marvell  
 Comment Type TR Comment Status A  
 Incorrect range in the first case in the equation.  
 SuggestedRemedy  
 Equation (165-1): change "less than or equal to 17654" to "less than 17646" OR to "less than or equal to 17645"  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 change "less than or equal to 17654" to "less than 17646"

Cl 165 SC 165.3.5 P64 L21 # 803  
 Jonsson, Ragnar Marvell  
 Comment Type ER Comment Status A  
 Incorrect equation numbering: Equaiton identifier (165-1) was previously used for equation on page 58, line 36.  
 SuggestedRemedy  
 Update equation numbers to have consistent unique numbering throughtout the document.  
 Response Response Status C  
 ACCEPT.

Cl 165 SC 165.3.7.3 P68 L16 # 794  
 McClellan, Brett Marvell  
 Comment Type T Comment Status A  
 missing a description of Figure 165–14—EEE transmit state diagram  
 SuggestedRemedy  
 insert "The EEE transmit state diagram shown in Figure 165–14 controls transitions between normal operation and low power idle."  
 Response Response Status C  
 ACCEPT.

Cl 165 SC 165.4.2.4.3 P67 L6 # 786  
 Dawe, Piers Nvidia  
 Comment Type E Comment Status A  
 Partial PHY frame count  
 SuggestedRemedy  
 Delete "PHY". There are a few more  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 Change all instances of "partial PHY frame count" to "partial frame count"  
 Comment is actually against page 77, line 6.

Cl 165 SC 165.4.2.4.6 P78 L51 # 790  
 Wienckowski, Natalie General Motors  
 Comment Type T Comment Status A DataSwPFC24  
 Change based on D2.0 comments #647 and #471.  
 SuggestedRemedy  
 Change: DataSwPFC24 shall be set to an integer multiple of 32. When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary.  
 To: When the value of DataSwPFC24 is a multiple of 32 the switch from PAM2 to PAM4 occurs on a L=8 superframe boundary.  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 See comment #795

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CI 165 SC 165.4.2.4.6 P78 L52 # 795  
 McClellan, Brett Marvell  
 Comment Type E Comment Status A DataSwPFC24  
 delete sentence per instruction of D2.0 comment 710 resolution  
 SuggestedRemedy  
 When the value of  
 delete "When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary. DataSwPFC24"  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 Delete "When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary."

CI 165 SC 165.4.2.4.6 P79 L1 # 789  
 Wienckowski, Natalie General Motors  
 Comment Type E Comment Status A EZ  
 SuggestedRemedy  
 Delete red Editorial note.  
 Response Response Status C  
 ACCEPT.

CI 165 SC 165.4.2.6 P81 L10 # 787  
 Dawe, Piers Nvidia  
 Comment Type E Comment Status A  
 "signaling rate of the SEND\_S signal shall be 703.125 MHz" Is that signaling rate (MBd) or pattern repetition rate?  
 SuggestedRemedy  
 Change MHz to MBd?  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 The following changes are made:  
 Delete the text "The nominal signaling rate of the SEND\_S signal shall be 703.125 MHz."

Revise the existing statement by adding statement in <<>>:  
 "An implementation of MASTER and SLAVE PHY SEND\_S PN sequence generators by linear-feedback shift registers is shown in Figure 165–20. The bits stored in the shift register delay line at time n are denoted by Sn[7:0]. <<The symbols of the shift register sequence Sn[] shall be generated at a rate of 703.125 MHz.>> At each symbol period, the shift register is advanced by one bit, and one new bit represented by Sn[0] is generated. The PN sequence generator shift registers shall be reset to a value of Sn[7:0] = 0000 0001 upon entering into the TRANSMIT\_DISABLE state (see Figure 165–20) or on the transmission of the first symbol of the alert sequence. The receiver may not necessarily receive a continuous PN sequence between separate periods of the SEND\_S signal."  
 Update PICS as needed

CI 165 SC 165.5.2 P93 L25 # 788  
 Dawe, Piers Nvidia  
 Comment Type E Comment Status A EZ  
 "25GBASE-T1: 1x" looks like a leftover from a diagram that included more lanes  
 SuggestedRemedy  
 Delete  
 Response Response Status C  
 ACCEPT IN PRINCIPLE.  
 Delete ": 1x"

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Cl 165 SC 165.5.3 P93 L17 # 781

Dawe, Piers Nvidia  
 Comment Type T Comment Status R

For some of the measurements where a high speed signal is to be observed with a scope, there should be a specified scope bandwidth. fb x 3/4 is usual. This standardises the measurement and keeps some irrelevant instrument and DUT noise out of it.

SuggestedRemedy

This would be beneficial for 165.5.3.2 Transmitter linearity (SNDR), 165.5.3.3.1, 2 Transmit MDI jitter in MASTER mode and 165.5.3.5, and harmless for some others such as droop.

Response Response Status C

REJECT.

No specific change proposed.

Cl 165 SC 165.5.3.3 P95 L5 # 782

Dawe, Piers Nvidia  
 Comment Type T Comment Status A

Jitter measurement bandwidth "at least 200 MHz" same as it was in 149 for a slower divided clock, and open ended.

SuggestedRemedy

Should it be increased? Give a value or range rather than "at least"

Response Response Status C

ACCEPT IN PRINCIPLE.

Delete "at least" from the statement.

The number was left at 200MHz intentionally and will not be modified.

Cl 165 SC 165.5.3.3 P95 L8 # 783

Dawe, Piers Nvidia  
 Comment Type T Comment Status R

Measuring jitter on 0.4 ms blocks with no clock recovery unit in the measurement gives an extremely low (~ kHz) implied high-pass jitter measurement corner. 165.5.3.3.2 has fn = 2.5 MHz which is much higher.

SuggestedRemedy

Should there be a "soft" CRU function not just linear regression in the TIE analysis?

Response Response Status C

REJECT.

The current system design is as intended. No changes to the draft needed.

Cl 165 SC 165.5.3.4 P96 L1 # 799

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve  
 Comment Type T Comment Status R LFL

I realize this is out of scope, and the comment is made to put the issue on the table - for resolution at initial SA ballot. The lower frequency ranges for the PHY, Link Segment specifications, and MDI are all over the place. Starting at 0 Hz is not going to be practical for measurements of a PSD going to up to 13.75 GHz. Likewise, the ANEXT and AFEXT loss are constrained starting at 1 MHz - also too low for practicality. Additionally, the TX PSD lower bound frequency is 5 MHz - below the link segment low frequency limit of the insertion loss. For all of these, going this low won't be necessary for link segments starting at 10 MHz. Suggest they be aligned at 10 MHz.

Unlike my subsequent comments on return loss, I think this comment is likely ready to make the change.

SuggestedRemedy

Change low frequency limit for Upper TX PSD mask (eq 165-6, Pg 96 line 1), Lower TX PSD mask (eq 165-7, Pg 96 line 7), PSANEXT (eq 165-35, Pg 108 line 24), and PSAFEXT (eq 165-36, Pg 109 line 18) to 10 MHz.

Response Response Status C

REJECT.

This comment is out of scope for this recirculation. The issue was recorded in the action item list for D3.0 study.

Cl 165 SC 165.7.1.3.1 P102 L51 # 800

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve  
 Comment Type T Comment Status R LFL

(also out of scope)  
 Link segment return loss specifications start at 30 MHz, whereas the link segment return loss is constrained (at least) by the Insertion loss between 10 MHz and 30 MHz (at least 6.8dB RL at 10 MHz to meet the IL at 10 MHz)

While I've proposed a remedy, I think this needs further thought and I would be OK rejecting this comment and working on it with the TF for initial SA ballot.

SuggestedRemedy

Consider changing the low frequency limit for link segment return loss Eq 165-17 at pg 102 line 51 from 30 MHz to 10 Mhz and adding a frequency range from 10 Mhz to 30 MHz to Equation 165-17 with value of  $20 - 6.5 * (30-f)/10$  dB  $10 \leq f < 30$  MHz.

Response Response Status C

REJECT.

This comment is out of scope for this recirculation. The issue was recorded in the action item list for D3.0 study.

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Cl 165 SC 165.7.1.3.4 P106 L13 # 796

Sedarat, Hossein Ethernovia

Comment Type T Comment Status A

The last sentence was eliminated from step 8 which makes the last step of ETM calculation procedure incomplete and ambiguous.

## SuggestedRemedy

Change the sentency in step 8 to: "Apply steps 3, 4, and 5 to partial response g\_n^m (instead of h\_n) to calculate the associated REM. The ETM(m) is this REM calculated for g\_n^m and evaluated at Ndiscard\_etm."

Response Response Status C

ACCEPT.

Cl 165 SC 165.7.1.6 P107 L47 # 797

Sedarat, Hossein Ethernovia

Comment Type T Comment Status A

The maximum propagation delay of 69 ns is excessively large and may unnecessarily add complexity to the echo canceller. A value of 55 ns provides roughly 10% margin with respect to available measurements of current (802.3ch-grade) and future (802.3cy-grade) cables. More discussion on the topic can be found on email reflector: <https://www.ieee802.org/3/B10GAUTO/email/msg00389.html>

## SuggestedRemedy

replace 69 ns with 55 ns.

Response Response Status C

ACCEPT IN PRINCIPLE.

replace 69 ns with 60 ns + update PICS.

Add a new sentence at the end of the paragraph: "The delay specification represents an acceptable margin over the delay of 11m of automotive cabling expected to be used."

Cl 165 SC 165.8.2.1 P110 L21 # 801

Zimmerman, George CME Consulting/APL Gp, Cisco, CommScope, Marve

Comment Type T Comment Status R LFL

Why is the link segement return loss only to 30 MHz when the MDI return loss is constrained starting at 5 MHz? These require study and should be considered for changes at initial SA ballot. Whatever considerations are important for one RL are equally applicable to the other. It probably is not relevant to constrain the MDI RL down to 0 dB RL (which is is at 5 MHz). At 10 Mhz, the lower end of the IL spec, the MDI RL is 6 dB as written.

While I've proposed a remedy, I think this needs further thought and I would be OK rejecting this comment and working on it with the TF for initial SA ballot.

## SuggestedRemedy

Change MDI return loss lower limit to 10 MHz. (eq 165-37), pg 110, line 21, maintaining the existing equation, except for the frequency limit change.

Response Response Status C

REJECT.

This comment is out of scope for this recirculation. The issue was recorded in the action item list for D3.0 study.