FEC and Interleaving

Contribution to IEEE 802.3cy

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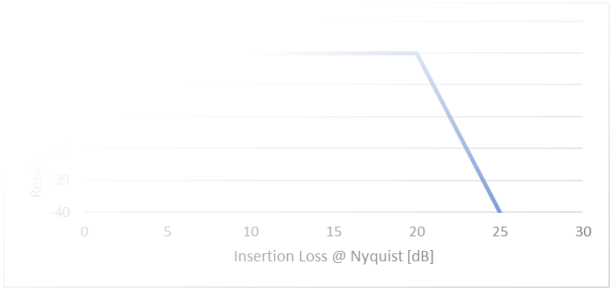
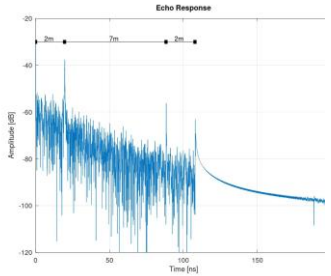
Introduction

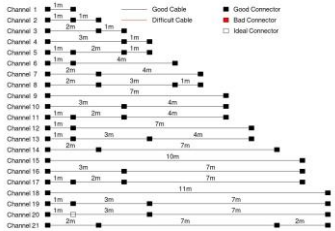
- In the Telephonic Interim Meeting on September 9, 2021, the text proposal in jonsson_etal_3cy_01a_09_21_21 was adopted
- FEC and Interleaving was further discussed in

  jonsson_3cy_01_11_09_21

  tingting_3cy_01a_11_16_21
- This contribution discusses the importance of considering coding gain when selecting FEC and the interleaving depth

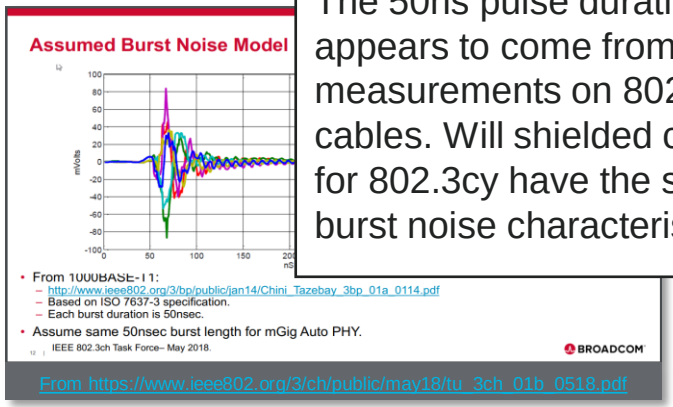






Open Questions Related to FEC and Interleaving

We have not found any specific information suggesting that the latency requirements have changed.



From https://www.ieee802.org/3/ch/public/may18/tu_3ch_01b_0518.pdf

The 50ns pulse duration appears to come from measurements on 802.3bp cables. Will shielded cables for 802.3cy have the same burst noise characteristics?

We have not found any information on this. Can we ignore overlapping pulses in our analysis?

Questions from jonsson_3cy_01_11_09_21:

- Have the latency requirements changed from 802.3ch?
- Is 50ns the right target for pulse duration?
- What is the probability of having two pulses on top of one another?

FEC must provide coding gain

Unlike some earlier standards, that had sufficient SNR margin at the limit line, the 802.3cy FEC must provide coding gain on top of the noise burst protection

The Insertion Loss Limit-Line is Challenging

100% of FEC goes to Coding Gain

Using the usual design tradeoffs

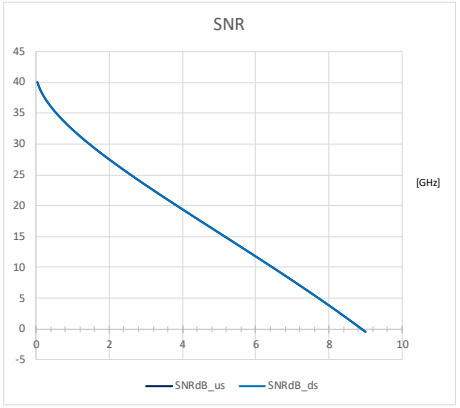
Cable at the IL Limit-Line

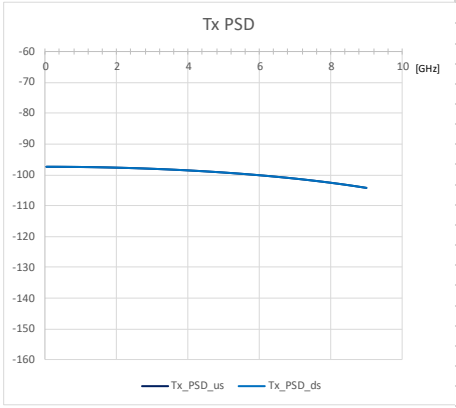
SNR Margin is too low

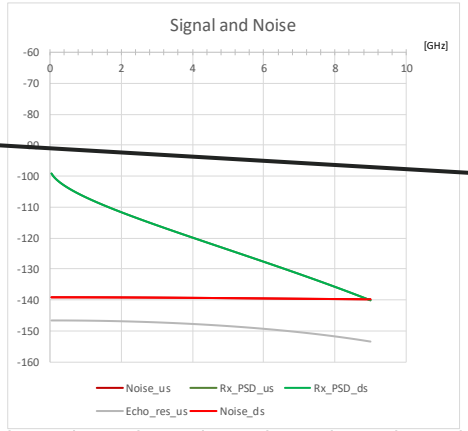
jonsson_3cy_01_04_20_21 - Channel Capacity Calculator Version 1.4

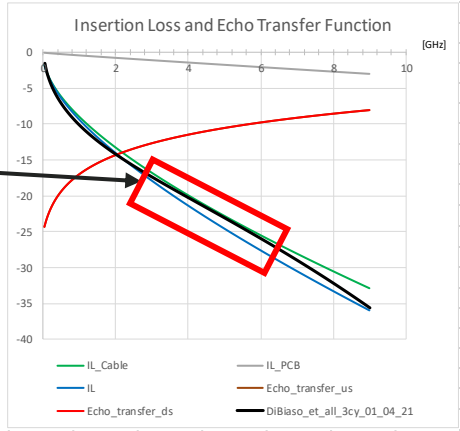
	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	60	
Max Simulation Frequency:	9.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.75	21.75
Estimated Slicer SNR [dB]:	16.75	16.75
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	-0.45	-0.45
Wire u-reflections [dB]:	-43.14	-43.14
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	30.49	30.49
Cable Insertion Loss @ Nyquist [dB]:	28.14	28.14









We Need the Coding Gain

- If most of the FEC is allocated to correcting the pulse noise, then we will not have sufficient slicer SNR
- The calculations to the right show the margin calculations when 90% and 100% of the FEC is dedicated to the pulse error
- For these cases, the SNR margin are -5.95dB and -7.25dB, respectively
- **Some of the FEC must be reserved for "Gaussian noise" coding gain**

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	10%	10%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	0.00E+00	0.00E+00
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	60	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.75	21.75
Estimated Slicer SNR [dB]:	16.75	16.75
Required Slicer SNR [dB]:	22.70	22.70
SNR Margin [dB]:	-5.95	-5.95
Wire u-reflections [dB]:	-43.14	-43.14
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	30.49	30.49
Cable Insertion Loss @ Nyquist [dB]:	28.14	28.14

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	0%	0%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	0.00E+00	0.00E+00
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	60	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.75	21.75
Estimated Slicer SNR [dB]:	16.75	16.75
Required Slicer SNR [dB]:	24.00	24.00
SNR Margin [dB]:	-7.25	-7.25
Wire u-reflections [dB]:	-43.14	-43.14
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	30.49	30.49
Cable Insertion Loss @ Nyquist [dB]:	28.14	28.14

We Need More Interleaving

- One way to get better slicer SNR is to enhance the AFE design and increase FEC interleaving
- Calculations on the right assume **-143dBm/Hz** AFE noise
- Calculations on the right assume that **50%** of the FEC capacity is dedicated to coding gain
- The RS(360,326) and RS(720,652) have about 0.6dB and 1.5dB SNR margin, respectively

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	50%	50%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	0.00E+00	0.00E+00
AFE-noise [dBm/Hz]:	-143	-143
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	60	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	24.15	24.15
Estimated Slicer SNR [dB]:	19.15	19.15
Required Slicer SNR [dB]:	18.58	18.58
SNR Margin [dB]:	0.57	0.57
Wire u-reflections [dB]:	-43.14	-43.14
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	30.49	30.49
Cable Insertion Loss @ Nyquist [dB]:	28.14	28.14

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	720	720
FEC Data Size (k):	652	652
RS-FEC Correction Efficiency:	50%	50%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	0.00E+00	0.00E+00
AFE-noise [dBm/Hz]:	-143	-143
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	60	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	24.15	24.15
Estimated Slicer SNR [dB]:	19.15	19.15
Required Slicer SNR [dB]:	17.63	17.63
SNR Margin [dB]:	1.52	1.52
Wire u-reflections [dB]:	-43.14	-43.14
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	30.49	30.49
Cable Insertion Loss @ Nyquist [dB]:	28.14	28.14

FEC and Interleaving Analysis

What is the expected performance for different FEC and interleaving designs

Analysis Description

- The objective is to guarantee when a transient occurs the bit error rate is below 1e-12
- A transient of certain duration (T_n) is considered for this purposes (e.g., 50 ns)
- The combination between the error correction capability of the code and interleaver depth will determine the burst error correction capability of the system. This capability has to be enough to guarantee that it can deal with transient noise + random errors
- For a system with a RS(N, K, m) code with error correction capability t and interleaving depth of L, the burst error protection can be calculated as $(t \cdot m \cdot L)/S$, where S is the speed of the line transmission. Also, it can be expressed in RS symbols as $t \cdot L$
- In the opposite direction we can translate the transient noise duration to RS symbols by $\lceil T_n \cdot S/m \rceil$
- In this way the remaining error correction capability expressed in RS symbols results

$$t_r = \left\lfloor t - \frac{\left\lceil \frac{T_n \cdot S}{m} \right\rceil}{L} \right\rfloor$$

- With the resulting t_r a required slicer SNR is calculated

FEC and Interleaving Options

RS Code	Interleaver Depth	Required Slicer SNR [dB]		Intrinsic Latency [ns]	Relative Complexity*
		50 ns burst	25 ns burst		
(360,326)	8	-	18.2	1124	3.7
	10	20.9	18.0	1404	4.4
	12	19.1	17.6	1685	5.2
	16	18.2	17.5	2247	6.7
(720,652)	4	-	17.5	1122	4.3
	5	19.4	17.2	1403	5.0
	6	18.3	17.0	1683	5.8
	8	17.5	16.8	2244	7.3

* Relative complexity is expressed with respect to RS(360,326) with an interleaver depth of 1. It is a relative measure of silicon area

Summarizing the FEC and Interleaving Results

- The FEC and Interleaving needs to be longer than in earlier standards that had surplus SNR margin
- The longer interleaving is manly needed on the longest cables with the most challenging SNR margin
- Both RS(360,326) and RS(720,652) can achieve the required SNR, with the right interleaving
- The maximum noise burst duration will affect the necessary interleaving, so we need to have good understanding of the maximum noise burst duration

Conclusion

There are still some open questions about latency and pulse duration for 802.3cy

The FEC must provide coding gain on top of noise burst protection

Two different RS codes with different interleaving depth were compared

We will need sufficient interleaving depth for 802.3cy to provide the necessary coding gain on top of the noise burst protection

Essential technology, done right™