
Tx Function to Rx Function Channel Considerations

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January 2021

Purpose

- **Tx Function to Rx function channel considerations**

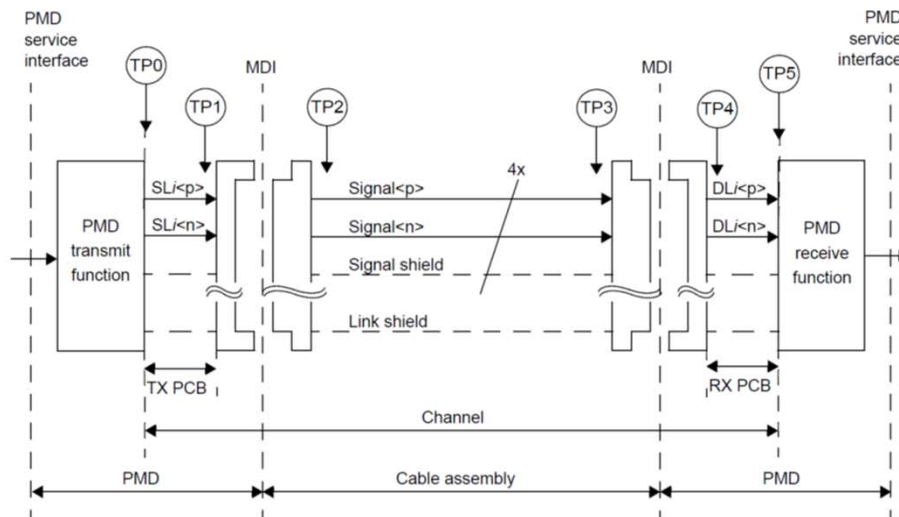
Background – 802.3bj/by/cd/ck

IEEE Standards - 25/50/100 Gb/s Operation – Shielded Cable

- 802.3bj - 100GBASE-CR4 - 2-level PAM - 25.78125 GBd per lane – Channel loss budget (35 dB@12.8906 GHz). Link segment up to at least 5 m (22.8 dB@12.8906 GHz)
- 802.3by - 25GBASE-CR and 25GBASE-CR-S - 2-level PAM - 25.78125 GBd per lane – Channel loss budgets (35 dB, 29 dB, 28.02 dB)@12.8906 GHz . Link Segments 3-5 m (22.48 dB, 16.48 dB, 15.50 dB)@12.8906 GHz reach depending on FEC
- 802.3cd - 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4– PAM4 - 26.5625 GBd per lane – Channel loss budgets 30 dB@13.28 GHz. Link Segment up to at least 3 m reach 17.6 dB@13.28 GHz.
- 802.3ck - 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 – PAM4 - 53.125 GBd per lane – Channel loss budgets 28.5 dB@26.56 GHz. Link Segment up to at least 3 m reach 19.75 dB@26.56 GHz

Background – 802.3bj/by/cd/ck

- The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly (link segment).
- Test points provide specification references for channel and cable assembly and RX and TX
- Test fixtures enable testing at test points – module compliance board (MCB); host compliance board (HCB)



Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92-2. The cable assembly test fixture of Figure 92-17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92-6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

Background – 802.3bj/by/cd/ck

- TP0 and TP5 test point parameters and channel characteristics (802.3ck Annex 162A - (informative))
- Test fixture – module compliance board (MCB); host compliance board (HCB)

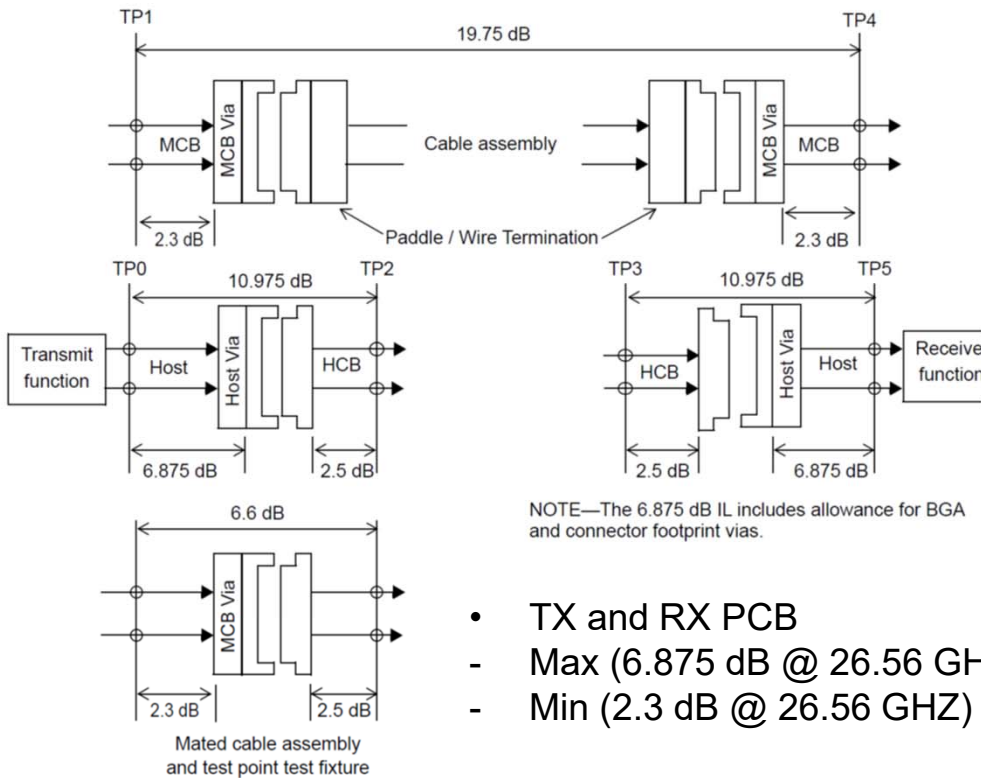


Figure 162A-3—Cable assembly, host, and test fixture insertion loss at 26.56 GHz

- TX and RX PCB
- Max (6.875 dB @ 26.56 GHz)
- Min (2.3 dB @ 26.56 GHz)

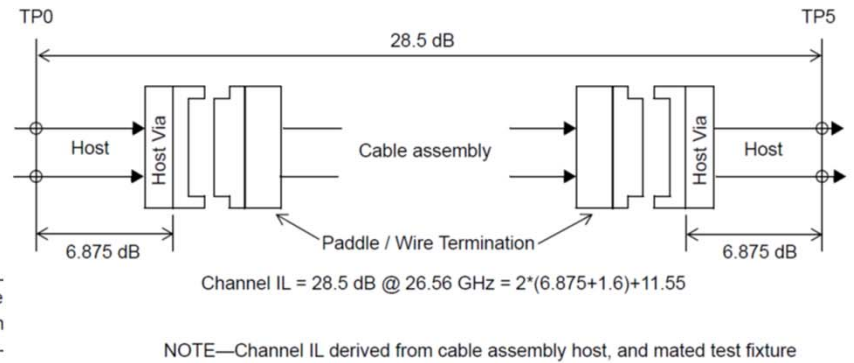


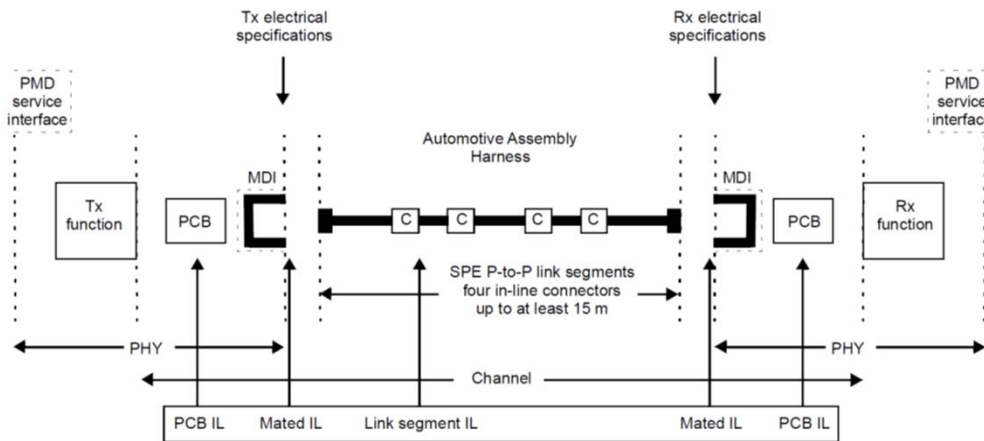
Figure 162A-4—Channel insertion loss at 26.56 GHz

Table 162A-1—Insertion loss budget values at 26.56 GHz

Parameter	Value	Units
IL_{Chmax}	28.5	dB
IL_{Camax}	19.75	dB
IL_{Chmin}	19.75	dB
IL_{Camin}	11.0	dB
$IL_{MaxHost}$	10.975	dB
$IL_{MatedTF}$	6.6	dB

Tx Function to Rx function channel considerations

IEEE Std 802.3ch-2020 - Annex 149C



149C.2 Differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are as specified in Equation (149C-1) and Equation (149C-2), respectively.

$$IL_{PCB(76.2mm)} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000} \right) \times 76.2 \text{ (dB)} \quad (149C-1)$$

$$IL_{PCB(25.4mm)} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000} \right) \times 25.4 \text{ (dB)} \quad (149C-2)$$

where

f is the frequency in MHz; $1 \leq f \leq F_{max}$

$$F_{max} = 4000 \times S \quad (149C-3)$$

See Table 149-1 for the definition of S .

149C.3 Channel insertion loss

The channel topology with the 76.2 mm PCB insertion loss is determined using Equation (149C-4), Equation (149C-5), and Equation (149C-6).

$$IL_{channel} = 2 \times IL_{PCB(76.2mm)} + 2 \times IL_{MDI} + IL_{LinkSegment} \quad (149C-4)$$

$$IL_{MDI} = 0.1 \times \sqrt{\frac{f}{1000}} \quad (149C-5)$$

$$IL_{LinkSegment} = 0.002 \times f + 0.68 \times f^{0.45} \quad (149C-6)$$

where

f is the frequency in MHz; $1 \leq f \leq F_{max}$

F_{max} is defined by Equation (149C-3)

Table 149C-1—Channel insertion loss for each PHY type

PHY	Rate MBd	Bandwidth (MHz)	$IL_{PCB(76.2mm)}$ (dB)	$IL_{LinkSegment}$ (dB)	IL_{MDI} (dB)	$IL_{channel}$ (dB)
2.5GBASE-T1	1406.25	703.125	0.6948	14.3982	0.084	15.955
5GBASE-T1	2812.5	1406.25	1.1238	20.56	0.119	23.045
10GBASE-T1	5625	2812.5	1.8717	29.8688	0.168	33.948

Tx Function to Rx function channel considerations

Annex 149C - IEEE Std 802.3ch-2020

149C.4 Channel return loss



Figure 149C-2—Tx/Rx function channel topology

149C.4.2 Link segment return loss

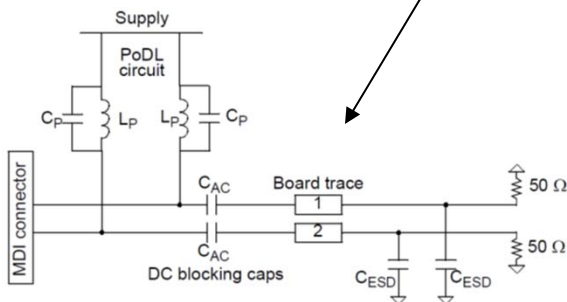


Figure 149C-3—Example implementation MDI to Tx function

$$RL = 20\log_{10}|\Gamma|$$

$$\Gamma = \frac{Z_{in} - Z_s}{Z_{in} + Z_s}$$

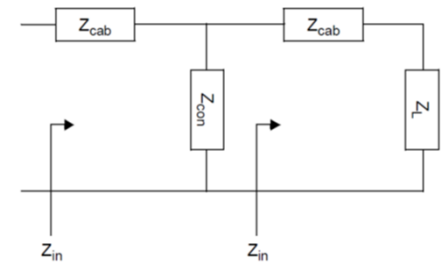


Figure 149C-5—Two-port ladder network

Table 149C-2—Analysis parameters and values

Element	Unit	Minimum	Nominal	Maximum
R_T	Ω	45	50	55
Z_O	Ω	45	50	55
C_T	pF	—	0.1	—
L_P	μH	—	4.7	—
C_P	pF	—	0.18	—
C_{ESD}	pF	—	0.4	—
C_{AC}	nF	—	10	—

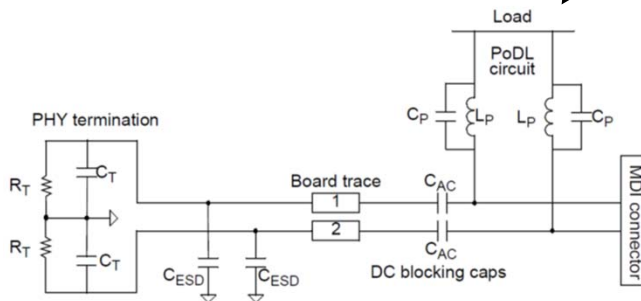


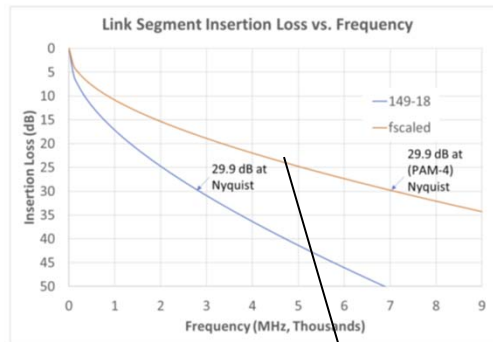
Figure 149C-4—Example implementation Rx function to MDI

Channel Insertion Loss – 802.3cy

Frequency Scaled link segment IL

$$IL \leq 0.002 \left(\frac{f}{2.5} \right) + 0.68 \left(\frac{f}{2.5} \right)^{0.45}$$

This is a starting point
Same IL at Nyquist as .3ch



https://www.ieee802.org/3/cy/public/nov20/zimmerman_3cy_01a_1120.pdf

$$IL_{Channel} \leq 2 \cdot IL_{PCB(76.2mm)} + 2 \cdot IL_{MDI} + IL_{Linksegment} \quad (\text{dB})$$

$$IL_{PCB(76.2mm)} \leq \left(0.0071 \sqrt{f/2.5 \cdot 10^3} + 0.0045 \cdot f/2.5 \cdot 10^3 \right) \cdot 76.2 \quad (\text{dB})$$

$$IL_{Linksegment} \leq 0.002 \left(\frac{f}{2.5} \right) + 0.68 \left(\frac{f}{2.5} \right)^{0.45} \quad (\text{dB})$$

$$IL_{MDI} \leq 0.1 \sqrt{\frac{f}{10^3}} \quad (\text{dB})$$

PHY	MBd	Bandwidth (MHz)	PCBILdb/76.2mm	IL Link Segment	IL MDI	IL Channel Max
2.5GBASE-T1	1406.25	703.125	0.6948	14.3982	0.084	15.955
5GBASE-T1	2812.5	1406.25	1.1238	20.5600	0.119	23.045
10GBASE-T1	5625	2812.5	1.8717	29.8688	0.168	33.948
25GBASE-T1	14062.25	7031.25	1.8717	29.8688	0.168	33.948

149C.3 Channel insertion loss

The channel topology with the 76.2 mm PCB insertion loss is determined using Equation (149C-4), Equation (149C-5), and Equation (149C-6).

$$IL_{channel} = 2 \times IL_{PCB(76.2mm)} + 2 \times IL_{MDI} + IL_{LinkSegment} \quad (149C-4)$$

$$IL_{MDI} = 0.1 \times \sqrt{\frac{f}{1000}} \quad (149C-5)$$

$$IL_{LinkSegment} = 0.002 \times f + 0.68 \times f^{0.45} \quad (149C-6)$$

where

f is the frequency in MHz; $1 \leq f \leq F_{max}$

F_{max} is defined by Equation (149C-3)

149C.2 Differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are as specified in Equation (149C-1) and Equation (149C-2), respectively.

$$IL_{PCB(76.2mm)} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000} \right) \times 76.2 \quad (\text{dB}) \quad (149C-1)$$

$$IL_{PCB(25.4mm)} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000} \right) \times 25.4 \quad (\text{dB}) \quad (149C-2)$$

where

f is the frequency in MHz; $1 \leq f \leq F_{max}$

$F_{max} = 4000 \times S$

(149C-3)

See Table 149-1 for the definition of S .

TX and RX PCB Loss

IEEE 802.3bj/by/cd

Host Tx and Rx PCB losses

- Transmitter and receiver differential printed circuit board trace loss

GHz	dB/in
1	0.1856
6.5	0.8971
7	0.9557
12.89	1.5924
14	1.702

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR - Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR - Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR - Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR - Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR - Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR - Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR - Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR - Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

*Using Algebraic Model v2.02a - see backup slides for values entered in Model

PROPOSED PARAMETERS:
GRAPHS ON PREVIOUS SLIDE

[Proposal for Defining Material Loss](#)
26-Jan 12

Elizabeth Kochuparambil
Joel Goergen

Cisco

http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

12

802.3bj Cu specifications

http://www.ieee802.org/3/bj/public/may12/diminico_01a_0512.pdf

PHY	MBd	Bandwidth (MHz)	PCBILdb/76.2mm	PCBILdb/in
25GBASE-T1	14062.25	7031.25	1.8717	0.624

IEEE 802.3cy TG

Dk Df Algebraic Model

Background

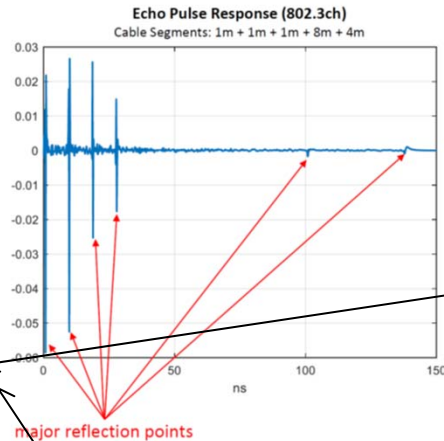
- Model first shown in Kochuparambil_01_1111
 - Filling a gap – allows us to talk the same “language”
 - Great for initial channel loss discussions!
- Model is made public:
<http://www.ieee802.org/3/bj/public/tools.html>
- No secret sauce
 - All equations used in the model are given in reference document
 - Also in public Tools folder; link above

Insertion Loss Deviation

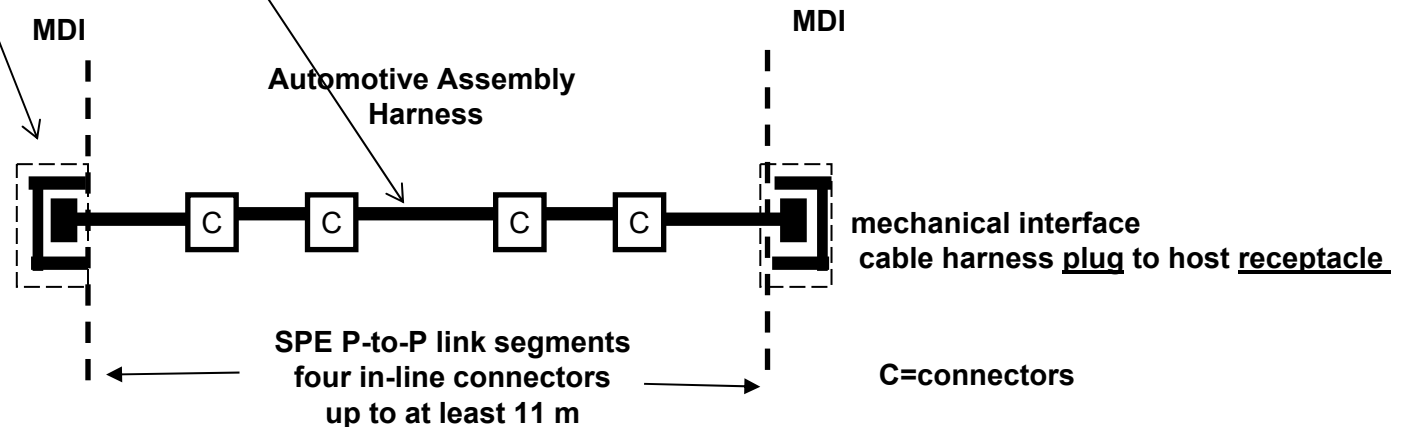
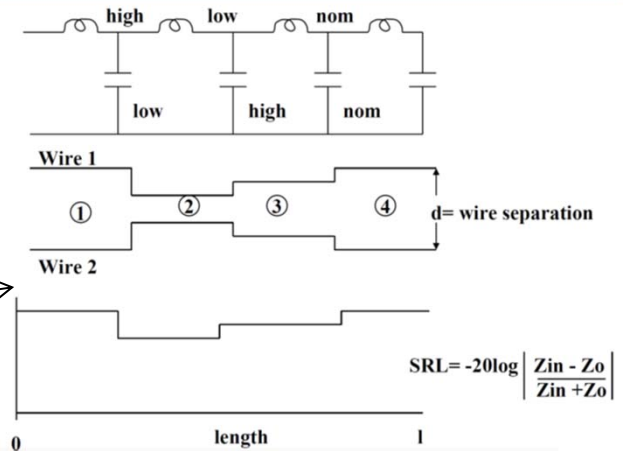
Echo Response in Time

- The echo pulse response consists of major reflections from a maximum of 6 discontinuities in the link segment
 - 2 MDI interfaces
 - No more than 4 connectors
- There are micro reflections, in between discontinuities and spread throughout the cable, due to cable inhomogeneity (nonuniform characteristic impedance)

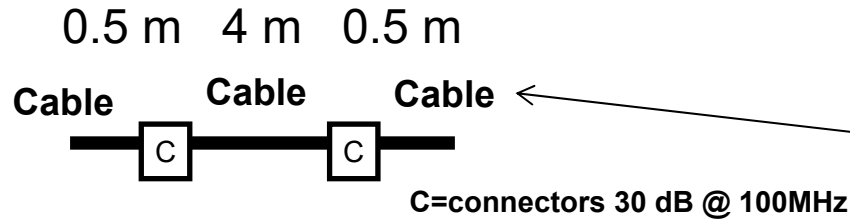
https://grouper.ieee.org/groups/802/3/cy/public/adhoc/sedarat_3cy_01_0920.pdf



Structural Return Loss (SRL) - Structural Variation Associated With Impedance Variations Of A Cable



Insertion Loss Deviation



Return loss is computed by multiplication of transmission matrices for each component (cable and connectors) in the link segment. Each component is modeled by its transmission matrix. Cable structure is added as pseudorandom impedance to asymptotic cable impedance.

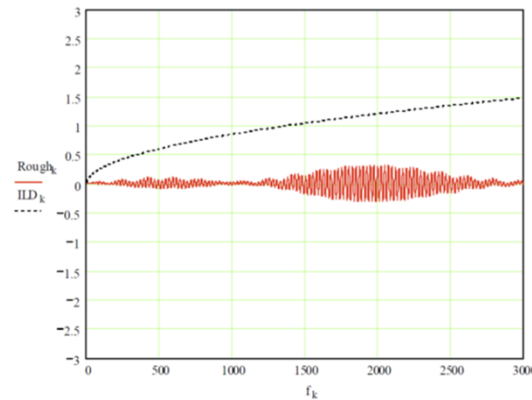
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \prod_k [T_k] \quad Z_{in} = \frac{A + \frac{B}{Z_{in}}}{C + \frac{D}{Z_{in}}} \quad RL = -20 \log \left(\frac{Z_{in} - 100}{Z_{in} + 100} \right)$$

Cable Insertion Loss Specification Scaled to Length of Channel

$$Atten_k := \frac{Att_k \cdot X_g}{100}$$

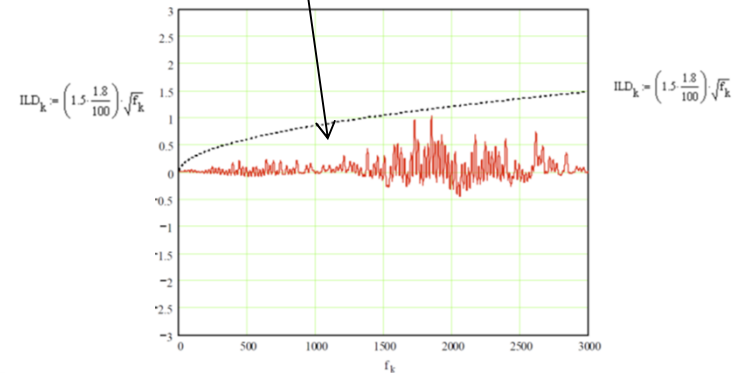
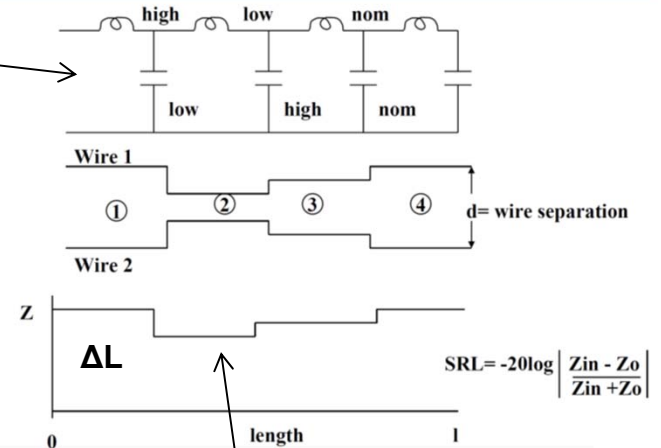
Insertion Loss Deviation Channel IL - Cable IL spec

$$Rough_k := 1 \cdot (IL_k - Atten_k)$$



cable without structure

Structural Return Loss (SRL) - Structural Variation Associated With Impedance Variations Of A Cable



cable with structure added pseudo-random Z ΔL

IEEE Std 802.3bj-2014 - FOM_{ILD}

93A.3 Fitted insertion loss

The fitted insertion loss as a function of frequency is given by Equation (93A-51).

$$IL_{fitted}(f) = a_0 + a_1\sqrt{f} + a_2f + a_4f^2 \quad (93A-51)$$

Denote the insertion loss, in dB, measured at frequency f_n as $IL(f_n)$. Given the insertion loss measured at N uniformly-spaced frequencies from start frequency f_{\min} to stop frequency f_{\max} with step no larger than Δf , the coefficients for the fitted insertion loss shall be calculated as follows.

Define the weighted frequency matrix F using Equation (93A-52).

$$F = \begin{bmatrix} 10^{-IL(f_1)/20} & \sqrt{f_1}10^{-IL(f_1)/20} & f_110^{-IL(f_1)/20} & f_1^210^{-IL(f_1)/20} \\ 10^{-IL(f_2)/20} & \sqrt{f_2}10^{-IL(f_2)/20} & f_210^{-IL(f_2)/20} & f_2^210^{-IL(f_2)/20} \\ \dots & \dots & \dots & \dots \\ 10^{-IL(f_N)/20} & \sqrt{f_N}10^{-IL(f_N)/20} & f_N10^{-IL(f_N)/20} & f_N^210^{-IL(f_N)/20} \end{bmatrix} \quad (93A-52)$$

Define the weighted insertion loss vector L using Equation (93A-53).

$$L = \begin{bmatrix} IL(f_1)10^{-IL(f_1)/20} \\ IL(f_2)10^{-IL(f_2)/20} \\ \dots \\ IL(f_N)10^{-IL(f_N)/20} \end{bmatrix} \quad (93A-53)$$

The fitted insertion loss coefficients are then given by Equation (93A-54).

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T L \quad (93A-54)$$

The values assigned to f_{\min} , f_{\max} , and Δf are defined by the Physical Layer specification that invokes this method.

93A.4 Insertion loss deviation

The insertion loss deviation $ILD(f)$ is the difference between the measured insertion loss $IL(f)$ and the fitted insertion loss $IL_{fitted}(f)$ (see 93A.3) as shown in Equation (93A-55).

$$ILD(f) = IL(f) - IL_{fitted}(f) \quad (93A-55)$$

A figure of merit for a channel that is based on $ILD(f)$ is given by Equation (93A-56). In Equation (93A-56), f_n are the frequencies considered in the computation of the fitted insertion loss and $W(f_n)$ is the weight at each frequency as defined by Equation (93A-57).

$$FOM_{ILD} = \left[\frac{1}{N} \sum_n W(f_n) ILD^2(f_n) \right]^{1/2} \quad (93A-56)$$

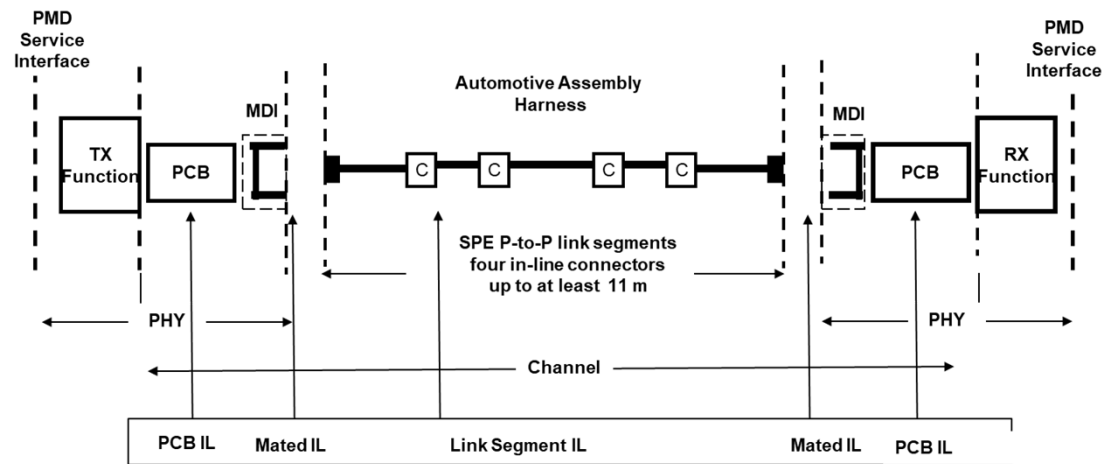
$$W(f_n) = \text{sinc}^2(f_n/f_b) \left[\frac{1}{1 + (f_n/f_t)^4} \right] \left[\frac{1}{1 + (f_n/f_r)^8} \right] \quad (93A-57)$$

The variable f_b is the signaling rate. The 3 dB transmit filter bandwidth f_t is inversely proportional to the 20% to 80% rise and fall time T_t . The constant of proportionality is 0.2365 (e.g., $T_t f_t = 0.2365$; with f_t in Hertz and T_t in seconds). The variable f_r is the 3 dB reference receiver bandwidth.

The values assigned to f_b , T_t , and f_r are defined by the Physical Layer specification that invokes this method.

Summary

- Tx Function to Rx function channel IL proposal



$$IL_{Channel} \leq 2 \cdot IL_{PCB(76.2mm)} + 2 \cdot IL_{MDI} + IL_{Linksegment} \quad (\text{dB})$$

$$IL_{PCB(76.2mm)} \leq \left(0.0071 \cdot \sqrt{f/2.5 \cdot 10^3} + 0.0045 \cdot f/2.5 \cdot 10^3 \right) \cdot 76.2 \quad (\text{dB})$$

$$IL_{Linksegment} \leq 0.002 \left(\frac{f}{2.5} \right) + 0.68 \left(\frac{f}{2.5} \right)^{0.45} \quad (\text{dB})$$

$$IL_{MDI} \leq 0.1 \sqrt{\frac{f}{2.5 \cdot 10^3}} \quad (\text{dB})$$

PHY	MBd	Bandwidth (MHz)	PCBILdb/76.2mm	IL Link Segment	IL MDI	IL Channel Max
25GBASE-T1	14062.25	7031.25	1.8717	29.8688	0.168	33.948