Modulation Evaluation

Comparison of different modulation variants

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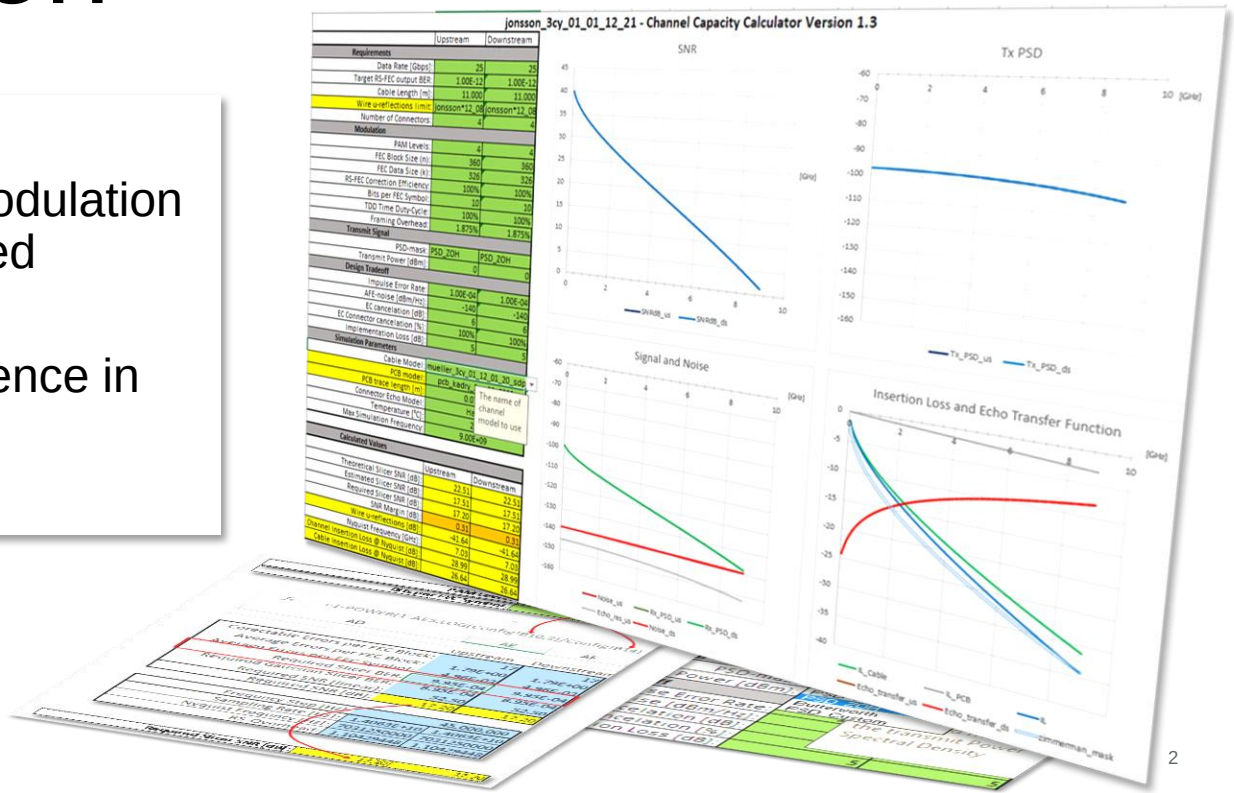
802.3cy

Introduction

- Different line-code modulation schemes are compared
- We use 802.3ch like modulation as a reference in these comparisons



Strawman Based on 802.3ch

- In the November 2020 plenary meeting we discussed proposal in zimmerman_3cy_01a_1120 to use 802.3ch as a strawman to compare other implementations against
- In this presentation we follow this approach

PHY specifications - bootstrapped

- PAM 4, 7031.25 Nyquist, 14062.5 MBaud
- PCS blocking, scramblers, state diagrams defined
- EEE modes defined
  - Q: Do we need something more for these use cases?
- RS-FEC interleaved block coding, per 802.3ch specification
  - Q: What interleave is needed for 25 Gbps rate?
- PMA electricals defined
  - E.g., 1.3Vpp output, Droop, PSD masks per frequency scaling
- Transmitter test modes defined
  - Receiver test levels need work but after link segment

What does this mean

- Consider adopting the 802.3ch specification as a “TBD” and then comparing new proposals or changes to it with a new “S” factor for 25 Gbps (S = 2.5) and a frequency-stretched link segment

- Gets us started toward a specification
- Gives something solid to compare against
- Gives us clear things to change and a clear metric to evaluate improvements
- Maximizes reuse in silicon design and standards specification

PAM Examples

- The two cases on the right were calculated using the CCC from [jonsson_3cy_01_04_20_21]
- The one on the left uses PAM4 (like 802.3ch) and the one on the right uses PAM5
- The two cases have very similar performance
- We want to evaluate the performance for different PAM modulations over different cables

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson_3cy_02	jonsson_3cy_02
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

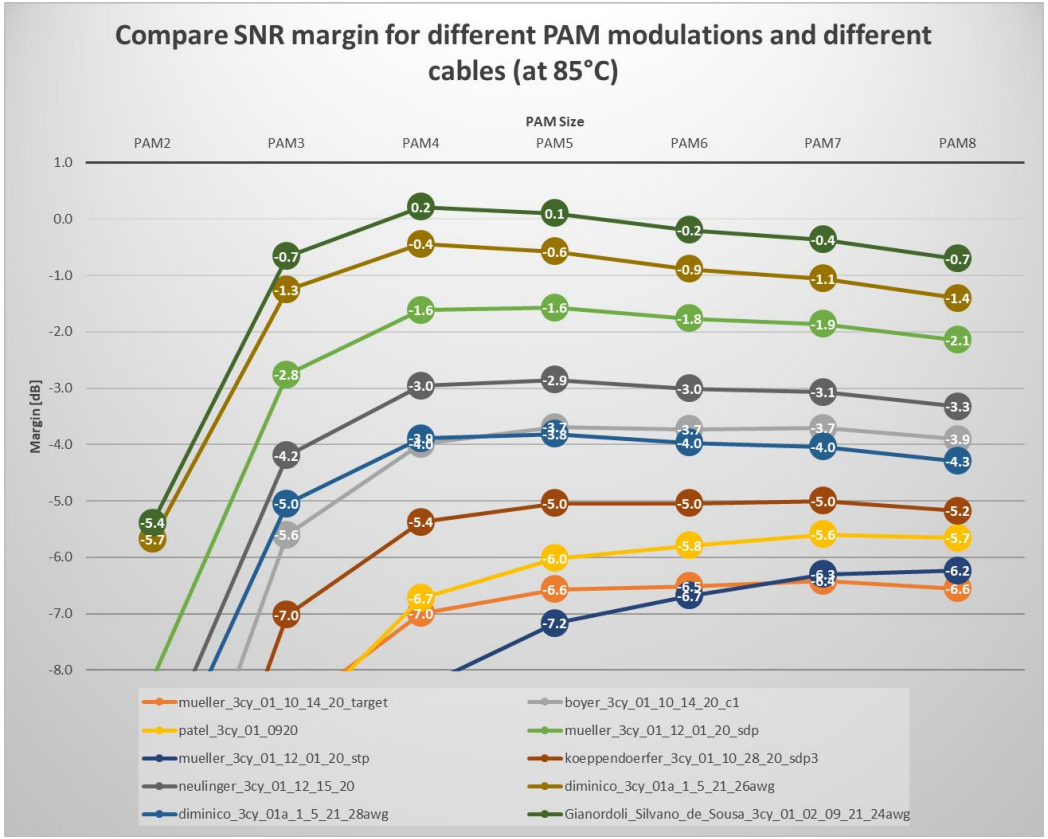
Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.00	21.00
Estimated Slicer SNR [dB]:	16.00	16.00
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	-1.20	-1.20
Wire u-reflections [dB]:	-36.68	-36.68
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	28.99	28.99
Cable Insertion Loss @ Nyquist [dB]:	26.64	26.64

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson_3cy_02	jonsson_3cy_02
Number of Connectors:	4	4
Modulation		
PAM Levels:	5	5
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	22.91	22.91
Estimated Slicer SNR [dB]:	17.91	17.91
Required Slicer SNR [dB]:	19.17	19.17
SNR Margin [dB]:	-1.26	-1.26
Wire u-reflections [dB]:	-36.68	-36.68
Nyquist Frequency [GHz]:	6.06	6.06
Channel Insertion Loss @ Nyquist [dB]:	26.24	26.24
Cable Insertion Loss @ Nyquist [dB]:	24.21	24.21

Comparing PAM Modulations

- We used calculations based on the CCC to compute the estimated cable reach for different PAM modulations
- In this comparison the FEC, implementation loss, etc. are assumed the same for all modulations
- **PAM4 is the best option for many cables and is a good option for all cables**



FEC Examples

- The two cases on the right were calculated using the CCC
- The one on the left uses 802.3ch RS-FEC
- The one on the right uses RS (750,680)
- The longer FEC code improves the SNR for this cable by 0.74dB
- We want to evaluate different RS codes for different cables

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson_3cy_02	jonsson_3cy_02
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

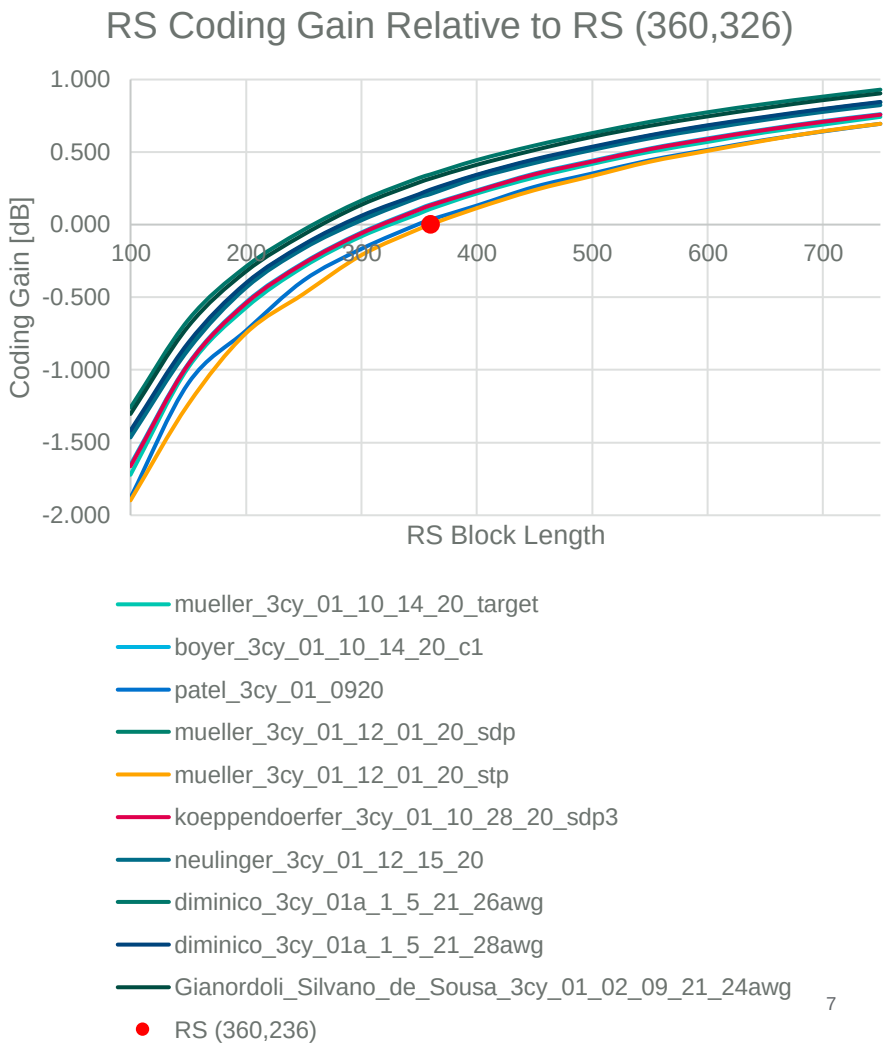
Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.00	21.00
Estimated Slicer SNR [dB]:	16.00	16.00
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	-1.20	-1.20
Wire u-reflections [dB]:	-36.68	-36.68
Nyquist Frequency [GHz]:	7.03	7.03
Channel Insertion Loss @ Nyquist [dB]:	28.99	28.99
Cable Insertion Loss @ Nyquist [dB]:	26.64	26.64

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	11.000	11.000
Wire u-reflections limit:	jonsson_3cy_02	jonsson_3cy_02
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	750	750
FEC Data Size (k):	680	680
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_sdp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	9.00E+09	

Calculated Values	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.03	21.03
Estimated Slicer SNR [dB]:	16.03	16.03
Required Slicer SNR [dB]:	16.49	16.49
SNR Margin [dB]:	-0.46	-0.46
Wire u-reflections [dB]:	-36.68	-36.68
Nyquist Frequency [GHz]:	7.02	7.02
Channel Insertion Loss @ Nyquist [dB]:	28.99	28.99
Cable Insertion Loss @ Nyquist [dB]:	26.64	26.64

Comparing FEC

- The plot shows the SNR gain from using Reed-Solomon FEC that is different from the RS (360,326) used in 802.3ch
- Longer block lengths give more coding gain
- It is possible to get additional 0.5dB to 1dB coding gain by using longer RS blocks
- Longer RS block will increase latency and increase encoding and decoding complexity



Summary

- We used 802.3ch modulation with S=2.5 as reference in our evaluation
- PAM4 is the best option for many cables and is a good option for all cables
- It is possible to improve the slicer SNR by using longer RS-FEC codes
- Using longer RS-FEC codes increases delay, complexity and power consumption of the RS encoding and decoding

Essential technology, done right™