Limit Line for Insertion Loss

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Overview

- A limit line for insertion loss is needed as a foundation to derive other specifications of the transceiver
- A summary of relevant contributions:
 - <u>kadry_081920</u>: Length-scaling of 802.ch 37 dB @ Nyquist
 - <u>sedarat_101420</u>: PHY complexity analysis 24 dB @ Nyquist
 - jonsson_111820: Capacity estimation tool
 - <u>zimmerman_111820</u>: Frequency scaling of 802.3ch 30 dB @ Nyquist
 - Many cable measurements over different lengths and types (STP, SDP)
- This presentation introduces a limit line that yields reasonable PHY operating margin considering other sources of signal loss

Outline

- A review of reported SNR margin with frequency-scaled limit of insertion loss
- A review of important factors not covered in that calculation
- A review of SNR margin considering the additional sources of loss in SNR
- Introducing a limit line that results in 0 dB margin

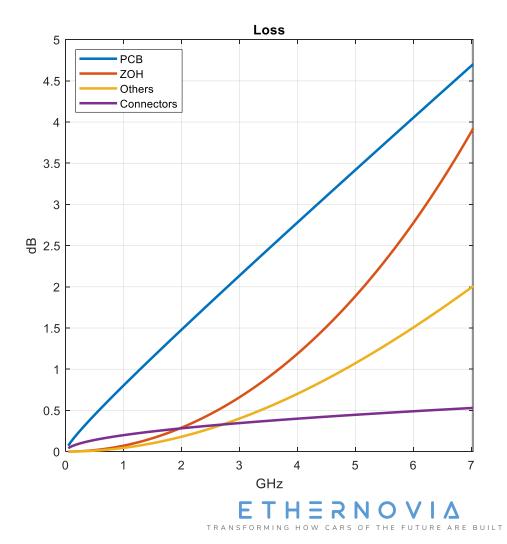
SNR with Frequency-Scaled Limit Line

- jonsson_120120 shows 2.5 dB SNR margin using an insertion loss derived from frequency scaling of 802.3ch limit
- Assumptions:
 - No sources of insertion loss other than the cable
 - Flat transmit PSD with 0 dBm power
 - No allocation of margin for EMI
 - No allocation for implementation loss

| Requrements Data Rate [Gbps]: 25 25 Target RS-FEC output BER: 1.00E-12 1E-12 Cable Length [m]: 11 11 Wire u-reflections [dB]: -40 -40 Number of Connectors: 4 4 Modulation -40 -40 Mevels: 4 4 FEC Dack Size (n): 360 360 FEC Data Size (k): 326 326 RS-FEC Correction Efficiency: 100% 100% Bits per FEC Symbol: 10 10 TDD Time Duty-Cycle: 100% 100% Framing Overhead 1.875% 1.875% Transmit Signal - 0 0 PSD-mask: PSD_brick PSD_brick Transmit Power [dBm]: 0 0 0 Design Tradeoff - 140 - EC cancelation [dB]: 5 5 5 5 5 EC Connector cancelation [%]: 100% 100% 100% | | Upstream | Downstream | | | |
|---|--------------------------------|-----------------|------------|--|--|--|
| Target RS-FEC output BER: 1.00E-12 1E-12 Cable Length [m]: 11 11 Wire u-reflections [dB]: -40 -40 Number of Connectors: 4 4 Modulation PAM Levels: 4 4 FEC Block Size (n): 360 360 FEC Data Size (k): 326 326 RS-FEC Correction Efficiency: 100% 100% Bits per FEC Symbol: 10 10 TDD Time Duty-Cycle: 100% 100% Framing Overhead 1.875% 1.875% Transmit Signal PSD-mask: PSD_brick PSD-mask: PSD_brick PSD_brick Transmit Power [dBm]: 0 0 Design Tradeoff 100E-04 0.0001 AFE-noise [dBm/Hz]: -140 -140 EC cancelation [dB]: 5 5 EC Connector cancelation [%]: 100% 100% Implementation Loss [dB]: 0 0 0 Simulation Parameters Cable Mode Zimmerman* Connector Echo Mode! Nard Calculated Values< | Requrements | 0 | | | | |
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| Wire u-reflections [dB]: -40 Number of Connectors: 4 Modulation PAM Levels: 4 FEC Block Size (n): 360 State (k): 326 RS-FEC Correction Efficiency: 100% Bits per FEC Symbol: 10 TDD Time Duty-Cycle: 100% Framing Overhead 1.875% Transmit Signal PSD-mask: PSD-mask: PSD_brick PSD-mask: PSD_brick Transmit Power [dBm]: 0 0 Design Tradeoff 0 0 Impulse Error Rate: 1.00E-04 0.0001 AFE-noise [dBm/Hz]: -140 -140 EC cancelation [dB]: 5 5 EC Connector cancelation [%]: 100% 100% Implementation Loss [dB]: 0 0 Simulation Parameters Cable Modes Zimmerman* Connector Echo Model: Nard 1 Temperature [°C] 20 0 Max Simulation Frequency: 9.00E+09 0 Max Simulation Frequency: 9.00E+09 | Target RS-FEC output BER: | 1.00E-12 | 1F-12 | | | |
| Number of Connectors: 4 4 Modulation PAM Levels: 4 4 FEC Block Size (n): 360 360 FEC Data Size (k): 326 326 RS-FEC Correction Efficiency: 100% 100% Bits per FEC Symbol: 10 10 TDD Time Duty-Cycle: 100% 100% Framing Overhead 1.875% 1.875% Transmit Signal PSD-brick PSD_brick Transmit Power [dBm]: 0 0 Design Tradeoff 0 0 Impulse Error Rate: 1.00E-04 0.0001 AFE-noise [dBm/Hz]: -140 -140 EC cancelation [dB]: 5 5 EC Connector cancelation [%]: 100% 100% Implementation Loss [dB]: 0 0 0 Simulation Parameters Cable Modes Zimmerma* Connector Echo Model: nard 1 Temperature [°C] 20 0 0 Max Simulation Frequency: 9.00E+09 | Cable Length [m]: | 11 | 11 | | | |
| Modulation PAM Levels: 4 4 FEC Block Size (n): 360 360 FEC Data Size (k): 326 326 RS-FEC Correction Efficiency: 100% 100% Bits per FEC Symbol: 10 10 TDD Time Duty-Cycle: 100% 100% Framing Overhead 1.875% 1.875% Transmit Signal V 95D_brick PSD_brick Transmit Power [dBm]: 0 0 0 Design Tradeoff V 0 0 Impulse Error Rate: 1.00E-04 0.0001 AFE-noise [dBm/Hz]: -140 -140 EC cancelation [dB]: 5 5 EC Connector cancelation [%]: 100% 100% Implementation Loss [dB]: 0 0 Simulation Parameters Cable Mode Zimmerman* Connector Echo Model: Nard 1 Temperature [°C] 20 20 Max Simulation Frequency: Max Simulation Frequency: 9.00E+09 0 | Wire u-reflections [dB]: | -40 | -40 | | | |
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| Nyquist Frequency [GHz]: 7.031 7.031 | | | | | | |
| | | | | | | |
| | Insertion Loss @ Nyquist [dB]: | | | | | |

Other Sources of Signal Loss

- Considering other sources of signal loss introduced in <u>sedarat_0820</u>:
 - Loss of PCB (<u>kadry_0820</u>)
 - Loss of MDI connectors (kadry_0820)
 - Loss of other components (1 dB on each end of the link)
- Zero order hold for transmit PSD



SNR Margin – Loss Included

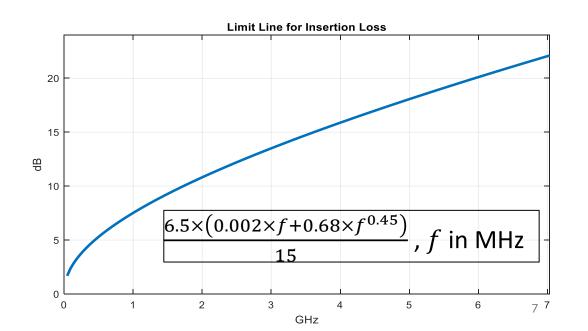
- The insertion loss from zimmerman_1120 is combined with other sources of signal loss and represented as 'column2'_
- 5 dB design margin to account for:
 - Implementation loss, RF immunity, crosstalk noise, FEC coding gain reduction, etc.
- Considering the lower limit of the transmit power of -1 dBm (802.3ch: -1 to +2 dBm)
- \rightarrow Operating margin = -5.5

| | Upstream | Downstream | | | |
|--------------------------------------|-----------------------|------------|--|--|--|
| Requrements | | | | | |
| Data Rate [Gbps]: | 25 | 25 | | | |
| Target RS-FEC output BER: | 1.00E-12 | 1.00E-12 | | | |
| Cable Length [m]: | 11 | 11 | | | |
| Wire u-reflections [dB]: | -40 | -40 | | | |
| Number of Connectors: | 4 | 4 | | | |
| Modulation | | | | | |
| PAM Levels: | 4 | 4 | | | |
| FEC Block Size (n): | 360 | 360 | | | |
| FEC Data Size (k): | 326 | 326 | | | |
| RS-FEC Correction Efficiency: | 100% | 100% | | | |
| Bits per FEC Symbol: | 10 | 10 | | | |
| TDD Time Duty-Cycle: | 100% | 100% | | | |
| Framing Overhead: | 1.875% | 1.875% | | | |
| Transmit Signal | Transmit Signal | | | | |
| PSD-mask: | PSD brick | PSD_brick | | | |
| Transmit Power [dBm]: | -1 | | | | |
| Design Tradeoff | | | | | |
| Impulse Error Rate: | 1.00E-04 | 1.00E-04 | | | |
| AFE-noise [dBm/Hz]: | -140 | -140 | | | |
| EC cancelation [dB]: | 5 | 5 | | | |
| EC Connector cancelation [%]: | 100% | 100% | | | |
| Implementation Loss [dB]: | 5 | 5 | | | |
| Simulation Parameters | Simulation Parameters | | | | |
| Cable Model: | colu | mn2 | | | |
| Connector Echo Model: | ha | ard | | | |
| Temperature [°C]: | | 0 | | | |
| Max Simulation Frequency: | 9.00 | E+09 | | | |
| | | | | | |
| Calculated Values | | | | | |
| | Upstream | Downstream | | | |
| Theoretical Slicer SNR [dB]: | 17.32 | 17.32 | | | |
| Estimated Slicer SNR [dB]: | 12.32 | 12.32 | | | |
| Required Slicer SNR [dB]: | 17 78 | 17.78 | | | |
| SNR Margin [dB]: | -5.47 | -5.47 | | | |
| Nyquist Frequency [GHz]: | 7.03 | 7.03 | | | |
| Insertion Loss @ Nyquist [dB]: | 38.45 | 38.45 | | | |
| | | | | | |

Limit on Insertion Loss

Based on 802.3ch limit line

- Frequency extended (not scaled)
- Length-scaled to 6.5 m
- → 22 dB loss at Nyquist Resulting in 0 dB operating margin



| | Upstream | Downstream |
|--------------------------------|-----------|------------|
| Requrements | | |
| Data Rate [Gbps]: | 25 | 25 |
| Target RS-FEC output BER: | 1.00E-12 | 1.00E-12 |
| Cable Length [m] | 6.54 | 6.54 |
| Wire u-reflections [dB]: | -40 | -40 |
| Number of Connectors: | 4 | 4 |
| Modulation | | |
| PAM Levels: | 4 | 4 |
| FEC Block Size (n): | 360 | 360 |
| FEC Data Size (k): | 326 | 326 |
| RS-FEC Correction Efficiency: | 100% | 100% |
| Bits per FEC Symbol: | 10 | 10 |
| TDD Time Duty-Cycle: | 100% | 100% |
| Framing Overhead: | 1.875% | 1.875% |
| Transmit Signal | - | |
| PSD-mask: | PSD_brick | PSD_brick |
| Transmit Power [dBm]: | -1 | -1 |
| Design Tradeoff | - | |
| Impulse Error Rate: | 1.00E-04 | 1.00E-04 |
| AFE-noise [dBm/Hz]: | -140 | -140 |
| EC cancelation [dB]: | 5 | 5 |
| EC Connector cancelation [%]: | 100% | 100% |
| Implementation Loss [dB]: | 5 | 5 |
| Simulation Parameters | | |
| Cable Model: | column2 | |
| Connector Echo Model: | hard | |
| Temperature [°C]: | 20 | |
| Max Simulation Frequency: | 9.00E+09 | |
| | | |
| Calculated Values | | |
| | Upstream | Downstream |
| Theoretical Slicer SNR [dB]: | 22.79 | 22.79 |
| Estimated Slicer SNR [dB]: | 17.79 | 17.79 |
| Required Slicer SNR [dB]: | | 17.78 |
| SNR Margin [dB] | 0.00 | 0.00 |
| Nyquist Frequency [GHz]: | | 7.03 |
| Insertion Loss @ Nyquist [dB]: | | 30.68 |
| | | |

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Future Considerations

- Is the reported PCB loss too conservative?
 - Better PCB material in future?
 - Shorter trace lengths?
- Is 1 dB loss for discrete components too optimistic?
- Is there room to increase the minimum transmit power?
 - Trade-offs: emission, driver linearity and power consumption, etc.
- Is 5 dB a reasonable budget for implementation loss, EMI, FEC coding gain, alien crosstalk, etc.



Cable Considerations

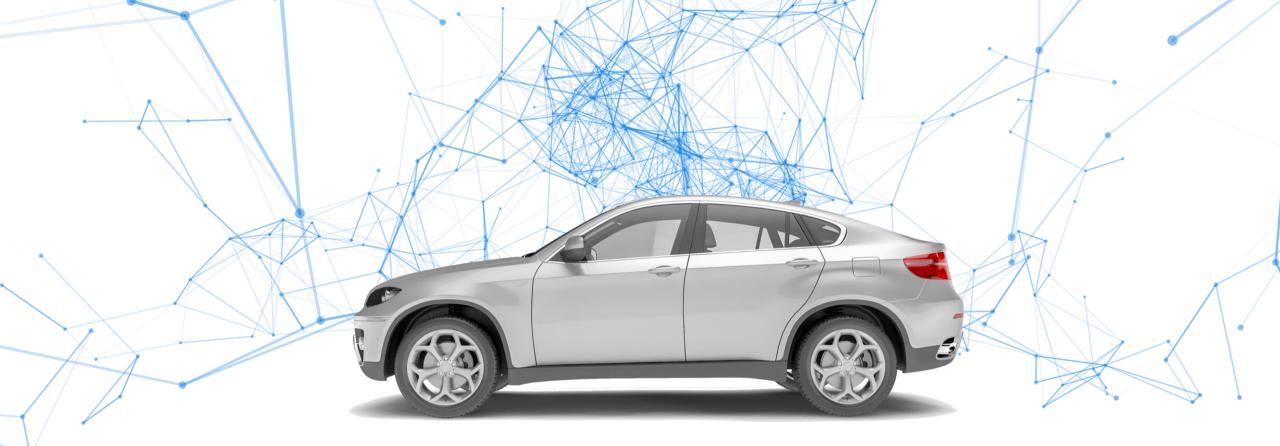
- <u>neulinger_121520</u> shows a proof of existence for a 7 m cable with inline connectors at 4 dB margin to the proposed limit
 - Need to validate across temperature and include the effects of aging
- Measurements of long cables mostly violate this limit
 - Is there better quality cables with current manufacturing technology?
 - Is there a path in future cable manufacturing to meet this limit?
 - Is the target reach of 11 m a hard requirement?
 - Is a 2-pair solution acceptable for long-reach applications?



Summary

- It is important to consider the following effects in SNR calculations:
 - Loss of PCB, MDI connectors and other discrete components
 - Zero order hold for transmit PSD
 - Lower limit of the transmit power
 - Reasonable allocation of SNR margin for implementation loss, RF immunity, crosstalk, etc.
- With these considerations, a cable with loss profile of 802.3ch length-scaled for 22 dB of loss at Nyquist results in 0 dB of operating margin





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