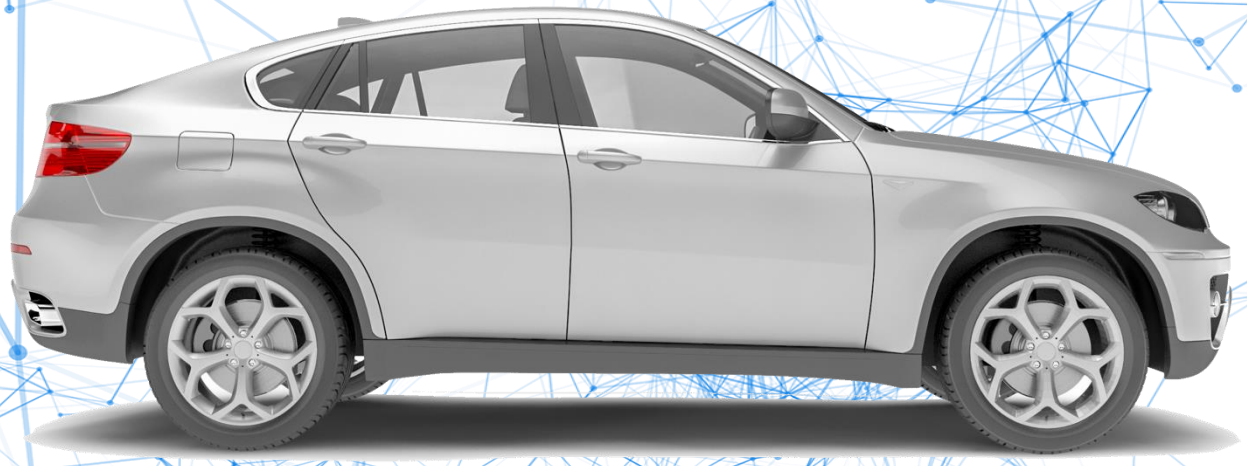

Reduced Set of PHY Design Parameters

Hossein Sedarat

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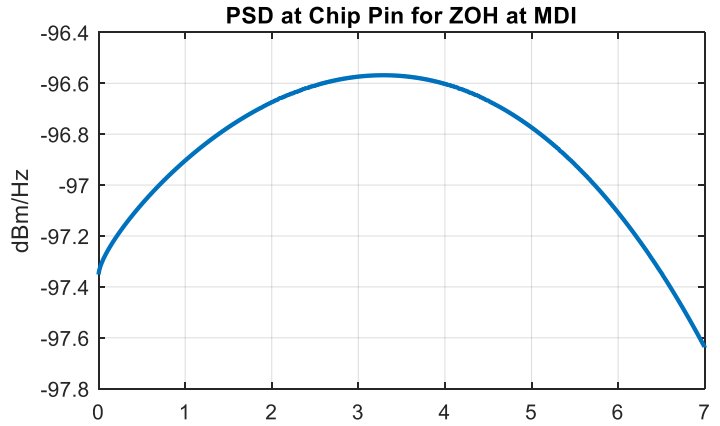
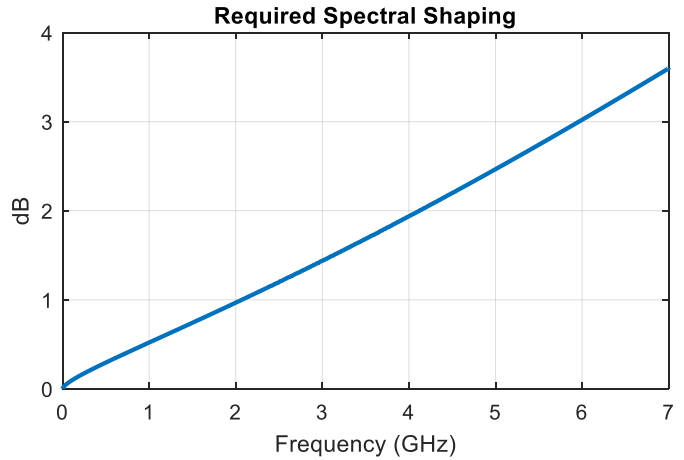
Parameters in SNR Calculations

- Transmit PSD and transmit power
- PCB loss and other sources of insertion loss
- AFE noise floor
- Residual Echo
- FEC coding gain
- Implementation loss
- Target SNR margin

Transmit PSD and Power

- 2 options have been considered for transmit PSD at MDI:
  - sedarat_010521: ZOH + (PCB+components loss) with power of -1 dBm
  - jonsson_011221: ZOH with power of 0 dBm
- A ZOH for PSD at MDI implies spectral shaping within PHY resulting in
  - A higher supply voltage to support higher peak-to-RMS ratio
    - ➔Higher power consumption
    - ➔Tougher electromigration/IR drop (EM/IR) issues
  - More high frequency content resulting in tougher requirements on
    - Mode conversion on PCB
    - Hybrid cancellation





Other Sources of Signal Loss

- Common-mode choke
- ESD protection
- AC coupling
- Chip package

AFE Noise Floor

- It should include all sources of error beyond the ones explicitly accounted for
  - Thermal noise
  - Alien crosstalk
  - Etc.
- Reasonable value?
  - -150 dBm/Hz
  - -140 dBm/Hz
  - -143 dBm/Hz

Residual Echo

- Depends heavily on the implementation of echo canceller
- What is reasonable cancellation?
  - 5 dB
  - 6 dB
  - Why not more?

FEC Coding Gain

- The FEC and interleaving is usually designed to cover for bursty impulse events
- The coding gain of FEC for Gaussian noise depends on the distribution of impulse events
  - Uniform
  - Bursty
- If FEC is designed primarily for impulse noise and it is also heavily leveraged for Gaussian noise, then can it provide coverage for EMI as well?

Implementation Loss

- It covers for non-idealities and non-Gaussian noise sources
  - Limited equalization
  - Limited echo cancellation
  - Nonlinearities
  - Sampling phase dependencies
  - Transmit power imbalance
  - Fast transient response (vibrations, cable bending, onset of EMI, etc.)

- Every designer uses a unique allocation for implementation loss

Reduced Set of Parameters

- Eliminate:
  - Level of echo cancellation
  - FEC coding gain
  - Implementation loss
- Agree on:
  - Loss from MDI to chip pin (PCB + components + package + etc.)
  - Transmit PSD and transmit power at MDI
  - An additive input-referred noise floor that captures all sources of error (AFE, residual echo, implementation loss, nonlinearities, EMI, crosstalk, etc.) and adjusted for perceived coding gain and target SNR margin
- Consider 0 dB operating margin as the pass/fail threshold

Differences to Reconcile

	sedarat	jonsson	**Difference is due to**
C2M Loss: Loss from Chip to MDI (dB at Nyquist)	3.5	2.5	Loss from components on board
Transmit power (dBm)	-1	0	Minimum vs typical transmit power
Transmit PSD (shape)	ZOH+C2M	ZOH	
Equivalent input noise floor (dBm/Hz)	-136	-137.5	Allocation of coding gain to Gaussian noise

THANK YOU

ETHERNOVIA | hossein.sedarat@ethernovia.com