802.3cy FEC Considerations

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Overview

- Reed-Solomon FEC was adopted for 802.3cy in September 2021
  - https://www.ieee802.org/3/cy/public/sep21/motions_3cy_0921.pdf Motion #3
  - https://www.ieee802.org/3/cy/public/sep21/jonsson_etal_3cy_01a_09_21_21.pdf Page 5
  - The RS-FEC block size may need to be changed to something other than (360,326)
  - The L (interleaving depth) values for 25G are 1 and TBD, up to four choices

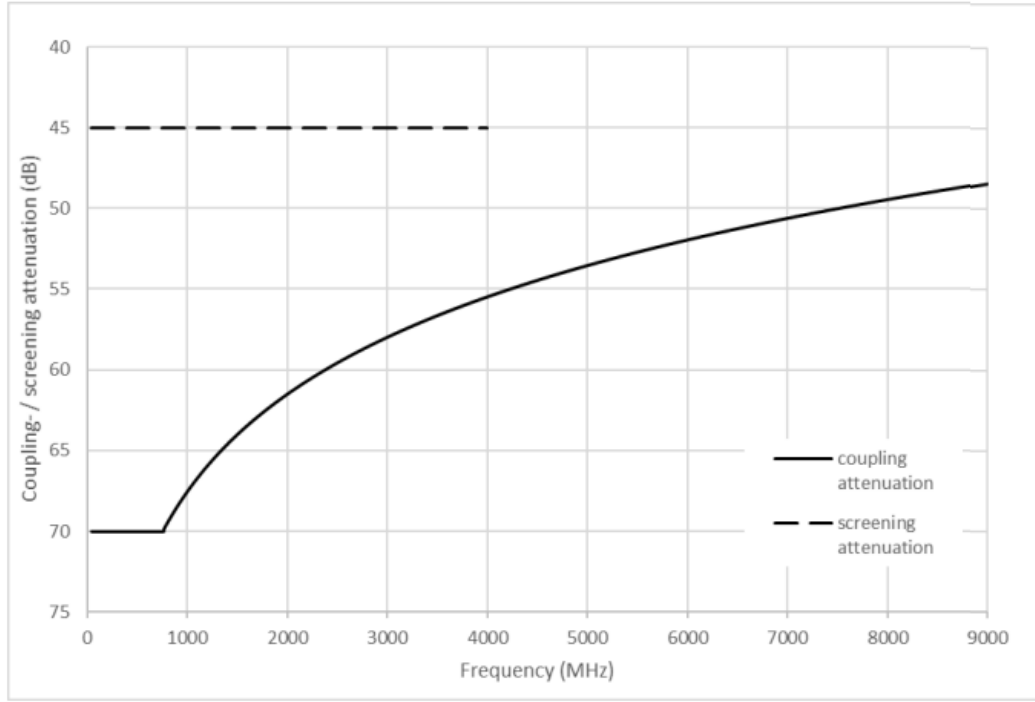
- 802.3cy FEC related contributions
  - https://www.ieee802.org/3/cy/public/adhoc/zimmerman_3cy_01_08_10_21.pdf
  - https://www.ieee802.org/3/cy/public/nov21/jonsson_3cy_01_11_09_21.pdf
  - https://www.ieee802.org/3/cy/public/nov21/tingting_3cy_01a_11_16_21.pdf

Key Design Considerations

- Error protection capability
- Latency
- PCS encoding
- PAM2 training frame
- EEE LPI Quiet/Refresh cycle
- Coding gain
- Implementation complexity

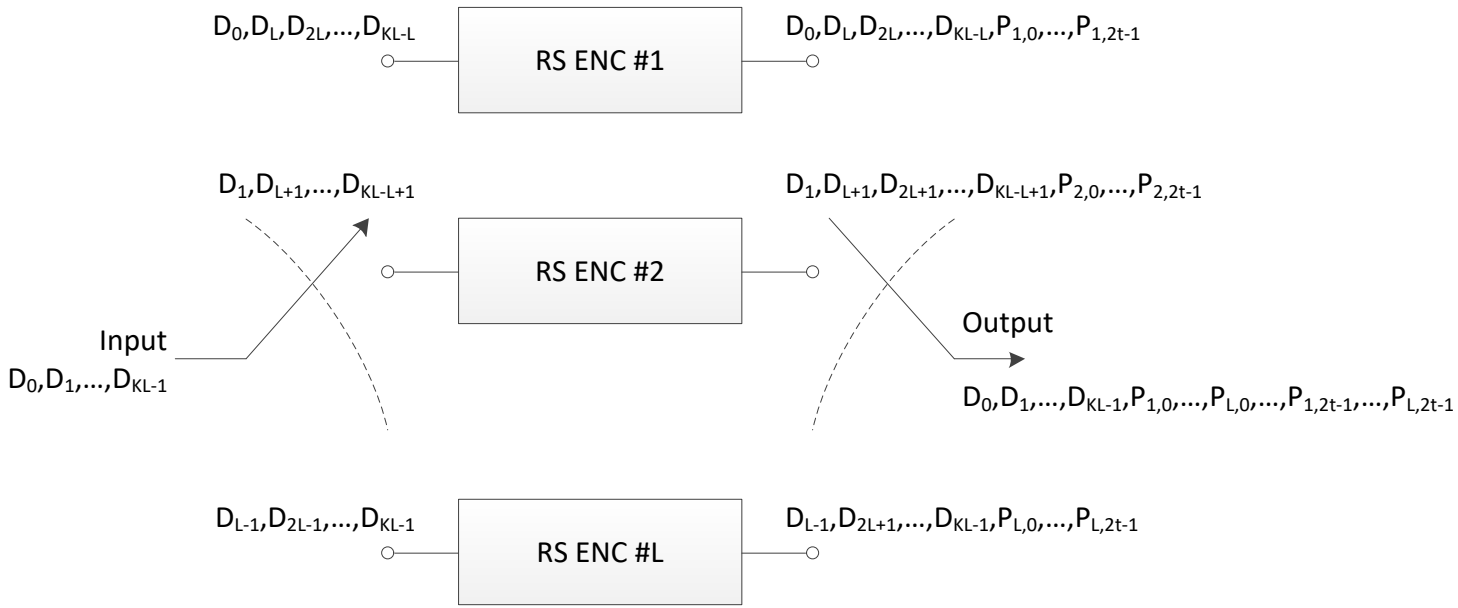
Error Protection Capability

- 60nsec burst error protection was selected for 802.3ch
- 802.3cy and 802.3ch link segment share similar characteristics
  - Screening and coupling attenuation
    - https://www.ieee802.org/3/cy/public/sep21/mueller_3cy_01_09_28_21.pdf
  - IL and RL
    - https://www.ieee802.org/3/cy/public/jul21/diminico_kadry_3cy_01_06_22_21.pdf
    - https://www.ieee802.org/3/cy/public/jul21/CuestaDiBiasoMuller_3cy_01_06_22_21.pdf
- Target >= 60nsec burst error protection for 802.3cy is a reasonable choice



Latency

- Intrinsic latency = L * FEC frame duration * (1 + (N-K)/N)
  - L = interleaving depth
  - N = # symbols per FEC codeword
  - K = # data symbols
- For 10GBASE-T1, this number is 1.404 usec with L=4 interleaving
  - If we target 60nsec burst error protection, the intrinsic latency will be in the same range



PCS Encoding

- PCS + FEC overhead = 12.5%
- PCS encoding options: 64B/65B, 128B/129B, 256B/257B, 512B/513B
- Rule of thumb
  - Must contain integer number of PCS blocks per RS FEC frames
  - Simple clock multiplier ratios for easier implementation
  - http://www.ieee802.org/3/ch/public/may18/McClellan_3ch_01a_0518.pdf
  - http://www.ieee802.org/3/ch/public/adhoc/farjarad_3chah_01b_061218.pdf
  - https://www.ieee802.org/3/ch/public/sep18/tu_3ch_01a_0918.pdf
  - https://www.ieee802.org/3/cy/public/nov21/tingting_3cy_01a_11_16_21.pdf
- Many options available that can meet burst error protection target
- Recommend to stay with 64B/65B to leverage existing 802.3ch standard

PAM2 Training Frame

- Each training frame consists of InfoField and alignment markers.
- The PAM2 training frame boundary should be aligned with data mode RS FEC boundary.
- For 802.3ch, each training frame is 1.28usec
- Keep 802.3cy training frame between 1~2usec
  - Sufficient response time for InfoField Exchange
  - Meet 100msec startup requirement

EEE LPI Quiet/Refresh Cycle

- For 802.3ch, 1 LPI cycle = 96 RS FEC frames = 30.72usec
- Receiver got updated via REFRESH (1 RS FEC frame length=320nsec) per cycle

- For 802.3cy:
- Keep overall LPI Quiet/Refresh cycle duration in similar range
- Keep sufficient REFRESH length for receiver to adapt properly

Coding Gain

- Additional coding gain preferred for 25GBASE-T1
- Noise floor likely higher vs. 10GBASE-T1
  - https://www.ieee802.org/3/cy/public/adhoc/feyh_3cy_01_09_07_21.pdf
- Additional 0.75dB coding gain available with RS (750,680)
  - https://www.ieee802.org/3/cy/public/adhoc/jonsson_3cy_01_08_03_21.pdf
- Simulation PAM4 AWGN @ 1e-12 BER
  - RS(360,326,m=10) baseline
  - RS(432,390,m=10) : 0.22dB coding gain
  - RS(864,780,m=10) : 0.74dB coding gain
- Expect 0.5~0.8dB AWGN coding gain vs. RS(360,326,m=10)
- Additional FEC coding gain should help relax (a bit) DSP/AFE requirement

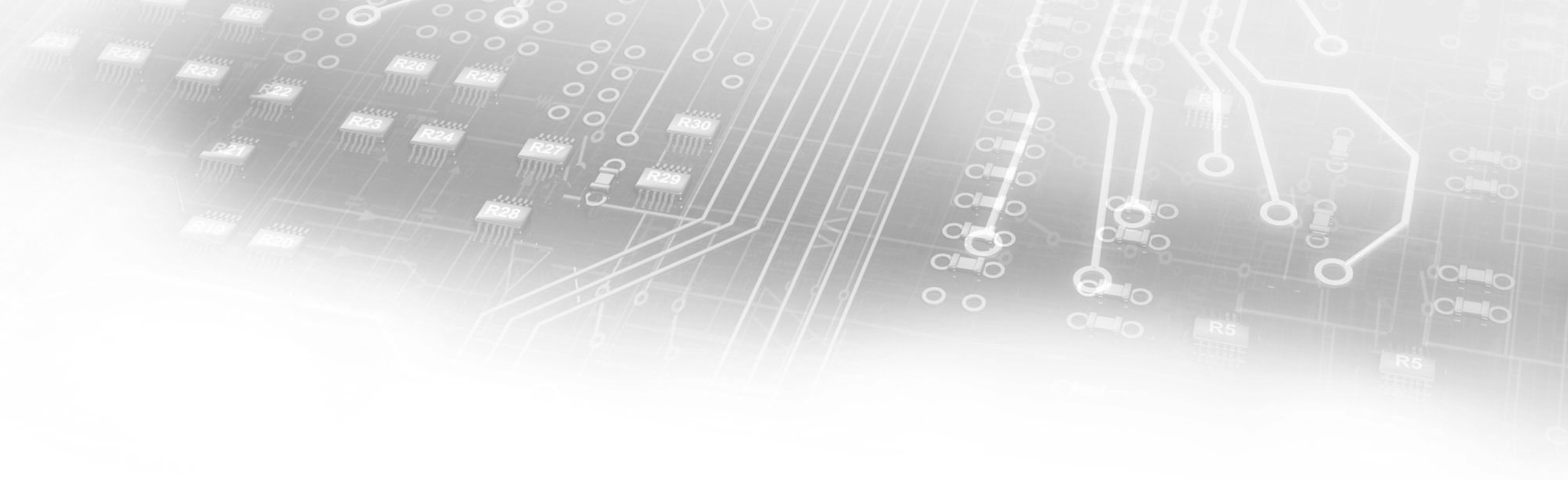
Implementation Complexity

m bits/symbol	N	K	L	Area Estimate
10	360	326	10	1x
10	648	586	6	1.7x
10	720	652	5	1.8x
10	936	846	4	2.1x
12	792	716	4	2.2x

- RS FEC area and power are minor compared to the rest of PHY receiver

FEC Candidates Based on 64B/65B PCS Encoding

# PCS blocks	m	RS N	RS K data	# oam	RS K	FEC frame nsec	L	latency nsec	total err protect nsec
50	10	360	325	1	326	128.00	10	1404.44	60.44
70	10	504	455	1	456	179.20	8	1572.98	68.27
90	10	648	585	1	586	230.40	6	1516.80	66.13
100	10	720	650	2	652	256.00	5	1404.44	60.44
130	10	936	845	1	846	332.80	4	1460.62	64.00
132	12	792	715	1	716	337.92	4	1483.09	64.85



THANK YOU

IEEE 802.3cy Task Force