

# Laning Split for PMA Reuse

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# Advantages of focus (from before)

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- Focuses link segment analysis on a single target link segment
- Focuses PHY modulation, line coding, receiver performance specifications on a single target transmitter/receiver
- Minimizes possible bleeding edge high-frequency work (especially at 100G)
- Allows design reuse of 25 Gbps PMA on early, less-common higher speed links

# “How to lane”?

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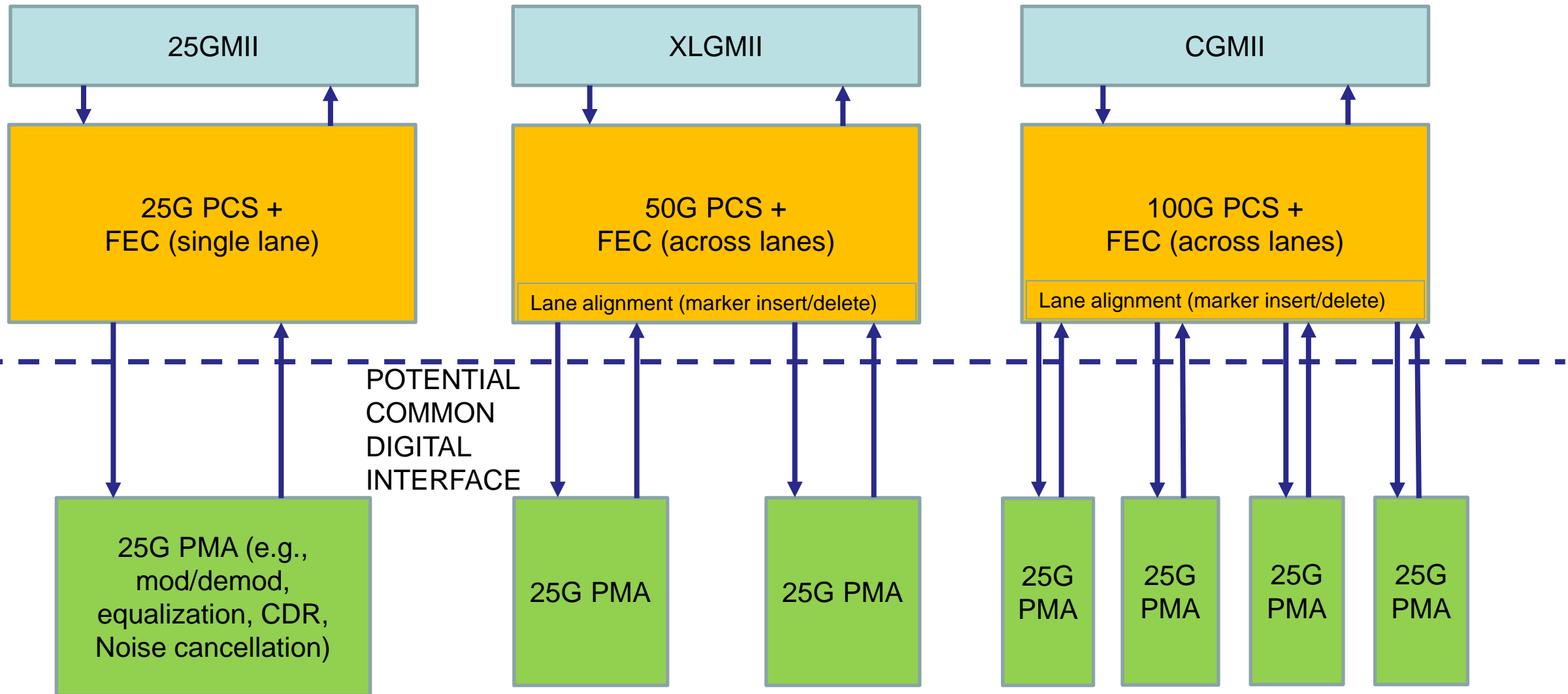
- Several choices:
  - Lane PMA only as a unit? (combine at FEC) (like CI 55)
    - Similar to BASE-T model, although FEC isn't separate sublayer
  - Lane PMA & FEC as a unit? (combine at PCS) (like CI 91 & 94)
    - Allows integration and repetition of a PMA/FEC with independent BER
  - Lane PMA/FEC/PCS as a unit? (combine at RS) (CI 143)
    - Allows independent PHY units to be bonded
    - PCS & FEC can still be internally laned if needed, independent of PMA

# Basic Functional Splits

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- PCS
  - Encode xMII commands and data into blocks for transmission (e.g., 64B/65B)
  - Lane separation, alignment, and combination
- FEC
  - Encoding/Decoding for Error correction and detection
- Bit grouping for PMA symbols traditionally in PCS, actually in PMA
- PMA
  - Modulation/precoding – translation of code groups to pulse levels, generating waveform to transmit
  - Demodulation/equalization – conversion of received analog waveforms to bit groups
  - Noise cancellation & filtering – echo cancellation, crosstalk or EMI cancellation
  - A/D, D/A conversion, Clock generation/recovery, Pulse shape, filtering

# Lane PMA Only



# Pros/Cons – Lane PMA

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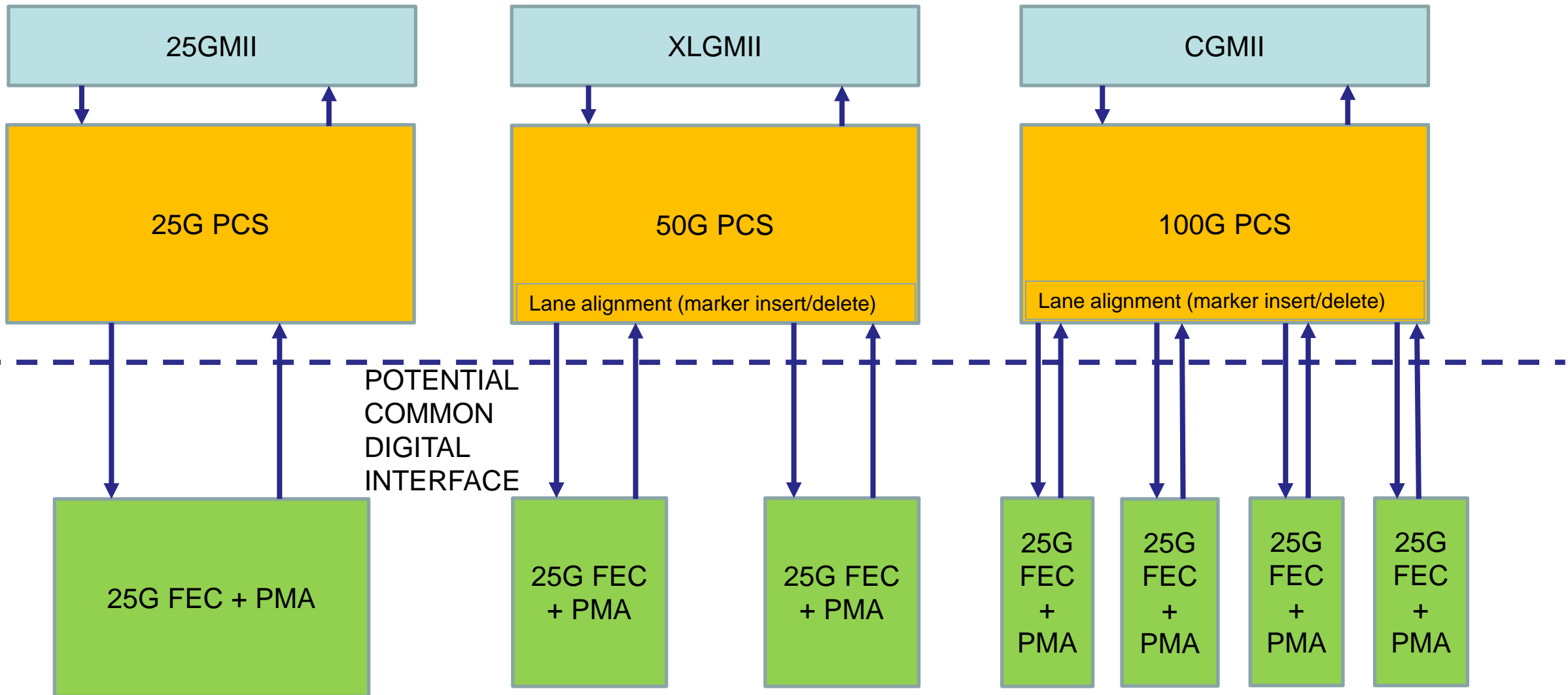
## PRO

- Allows coding across pairs
  - Better uncorrelated noise protection
- Separates design at traditional PCS/PMA boundary
  - Natural specification of common digital interface
- Potentially smallest “PHY” silicon
- FEC and PCS may be combined
- Potential for clean, standard digital interface for all 25G PHY units

## CON

- May require lane alignment prior to FEC decoding
- Requires code block length (with any interleaving) to scale as rate
- Speed-dependent FEC & PCS
- PMA operation cannot rely on PCS & FEC specifications
  - Must be robust to noise impacts
- Potential misalignment between FEC and PMA bit groups
- Even 25G PHY exists in 2 parts

# Lane PMA + FEC



# Pros/Cons – Lane PMA + FEC

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## PRO

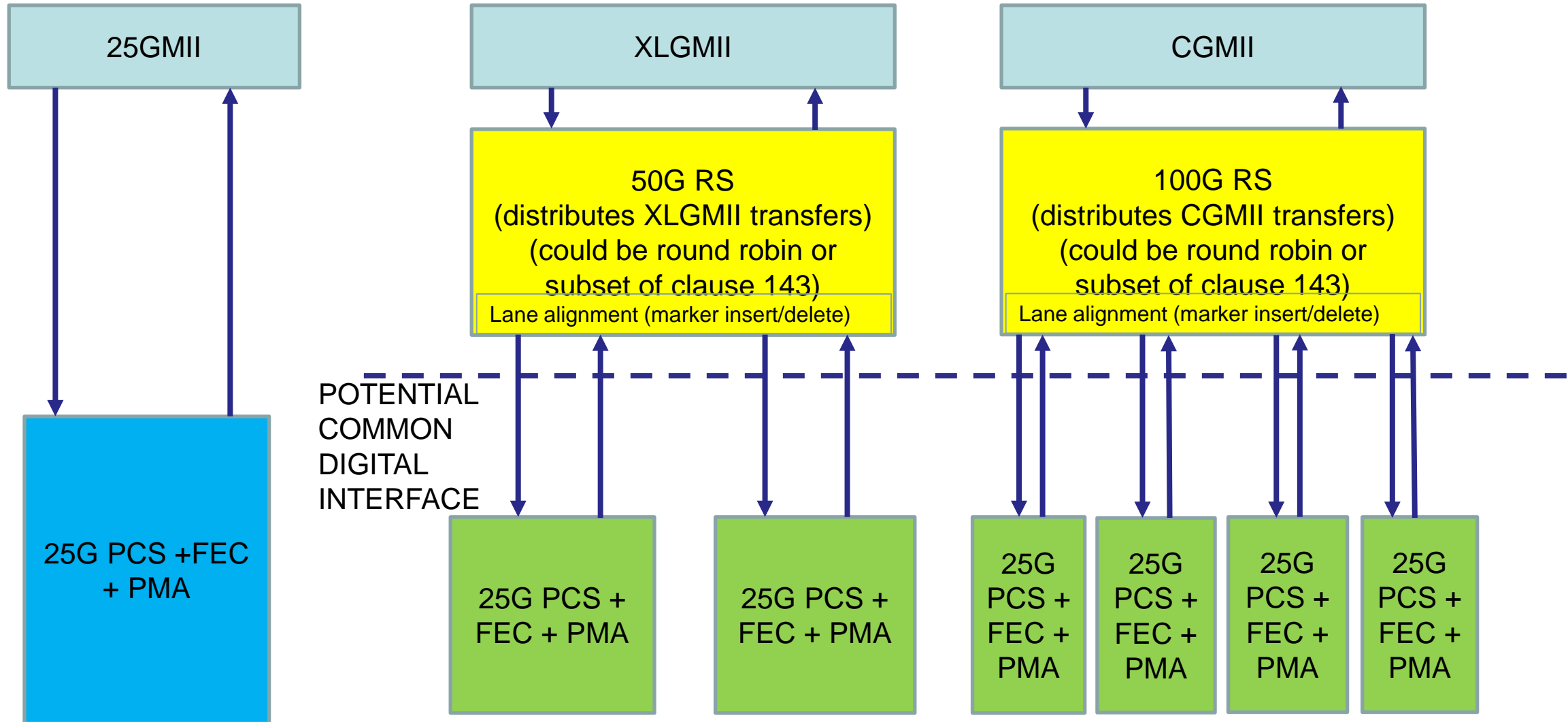
- PMA subunit gets benefit of FEC
- FEC block length independent of laning without interleaving
- PMA can benefit from FEC operation/decoding statistics
- Lower rate, Speed-independent FEC
- Cleaner tie between FEC bit grouping and PMA bit grouping
- Potential for clean, standard digital interface for all 25G PHY units

## CON

- No benefit from decorrelation of noise on other pairs
- Hard to do crosstalk cancellation
- Speed-dependent PCS
- FEC must be below PCS in layering, cannot be above or combined
- Even 25G PHY exists in 2 parts



# Lane PMA + FEC + PCS



# Pros/Cons – Lane PMA + FEC + PCS

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## PRO

- Full 25G PHY as atomic unit
- Shared digital interface only needed on higher speeds
- Full PHY bit error protection on subunit
- Single-speed FEC & PCS
- All processing at 25G rate
- Easier subunit test, most modular
- Maximum 25G reuse

## CON

- Largest “PHY” unit
- Need to define RS to do laning
  - Can borrow from existing clauses
- 25G PHY likely has a different interface to other chips/blocks than blocks used for other lanes

# Discussion

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- Recommendations?
  - My preference is PMA + FEC
    - Good balance of PHY silicon vs. integrated in controller/switch
    - Enables a reusable, clean digital interface
    - Enables robust PHY design delivering predictable bit-level performance
  - Reasonable minds may differ...

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**THANK YOU!**