# Test Points to Control Board Losses

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# Some realism

- Traditionally in BASE-T/T1, PCB losses are low compared to cable losses

- In 802.3ch we made some informative statements about PCB losses

- 802.3cy is a bit more like high-speed direct attach interfaces than standard BASE-T
  - Limited distances and good media permit GHz signaling
  - High speeds limit DSP equalization and TX power
  - High frequencies make PCB loss significant
  - Need to balance out pre-MDI losses in the budget

# MDI vs. TP

- MDI defines a point where there is a connector to a medium

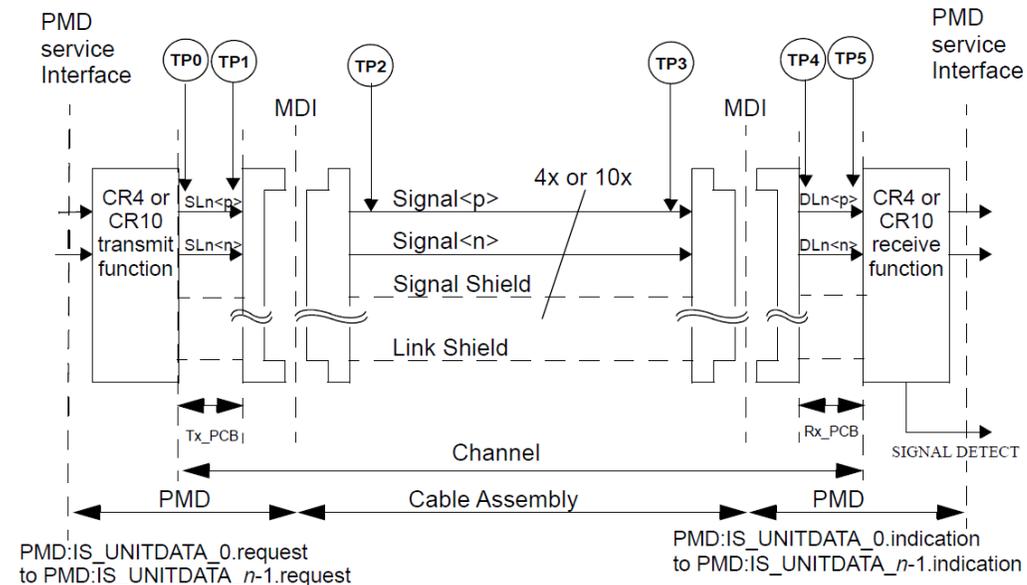- Backplane and high-speed links needed on-board references
  - Enter the Test Point



Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

# What is defined

**Table 85–4—40GBASE-CR4 and 100GBASE-CR10 test points**

| Test points | Description |
|---|---|
| TP0 to TP5 | The 40GBASE-CR4 and 100GBASE-CR10 channels including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss. |
| TP1 to TP4 | All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. The cable assembly test fixture of Figure 85–14 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4. |
| TP0 to TP1 TP4 to TP5 | A mated connector pair has been included in both the transmitter and receiver specifications defined in 85.8.3 and 85.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 85.8.3.4. |
| TP2 | Unless specified otherwise, all transmitter measurements and tests defined in Table 85–5 are made at TP2 utilizing the test fixture specified in 85.8.3.5. |
| TP3 | Unless specified otherwise, all receiver measurements and tests defined in 85.8.4 are made at TP3 utilizing the test fixture specified in 85.8.3.5. |
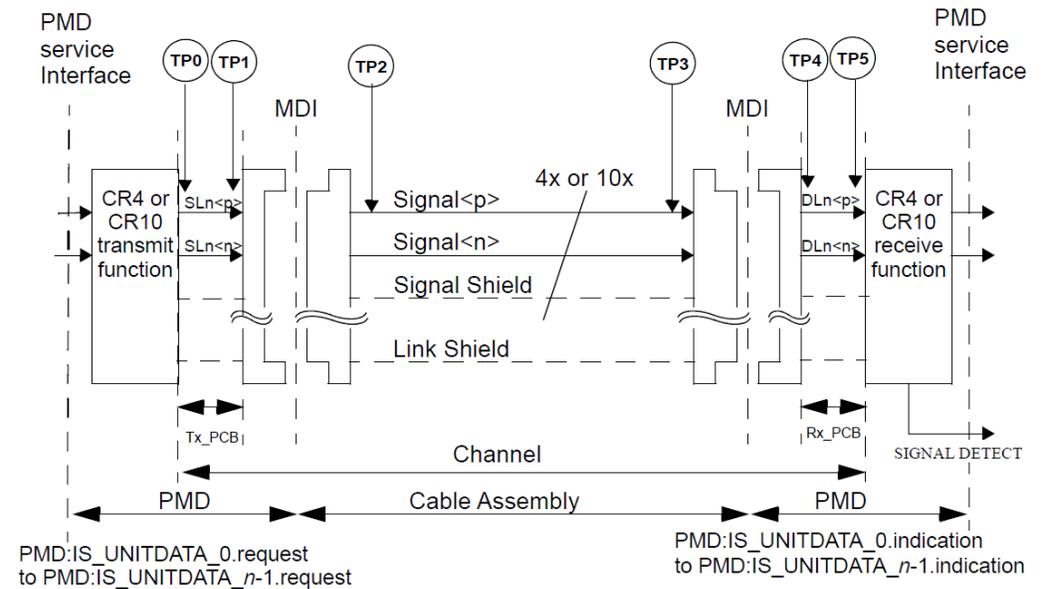


**Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)**

# What do we need to add?

- Definitely: Chip to MDI connector (PCB trace):
  - Significant contributor to loss (Kadry_3cy_02_0820.pdf )
  - TP0 to TP1 (Transmit ball to PCB-to-MDI interface)
  - TP4 to TP5 (MDI-to-PCB interface to Receive ball)
  - These should be symmetric for symmetric transmission
    - Budgets may be asymmetric for asymmetric transmission
    - Can be designed application-specific

# Dealing with the connector

- Currently we split the link segment at the MDI plane
  - This is halfway between TP1 and TP2, TP3 and TP4
  - High-speed specs call this a "Cable Assembly" (see e.g., 85.10 or 136.11)
  - Tested with special test fixtures
- DECIDING QUESTION: How significant are MDI connector losses?
  - Need contributions on whether these are significant
  - If so, then we'll need to go the next step and define TP2 and TP3
    - AND the "cable assembly" and test fixture
    - RESULT: "link segment" and the importance of MDI goes away
    - Measurements happen at the TPs

# Measuring the test points

- Involves separate measurements of host and channel
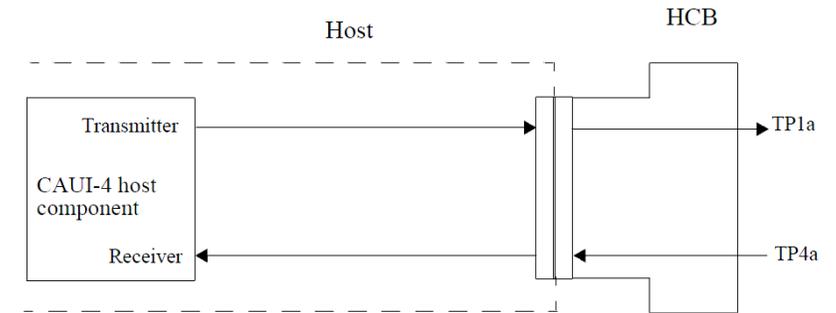
- 9/2/2



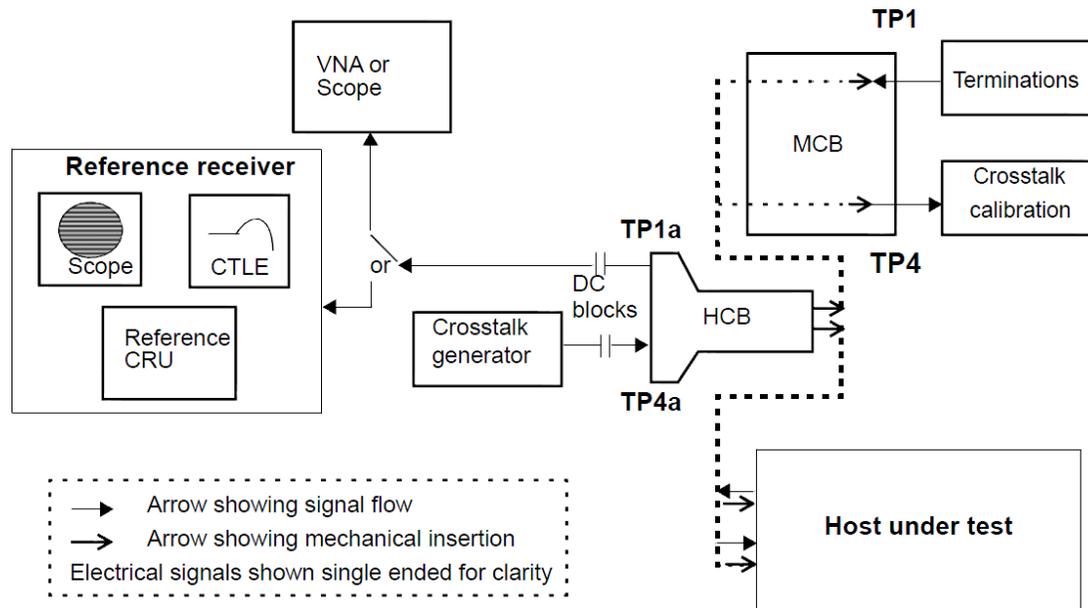Figure 83E–4—Host CAUI-4 compliance points



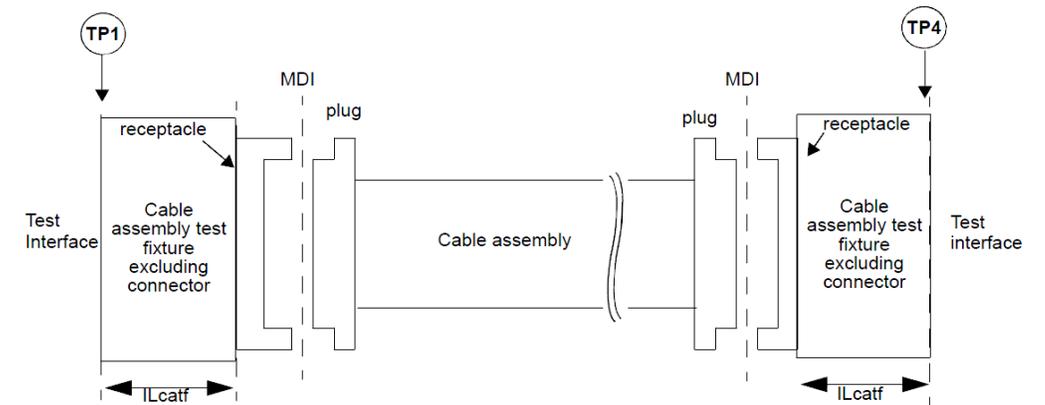Figure 83E–9—Example host output test configuration



Figure 92–17—Cable assembly test fixtures

$$IL_{catf}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \quad \text{(dB)} \qquad (92\text{–}35)$$

for $0.01 \text{ GHz} \leq f \leq 25 \text{ GHz}$

where

$f$      is the frequency in GHz

$IL_{catf}(f)$      is the reference test fixture printed circuit board insertion loss at frequency $f$

# Key Questions to Answer/ Get Consensus On

- WHAT LOSS to allocate for the PCB (TP0/TP1 and TP3/TP4)
- DOES THE MDI loss (half the connector) matter?
  - NEED MEASUREMENTS!
  - If not, life gets WAY easier
    - 802.3cy needs to specify at least a maximum connector Insertion Loss and Noise Component, and minimum Return Loss, but not more test points
  - If yes, then we need to specify more test points and fixtures
- CAN 802.3cy select a single MDI connector (even for test?)
  - To date, that answer has been NO in Automotive.
  - If it stays "NO", life gets WAY harder
  - If 802.3cy can select a connector, we can define cable qualification and board qualification from existing methodologies