Enhancing Robustness of Link Synchronization in Automotive Ethernet at 802.3cy-Part III

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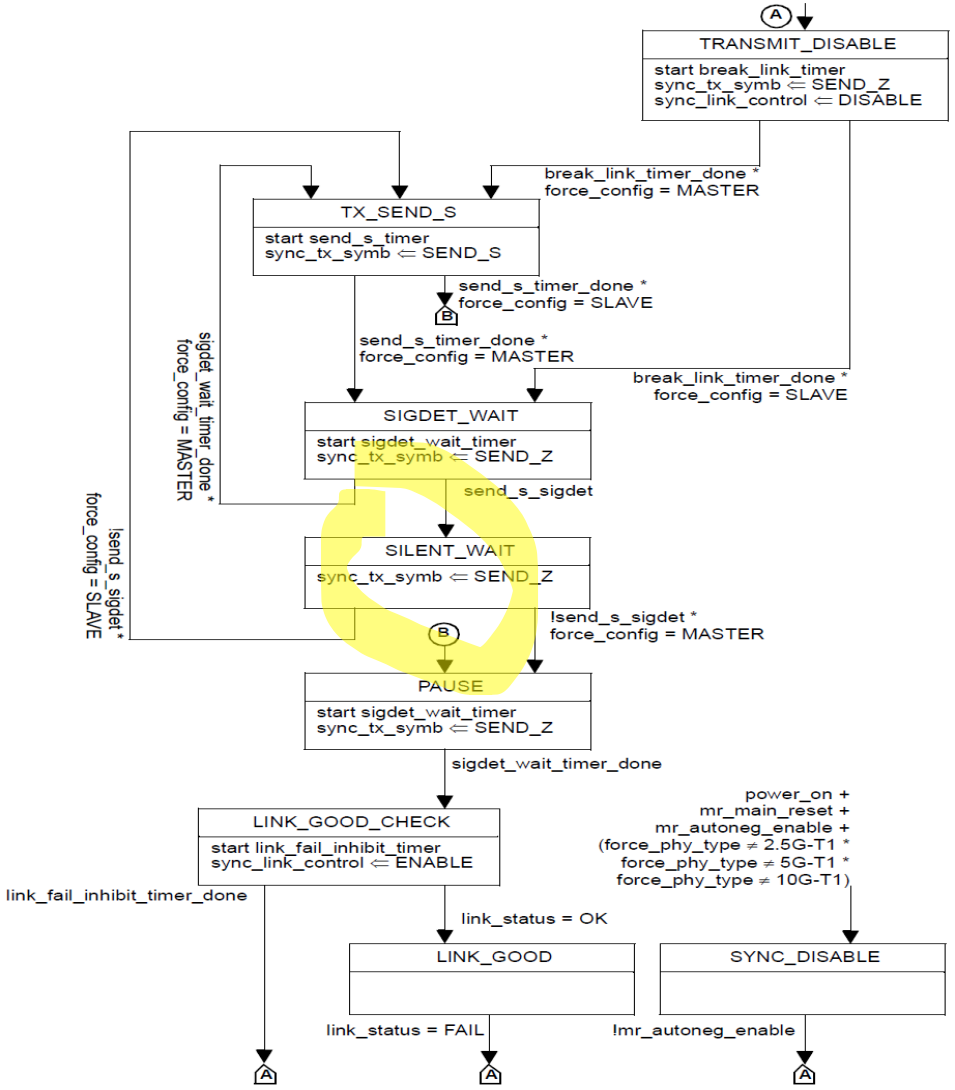
Introduction

- Link synchronization - SEND_S Signal is used by the MASTER and SLAVE to discover the link partner, and synchronize the start of PMA training
- Modifications have been proposed for 802.3cy in
  - wu_3cy_01_1121.pdf
  - wu_3cy_01_0122.pdf
- A possible issue is found during the review at the state diagram
  - possible overlap of MASTER/SLAVE send_s frames
  - silent_wait_timer is proposed to be added avoid Master/SLAVE frame overlapping

Link Synchronization in Existing Spec

- In current IEEE 802.3bp and IEEE 802.3ch specifications, device configured in master mode will continuously transmit SEND_S frames until it detect and receive a SEND_S frame response from slave mode device
- For slave mode device, once it enter SIGDET_WAIT state it will remain in this state and wait for SEND_S from master.
- Once the Frame detected, it will move to TX_SEND_S to send a single SEND_S frame and move to PAUSE state, marking Link Synchronization completion

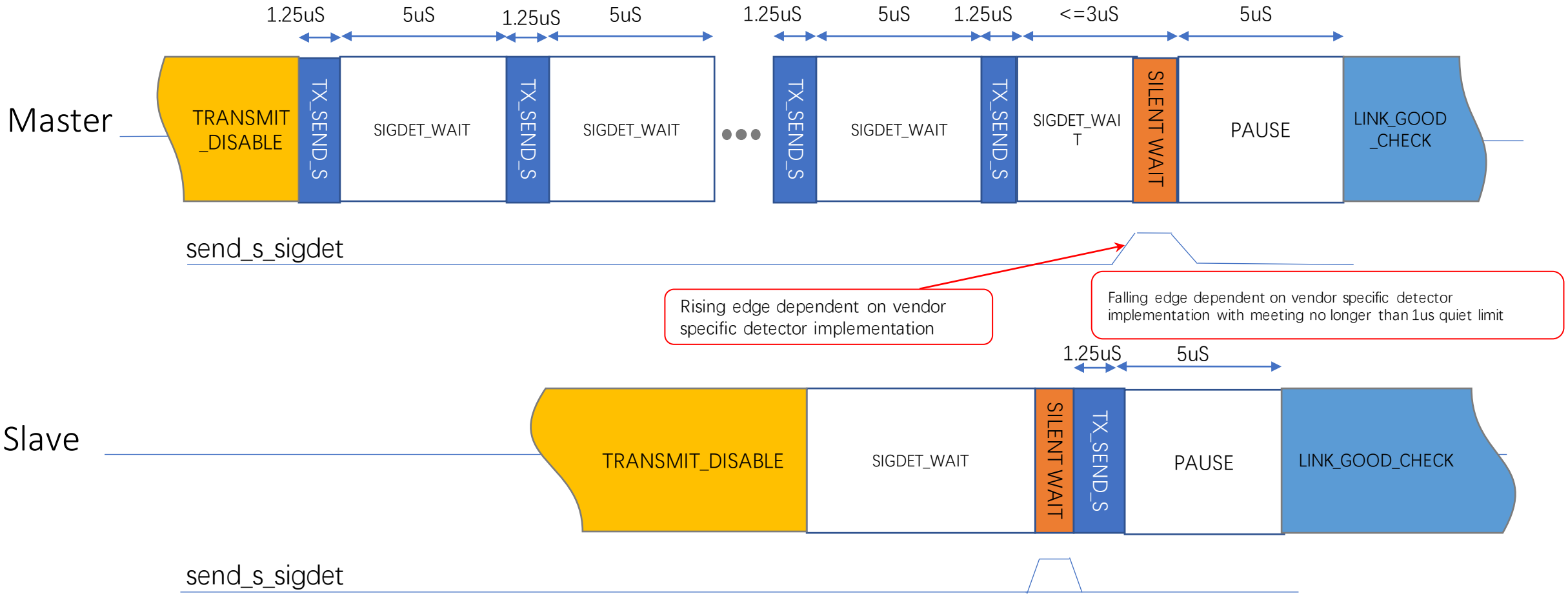


IEEE 802.3ch Figure 149-31 - PHY Link Synchronization state diagram

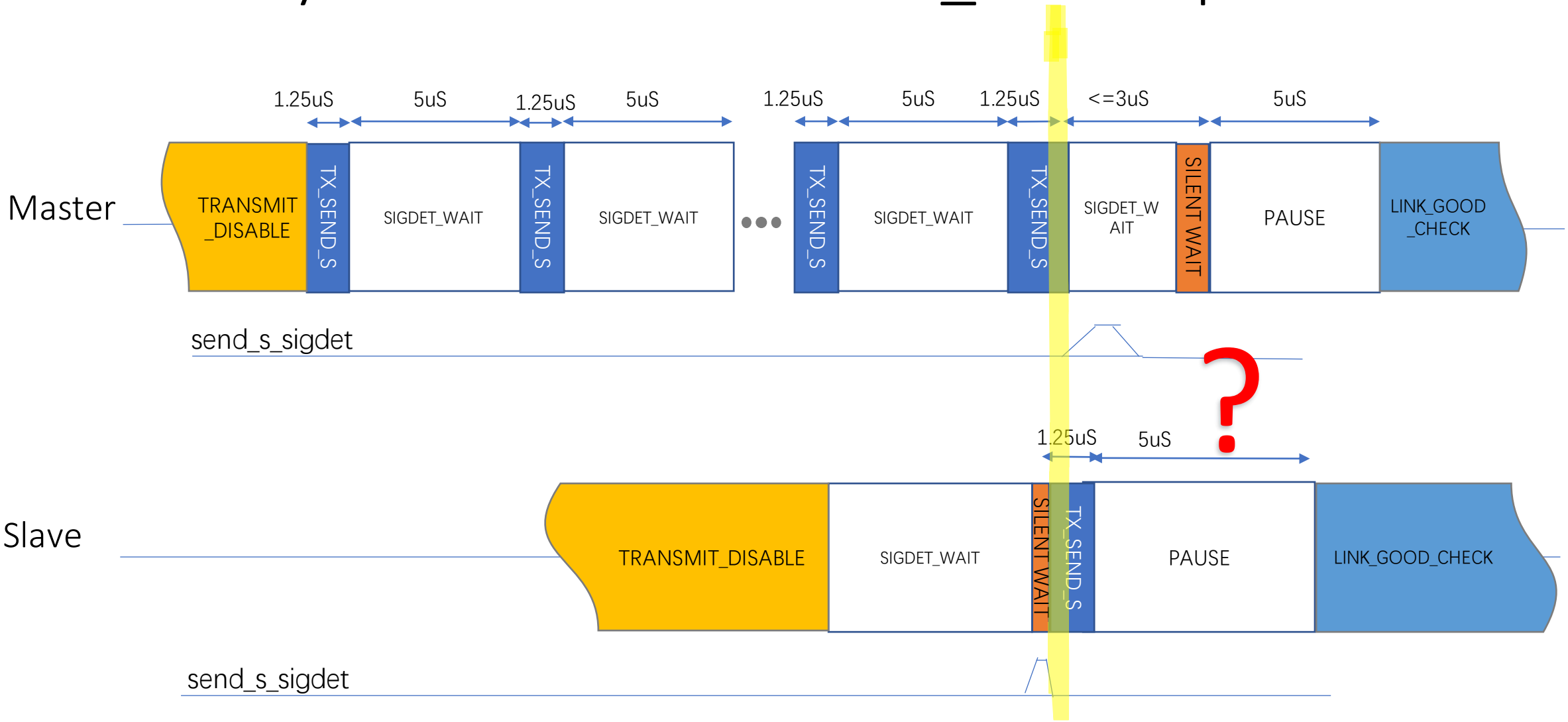
Problem - possible overlap of MASTER/SLAVE send_s frames

- Definition of send_s_sigdet
  - This variable indicates whether the SEND_S signal was detected. This variable shall be set FALSE, no later than 1 µs after the signal goes quiet on the MDI.
    - TRUE: SEND_S signal detected.
    - FALSE: SEND_S signal not detected.
- Detector of SEND_S:
  - 3 full cycle of frame of 255 PRBS patterns in SEND_S signal
  - send_s_sigdet
    - Rising edge could come up at first peak or later depending on vendor implementation
    - falling edge come up no later than 1us after MDI goes quite (specified at definition)
    - falling edge come could come up before line is quite (no requirement/definition)
- Overlap of MASTER and SLAVE frame
  - SLAVE move from SILENT_WAIT to TX_SEND_S “too early” before line is quiet
  - Both MASTER and SLAVE at TX_SEND_S
    - Depending Detector design, it may be an issue to have false or miss detections
    - To avoid confusions, it should be better fixed

PHY Link Synchronization - Normal



PHY Link Synchronization – sends_s overlap



Proposed Solution – Add a timer at SILENT_WAIT state

- Add a timer silent_wait_timer , to stay in SILENT_WAIT for at least 1.25us to avoid overlap
- silent_wait_timer = 1.25us

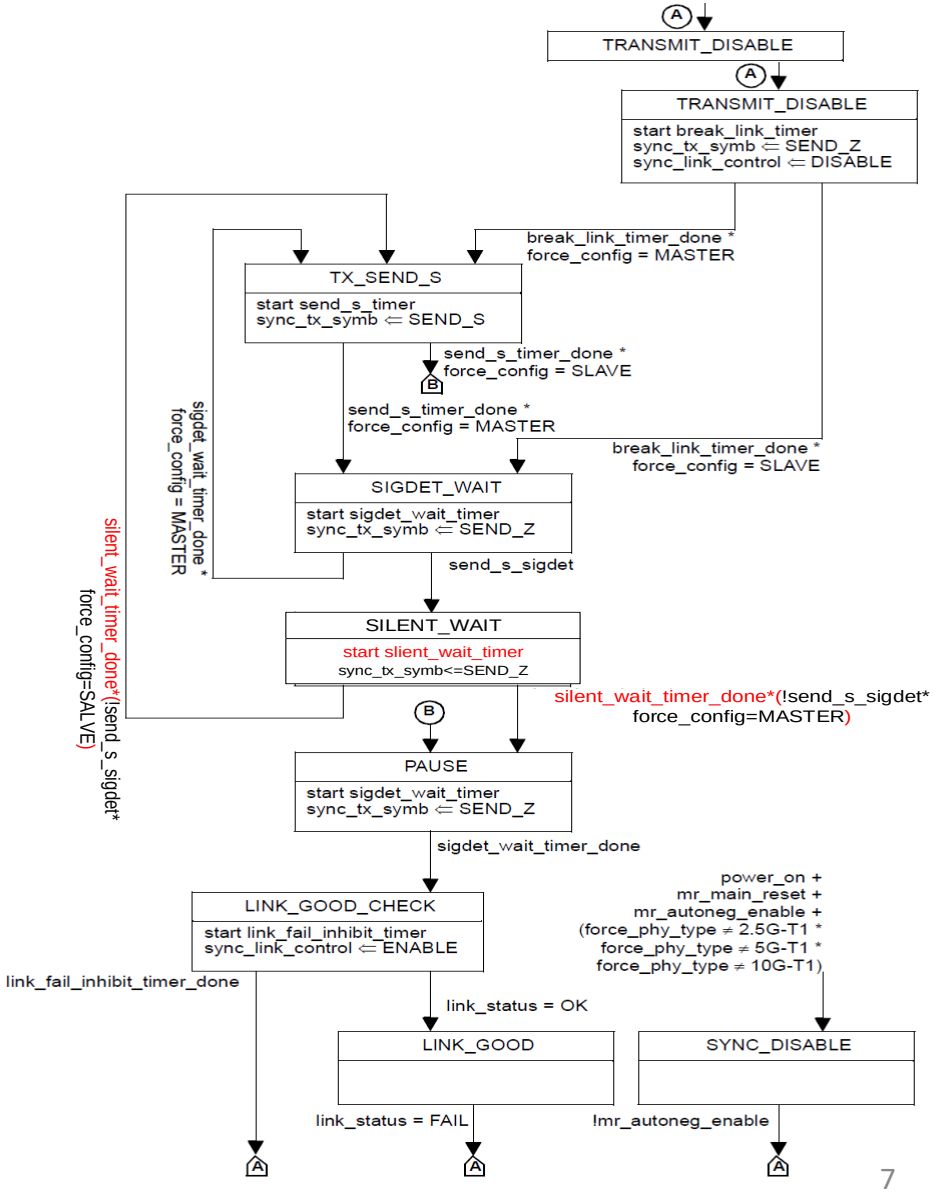
Case 1:

- Period of at least 363ns after seeing the signal is needed for *send_s_sigdet* become True at any reasonable detector (at least one peak checked)
- Total time to be quiet > 1.613us after seeing frames from LP and longer than 1.25us , no overlap

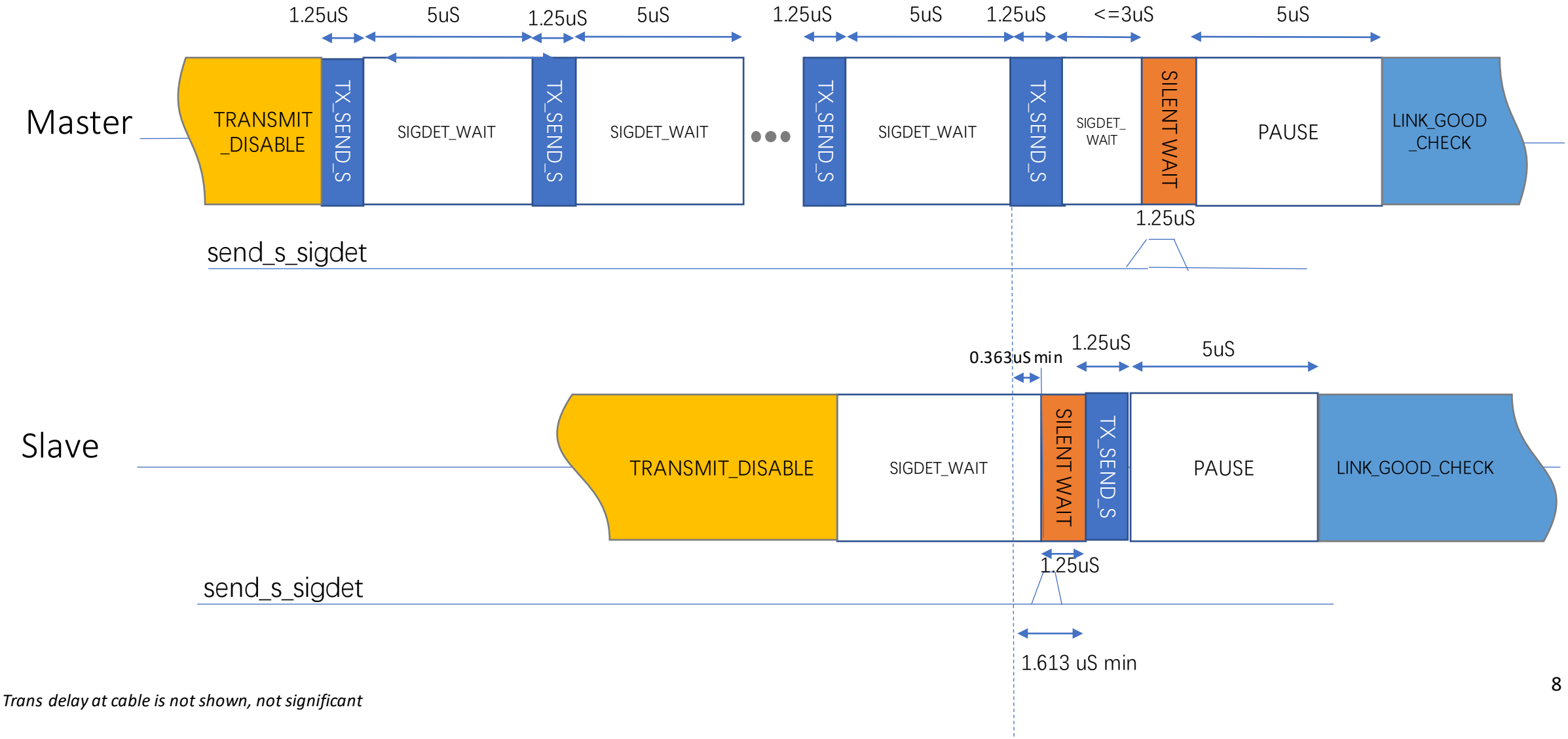
Case 2:

- The longest time period for *send_s_sigdet* to become *false after seeing send_s from LP is 2.5us (1.25+1.25)* .
- Total time to be quiet > 2.5us after seeing frames from LP and longer than 1.25us , no overlap, and 2.5us gap of quiet period on the other end if MASTER still transmits

transport delay on 15m cable less than 0.1us (ignored for the analysis)

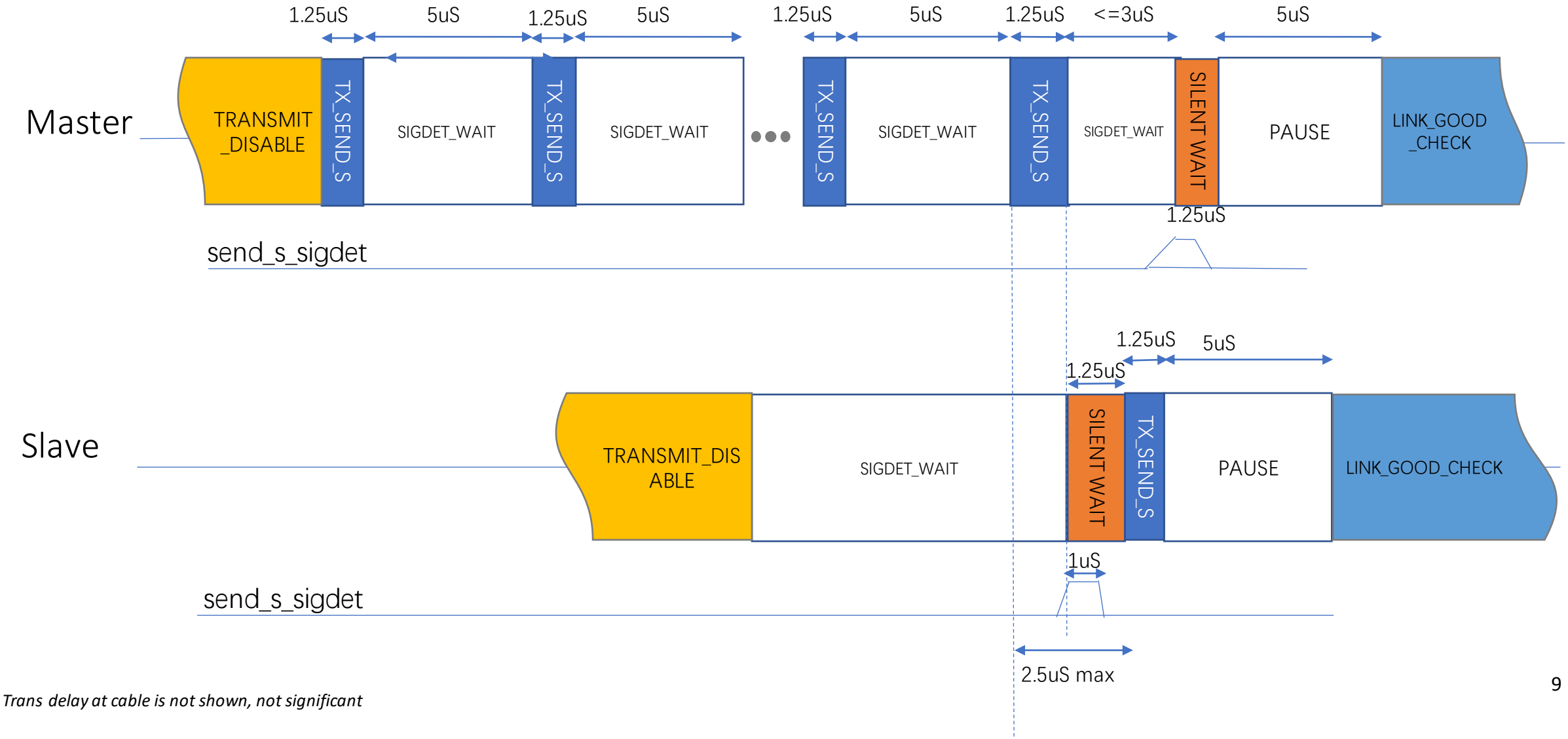


PHY Link Synchronization with added timer – case 1



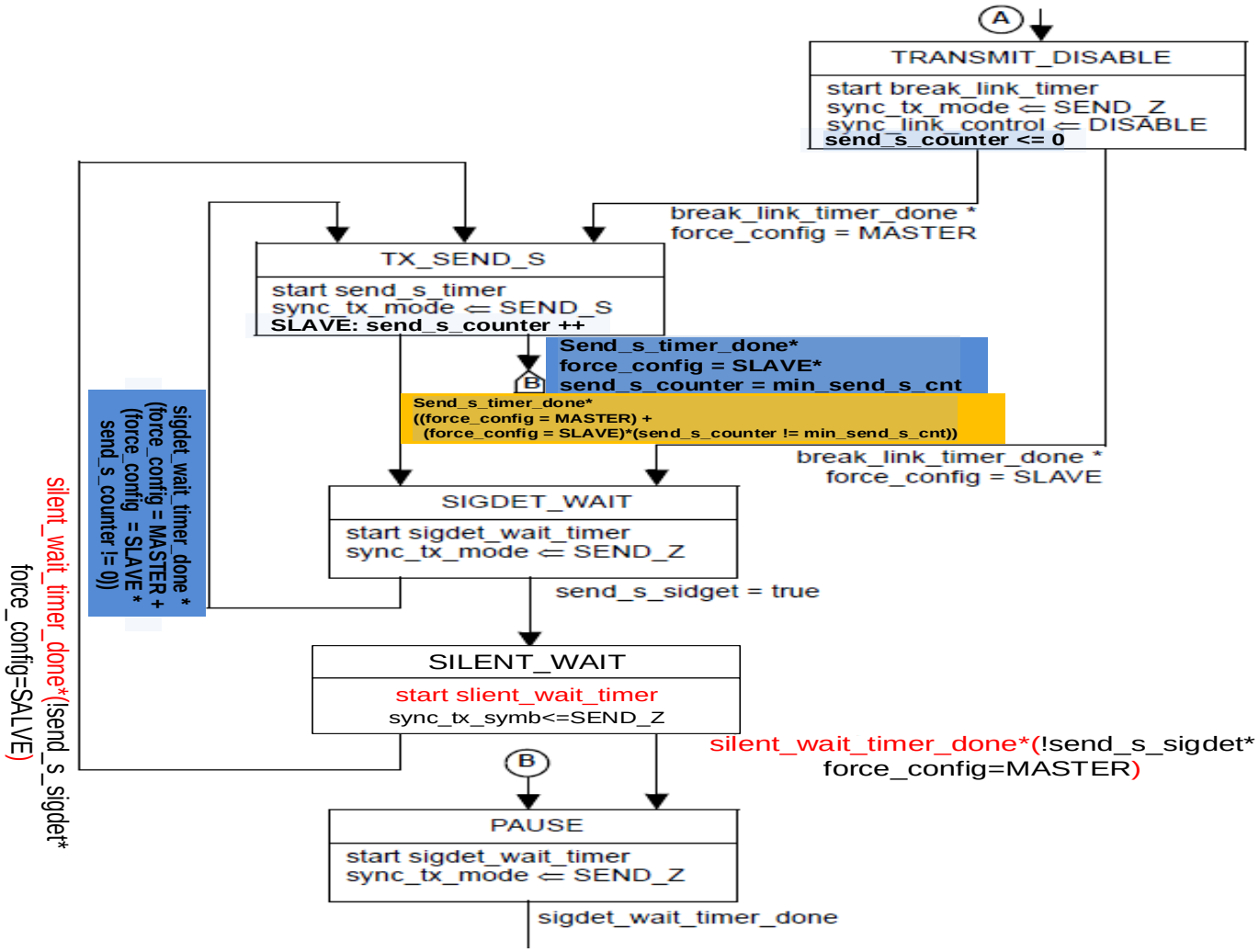
Note: Trans delay at cable is not shown, not significant

PHY Link Synchronization with added timer- case2



Note: Trans delay at cable is not shown, not significant

Final proposed state machine at 802.3cy



State diagram with changes proposed at wu_3cy_01_0122

Conclusion

To avoid overlapping of SEND_S signals from Master and Slave:

- Add in a timer at SILENT_WAIT state
- silent_wait_timer
  - value: 1.25us ± 0.05 µs

Thank You