Slave Startup : Duration Of SILENT State And Defining timing_lock_OK (updated June 19, 2022)

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Reduce the duration slave SILENT state

- Reduce the slave SILENT state to 30ms from 40ms
  - Master : From entry to SILENT state until en_slave_tx = 1 transmitted
  - Slave : Entry to exit of SILENT state

Table 165–10—Startup timing maxima for MASTER

Timing interval	Maximum time (ms)
From entry to SILENT state until en_slave_tx = 1 is transmitted	40 – 0.384
From entry of SILENT state until entry to COUNTDOWN state	95.975 – 0.384
Entry to COUNTDOWN until entry of TX_SWITCH	0.384
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

Table 165–11—Startup timing maxima for SLAVE

Timing interval	Maximum time (ms)
Entry to exit of SILENT state	40
Entry of SILENT state to exit of TRAINING state	95.975 – 0.384
Entry to COUNTDOWN until entry of TX_SWITCH	0.384
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

Define timing_lock_OK

- Recommended solution: adding a language similar to base Training to section 165.4.2.4.10, line 47

“In the TRAINING state, whenever slave operating in loop timing locks the Master timing reference, slave sets timing_lock_OK=1”

Thank You

Define timing_lock_OK (Alternative solution)

- Alternative solution: adding a language similar to requirement on master transmitter clock frequency in 165.5.3.6 , to section 165.4.2.4.10, line 47
  - After setting the “timing_lock_OK”, the slave transmitter clock short-term rate of frequency variation **shall** be less than TBD ppm/second

Startup timing: cy vs BASE-T

- There is imbalance between duration of states and tasks in cy standard
  - Comparing to Base T(2.5/5/10G),
    - The timing of silent half duplex, and training state in cy is similar to timing of 2.5/5/10G base T before PBO exchange
  - 2.5/5/10G base T links up after more than one second of the full training after PBO exchange

More than	Base T timing(ms)	Base T1 timing (ms)
Slave half duplex	350 (42% timing before PBO exchange)	40 (41% timing before link up)
Full duplex	480 (58% timing before PBO exchange)	56 (58% timing before link up)
Full duplex training	More than **1000ms** of training before link up	

Slave SILENT state in Current 802.3cy text

- Slave has to detect the infofield
  - "During startup, prior to entering the TRAINING state, the **SLAVE shall** align its transmit 65B RS-FEC frame to within +0/–4 partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE Infofield partial PHY frame count shall match the MASTER Infofield partial PHY frame count for the aligned frame"
  - Slave shall detect en_slave_tx = 1 in master infofield (PHY Control state diagram)
- The main task is making sure slave transmission does not cause problem for Master

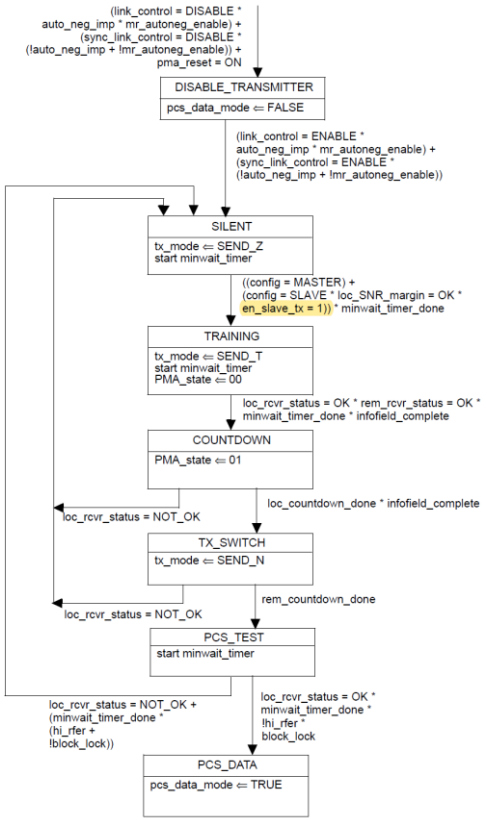

Figure 165–28—PHY Control state diagram