Delay Constraint

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Overview

- The delay constraint, which is a limit on the maximum internal delay of the combined receive and transmit paths in the PHY, is not specified in Draft 1.2
- Some of the contributing factors to this delay are discussed in the following presentations
  - https://www.ieee802.org/3/ch/public/apr19/Lo_3ch_01_0419.pdf
  - https://www.ieee802.org/3/bp/public/jul14/Lo_3bp_01a_0714.pdf
  - https://www.ieee802.org/3/bp/public/jul14/shen_3bp_01_0714.pdf
- The primary contributor is the buffering associated to FEC and interleaving

Proposal for Delay Constraint

- The following table shows the proposed limits for the delay for various interleaving depth
- The number for interleaving depth of 1 is scaled from 802.3ch for baud-rate, frame size and with some headroom for implementation
- These numbers are also rounded up for integer number of pause quanta

Interleave Depth	Bit Time	Pause Quanta	Delay (ns)
1x	25600	50	1024
2x	36864	72	1474.56
4x	58880	115	2355.2
8x	102400	200	4096