MARVELL

Realistic Parameter Values in Capacity Calculations

Configuring jonsson_3cy_01_10_28_20 capacity calculations

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802.3cy

Introduction

- We introduced channel capacity calculation tool in jonsson_3cy_01_10_28_20
- This contribution addresses some of the practical issues when using this calculator and recommends reference simulation values
- Examples are given of how the calculator can be used to evaluate performance of different system configurations

	Upstream	Downstream
ments		
ate [Gbps]:	25	25
output BER:	1.00E-12	1E-12
ble Length [m]:	8.5	8.5
-reflections [dB]:	-40	-40
nber of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
S-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-140	-140
EC cancelation [dB]:	5	5
Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
ax Simulation Frequency:	1.00E+10	

ated Values		
	Upstream	Downstream
dB]:	21.77	21.77
	21.77	21.77
	17.78	17.78
	08	3.98
	28.3	

Background

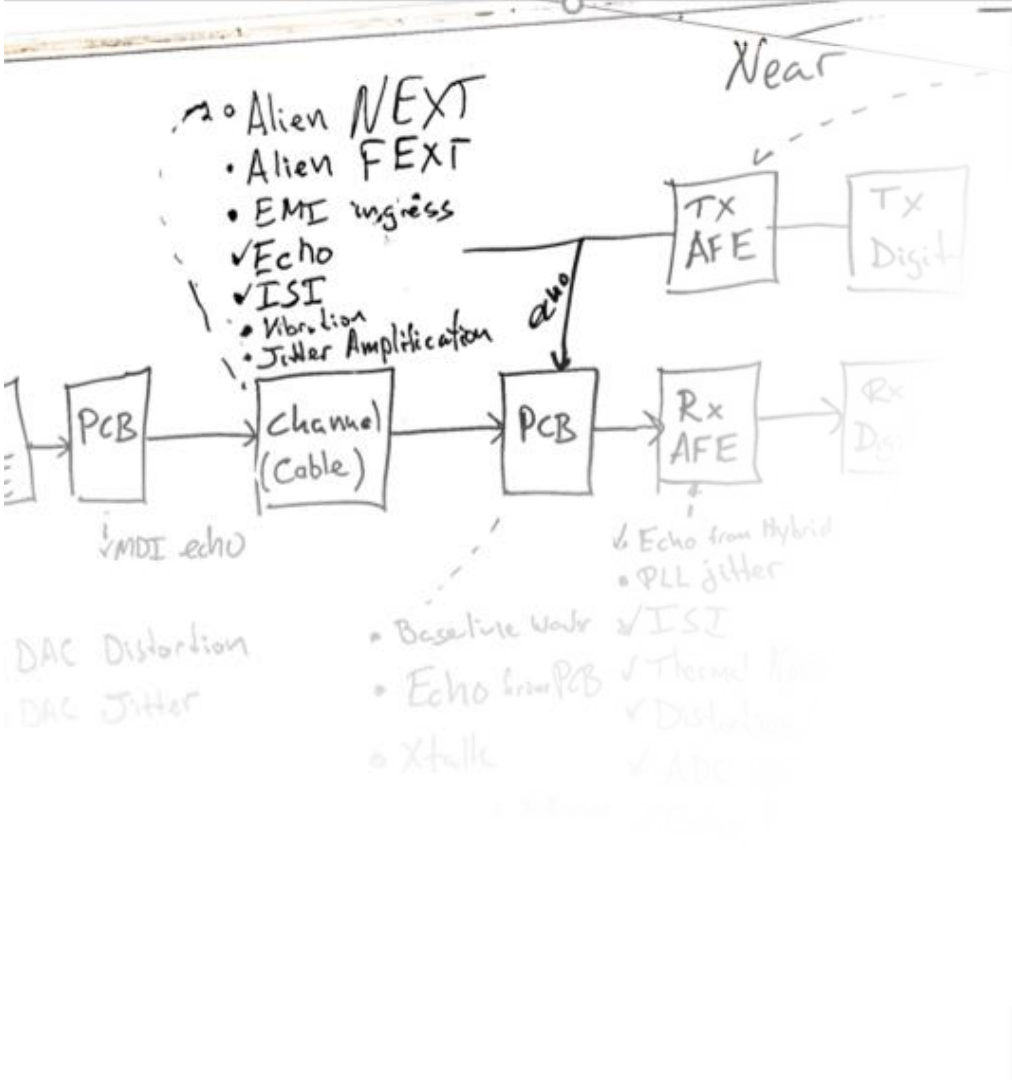
- The channel capacity calculator model introduced in jonsson_3cy_01_10_28_20 is based on theoretical calculations and system approximations
- The spreadsheet for the channel capacity calculator can be found at the link at the bottom of this slide
- The outcome of any calculation depends on the input values

- Evaluation of capacity-based models is highly sensitive to the uncancelled noise floor that is used in the calculations
- While it is tempting to use aggressive initial values, the impacts of using unrealistic values is that the PHY implementation may become impractical
- It is important to use realistic assumptions in the channel capacity calculations

https://www.ieee802.org/3/cy/public/adhoc/jonsson_3cy_01_10_28_20.xlsx

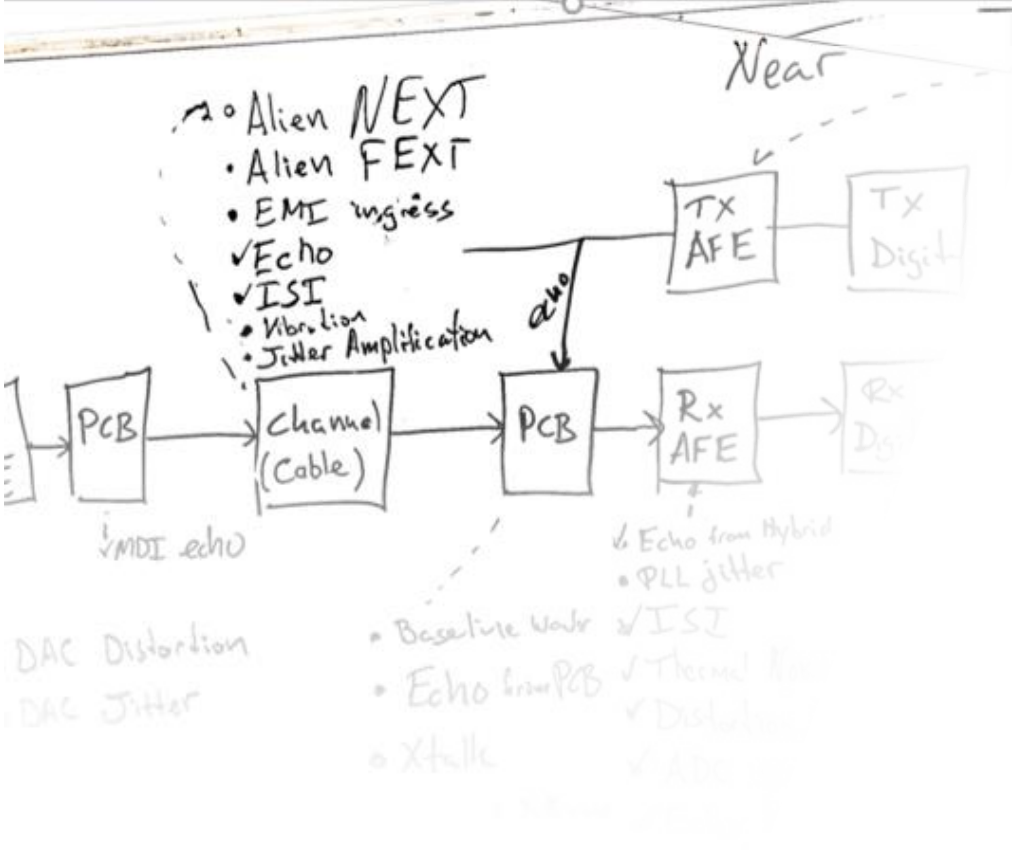
Noise Sources

- There are numerous noise sources in a communication system that will affect the SNR
- The list of all the noise sources is too long to list and analyze in a short presentation like this one
- Some of the key noise sources are:
  - PCB and system background noise
  - Cross talk
  - EMI Ingress
  - AFE thermal noise
  - Jitter Noise
  - Non-linearities
  - ADC quantization noise
  - Quantization noise in digital processing



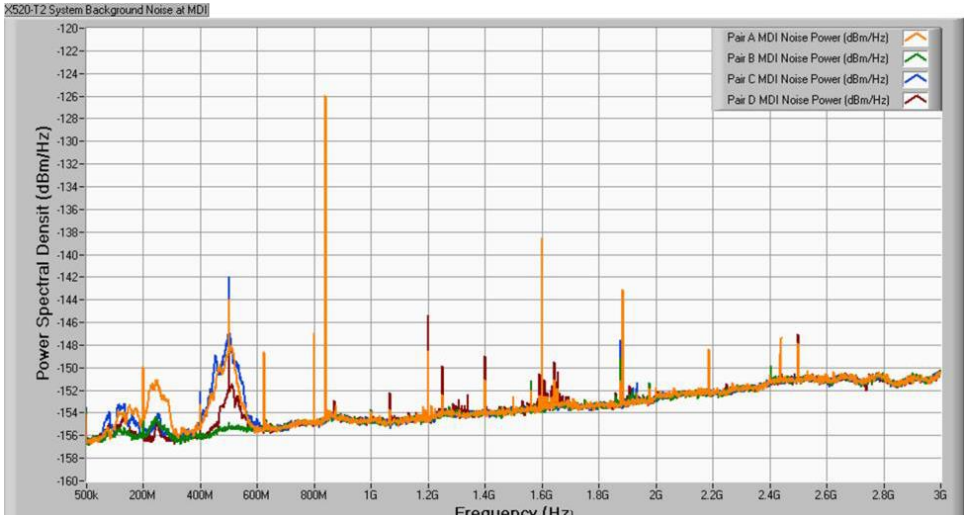
Noise Sources

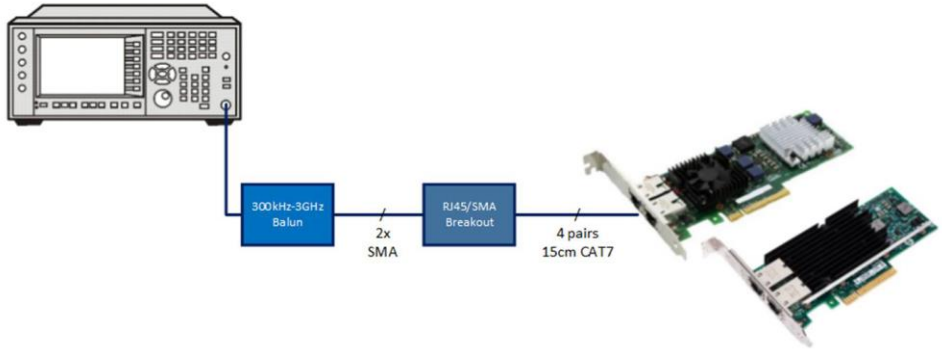
- The Cross Talk and EMI Ingress (largely) depend on the environment
  - They can be limited by standard specifications
  - They are not directly effected by the by the communication system design, but they do influence the design
- The PCB and system background noise depend on the communication system design
- The remaining noises primarily depend on the design tradeoffs in the Phy design
  - AFE thermal noise, Jitter Noise and Non-linearities depend on analog design of the AFE
  - ADC quantization noise is usually designed to be in line with other noise in the AFE
  - Quantization noise in digital processing is usually optimized to reflect the AFE noise



PCB & System Noise Floor

- According to cibula_3bq_02a_0314 the noise floor for a very good PCB board under good conditions is −152dBm/Hz
- According to cibula_3bq_02_0514 the noise floor for in a benign LAN server environment is about −149dBm/Hz
- We can assume that for a production board in automotive environment the PCB and System noise will be at least −150dBm/Hz and will probably be higher





The figures above are from cibula_3bq_02a_0314

Receive AFE Noise Floor

- The AFE noise floor can be approximated from the peak signal level and the background noise
  - AFE performance is often expressed as Effective Number of Bits (ENOB)
- The peak signal can be estimated from
  - the transmit level,
  - the insertion loss (IL) and
  - the Peak to Average Ratio (PAR)
- The PAR depends on receive signal properties, including modulation and IL transfer function
  - In this presentation we use effective PAR, PAR_e, which also accounts for headroom to limit signal clipping

The noise floor N_{AFE} (in dBm/Hz) can be estimated with

$$N_{AFE} \approx P_{tx} - IL_{avg} - ENOB \times 6dB + PAR_e$$

where

- P_{tx} is the transmit power in dBm/Hz
- IL_{avg} is the average Insertion Loss in dB
- $ENOB$ is the AFE-ENOB
- PAR_e is the effective PAR in dB

Receive AFE Noise Floor

Table values assume

- P_{tx} = -98dBm/Hz
- IL_{avg} = 12dB
- PAR_e = 9dB*

* Given 9GHz of bandwidth, and PAM-4 Tx PAR of 7 dB with distortion, PAR of 9dB is optimistic

ENOB	AFE Noise [dBm/Hz]
5	-131
5.5	-134
6	-137
6.5	-140
7	-143
7.5	-146
8	-149
8.5	-152

$$N_{AFE} \approx P_{tx} - IL_{avg} - ENOB \times 6dB + PAR_e$$

- It is realistic to assume that ENOB is close to 6 to 7 bits in practical designs
  - Higher ENOB means bigger die area and higher power consumption
  - This is consistent with other 802.3 PHYs with multi-GHz bandwidth
  - Going beyond 7.5 ENOB has diminishing returns even in the optimistic -149dBm/Hz (non-automotive) environments [cibula_3bq_02_0514]

Assuming AFE noise in the range −137dBm/Hz to −143dBm/Hz is a good estimates

Other Simulation Parameters

- Insertion loss of PCB
  - According to kadry_3cy_02_0820 the PCB IL per inch is about 0.8dB at 7GHz
  - This can be approximated by adding 0.25m to the cable length for each inch of PCB
  - For 2 PCB boards with 3in trace each this becomes 1.5m
- Transmit PSD
  - In the absence of transmit PSD mask it is simplest to use flat PSD (named PSD_brick in the model)
  - If transmit power has not been specified, it is reasonable to use 0dBm as reference transmit power

- Implementation Loss and Margin
  - The implementation loss and the margin can often be bundled into one total margin number
  - It is common to use 6-10dB for the combined total margin
  - The jonsson_3cy_01_10_28_20 capacity calculator accounts for AFE noise floor and residual echo, so smaller total margin can be assumed
  - It is reasonable to require total margin of 2-6dB in the capacity calculator

Summary of Generic Model Parameters

- AFE Noise Floor
  - −137dBm/Hz to −143dBm/Hz
- PCB Insertion Loss
  - Add 1.5m to cable length
- PSD-mask
  - PSD_brick
- Transmit Power
  - 0dBm
- Implementation Loss + Margin
  - 2-6dB

	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-140	-140
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

7m cable + 1.5m for PCB

Flat PSD mask with 0dBm transmit power

AFE-noise of -140dBm/Hz

0dB Impl. Loss means more margin is needed

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.77	21.77
Estimated Slicer SNR [dB]:	21.77	21.77
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	3.98	3.98
Nyquist Frequency [GHz]:	6.90	6.90
Insertion Loss @ Nyquist [dB]:	28.39	28.39

This total margin must account for Impl. Loss

Example Capacity Calculations

- Following slides give few examples of capacity calculations for different configurations
- All calculations assume 7m cable with two inline connectors
- All calculations include PCB IL
- All but one calculation assumes PAM-4 modulation
- All but one calculation assumes $-40dB$ micro-reflection loss

- Different System configurations:
  - 25G symmetric Echo Canceled systems
  - 25G up and 2.5G down asymmetric TDD systems
  - 25G symmetric TDD systems (one example)
- Different AFE-noise levels:

  -137dBm/Hz

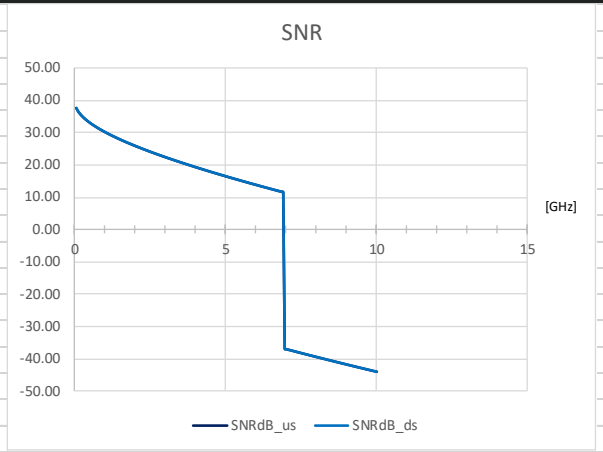
  -140dBm/Hz

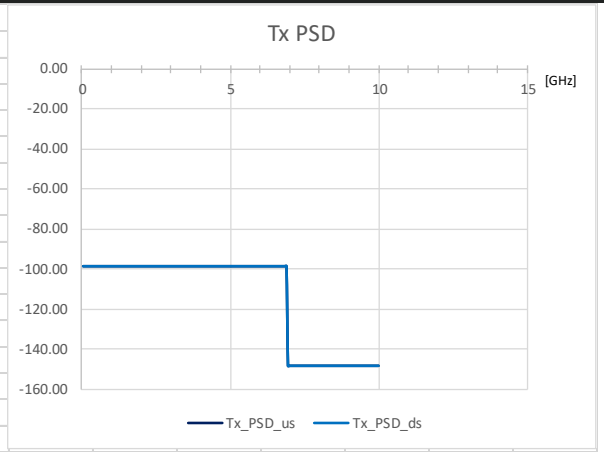
  -143dBm/Hz

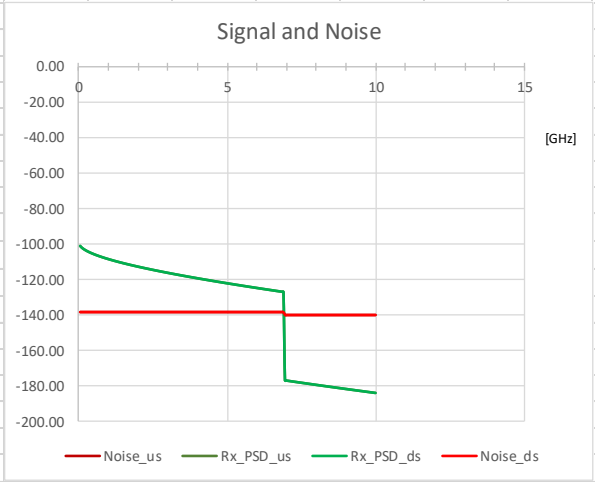
Example Performance for Echo Canceled System (7m Cable + PCB)

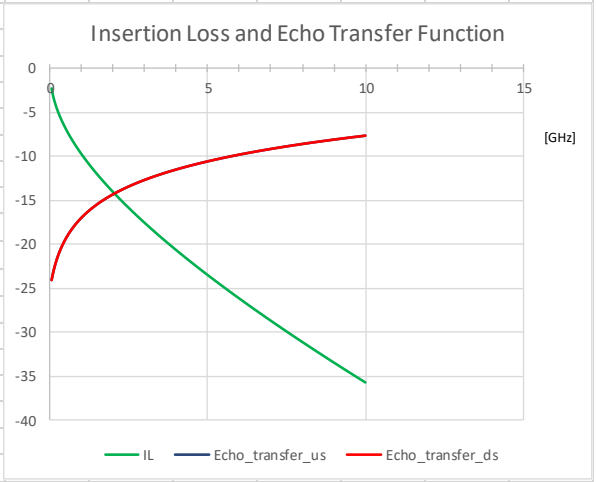
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-140	-140
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.77	21.77
Estimated Slicer SNR [dB]:	21.77	21.77
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	3.98	3.98
Nyquist Frequency [GHz]:	6.90	6.90
Insertion Loss @ Nyquist [dB]:	28.39	28.39





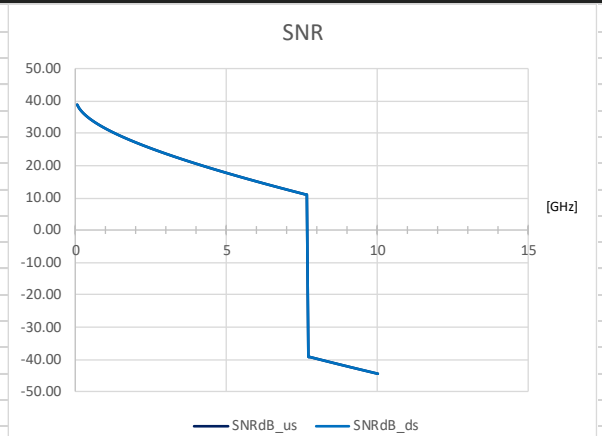


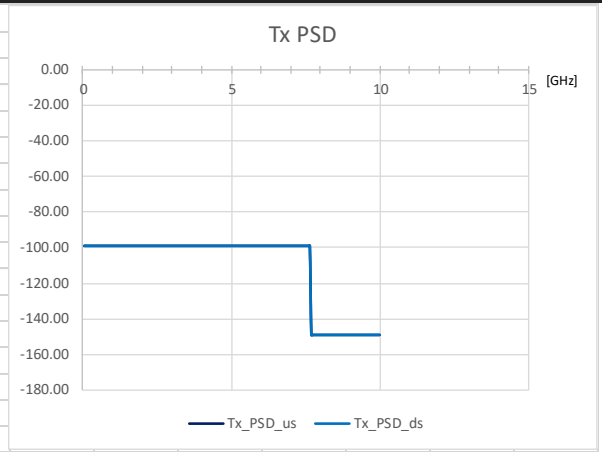


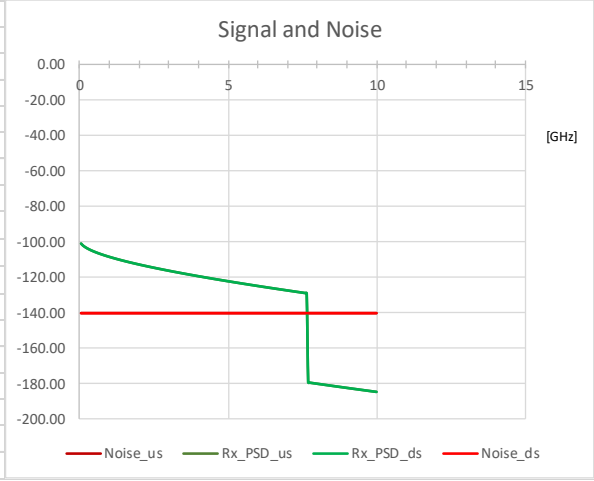
Example Performance for TDD System (7m Cable + PCB)

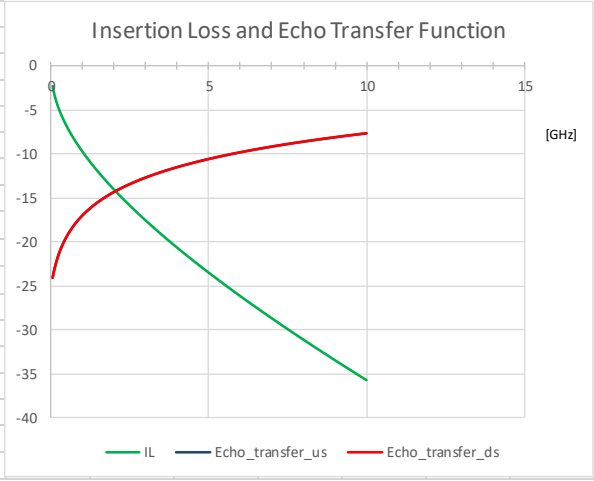
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	2.5
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	90%	9%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-140	-140
EC cancelation [dB]:	100	100
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	21.81	21.81
Estimated Slicer SNR [dB]:	21.81	21.81
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	4.02	4.02
Nyquist Frequency [GHz]:	7.67	7.67
Insertion Loss @ Nyquist [dB]:	30.22	30.22





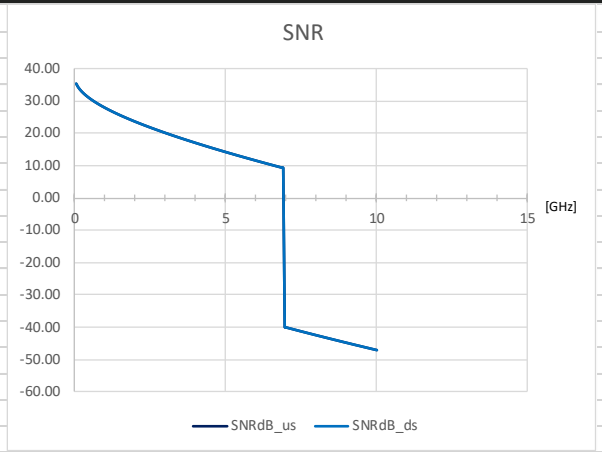


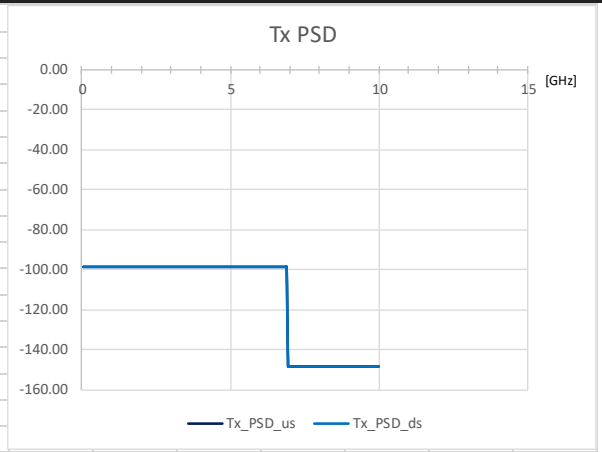


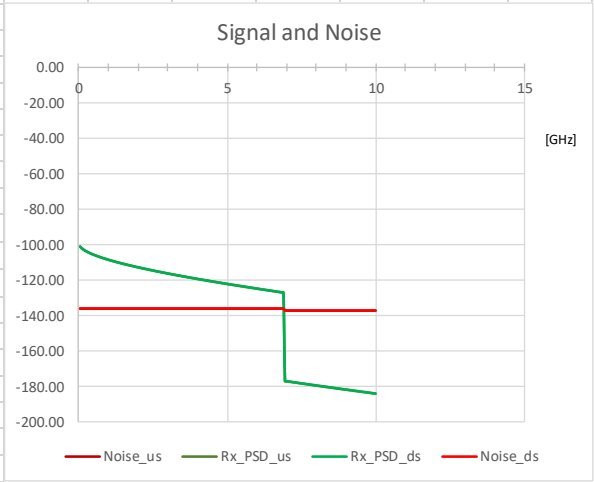
Example Performance for Echo Canceled System (with -137dBm/Hz)

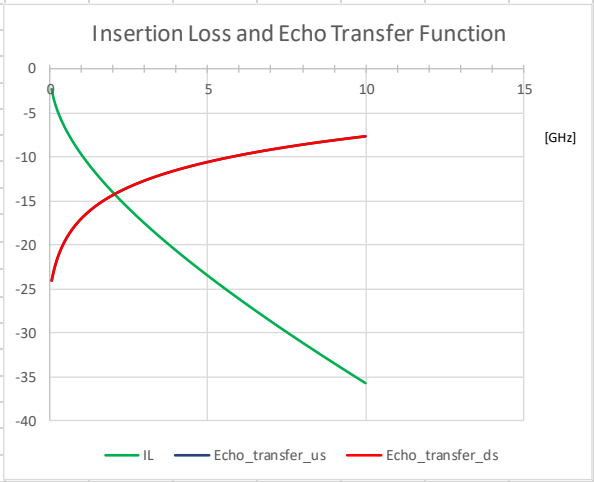
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-137	-137
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	19.51	19.51
Estimated Slicer SNR [dB]:	19.51	19.51
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	1.73	1.73
Nyquist Frequency [GHz]:	6.90	6.90
Insertion Loss @ Nyquist [dB]:	28.39	28.39





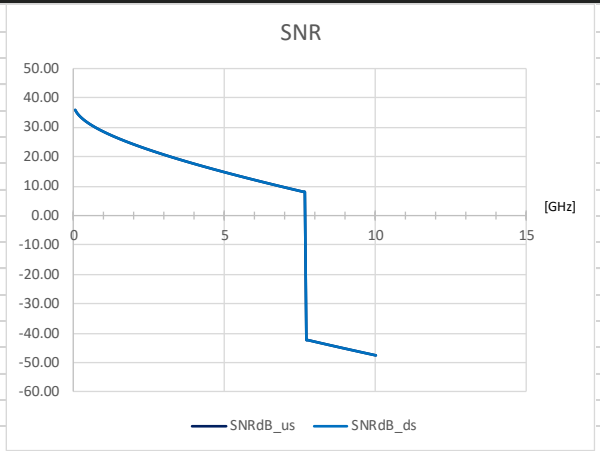


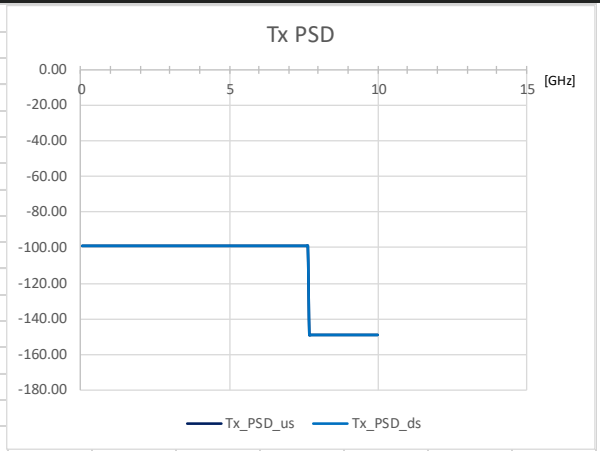


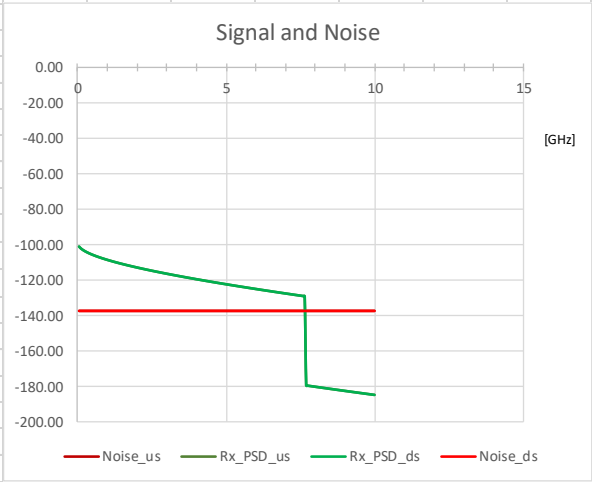
Example Performance for TDD System (with -137dBm/Hz)

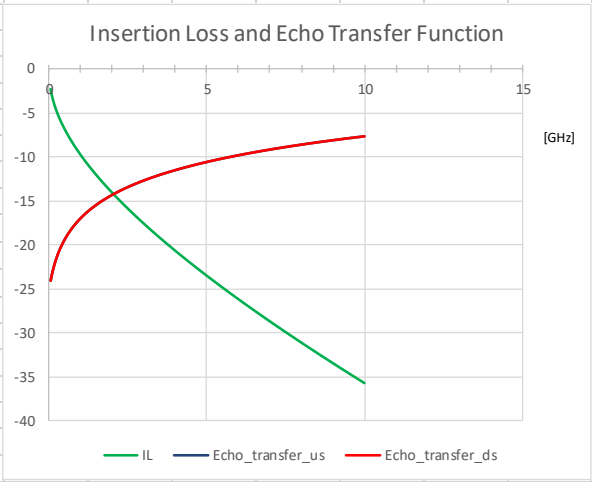
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	2.5
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	90%	9%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-137	-137
EC cancelation [dB]:	100	100
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	18.81	18.81
Estimated Slicer SNR [dB]:	18.81	18.81
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	1.03	1.03
Nyquist Frequency [GHz]:	7.67	7.67
Insertion Loss @ Nyquist [dB]:	30.22	30.22





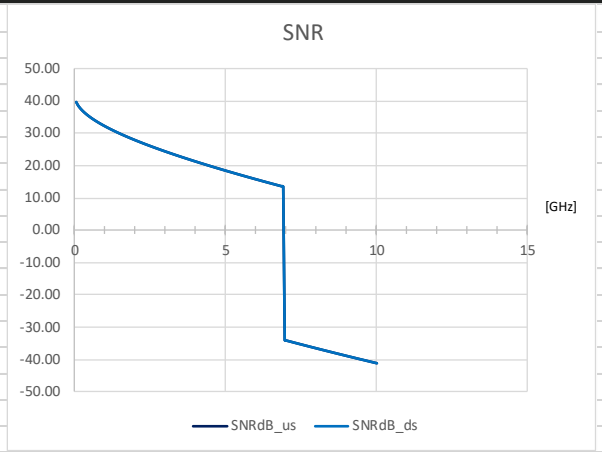


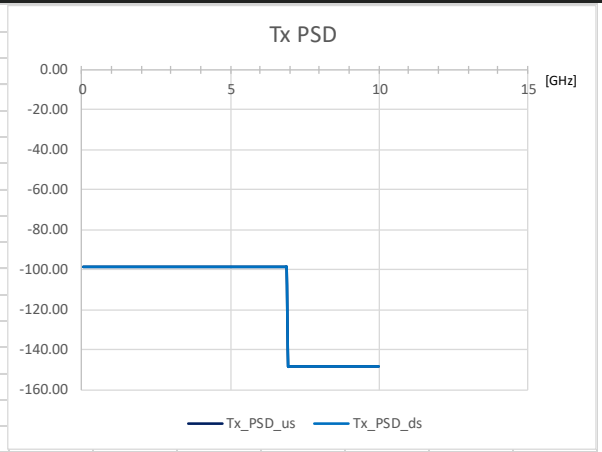


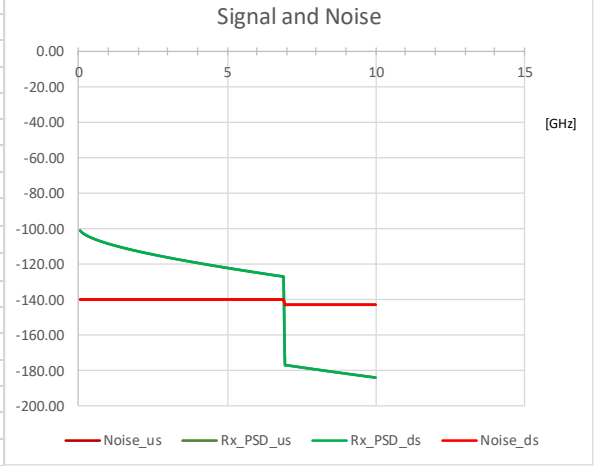
Example Performance for Echo Canceled System (with -143dBm/Hz)

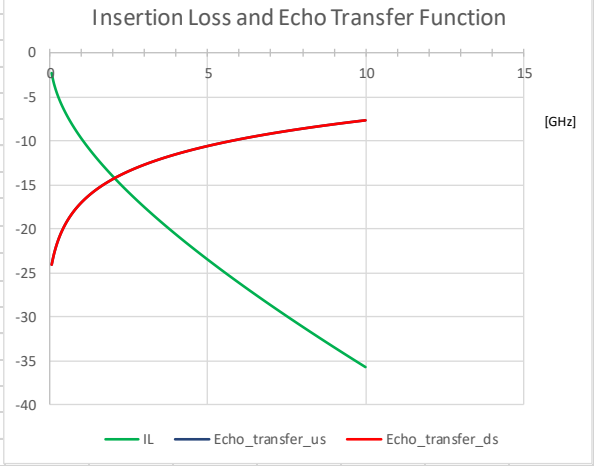
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-143	-143
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	23.59	23.59
Estimated Slicer SNR [dB]:	23.59	23.59
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	5.80	5.80
Nyquist Frequency [GHz]:	6.90	6.90
Insertion Loss @ Nyquist [dB]:	28.39	28.39





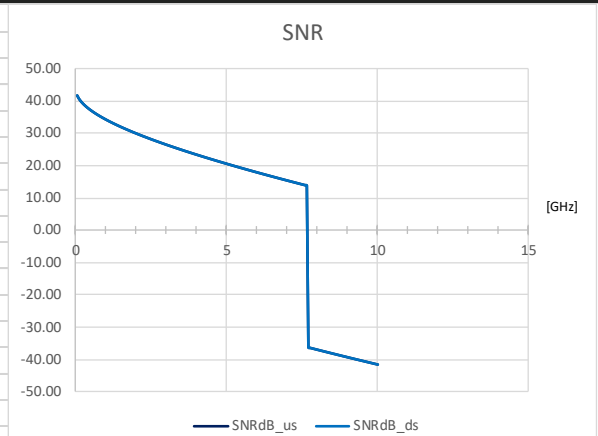


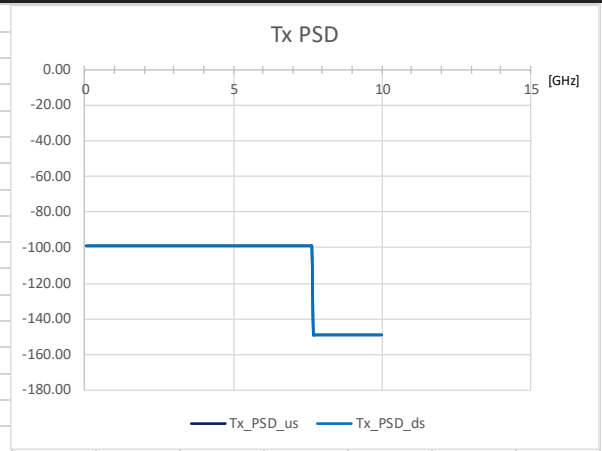


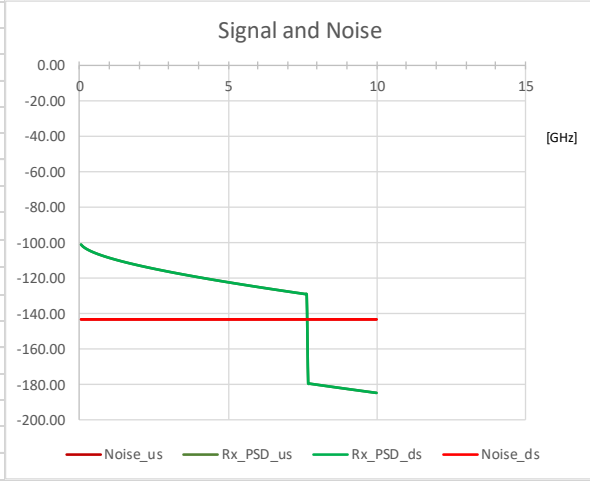
Example Performance for TDD System (with -143dBm/Hz)

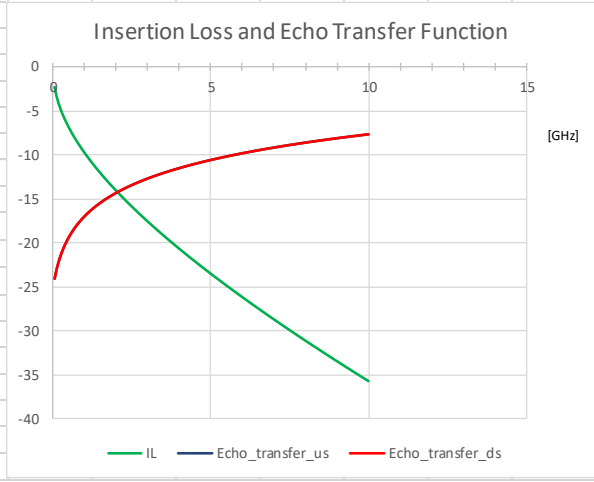
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	2.5
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	90%	9%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-143	-143
EC cancelation [dB]:	100	100
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	24.80	24.80
Estimated Slicer SNR [dB]:	24.80	24.80
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	7.01	7.01
Nyquist Frequency [GHz]:	7.67	7.67
Insertion Loss @ Nyquist [dB]:	30.22	30.22





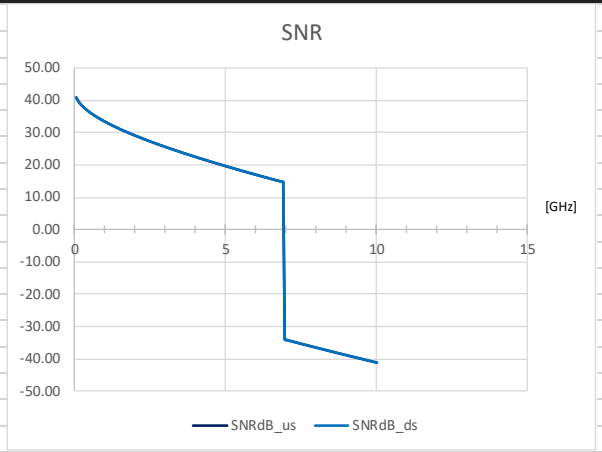


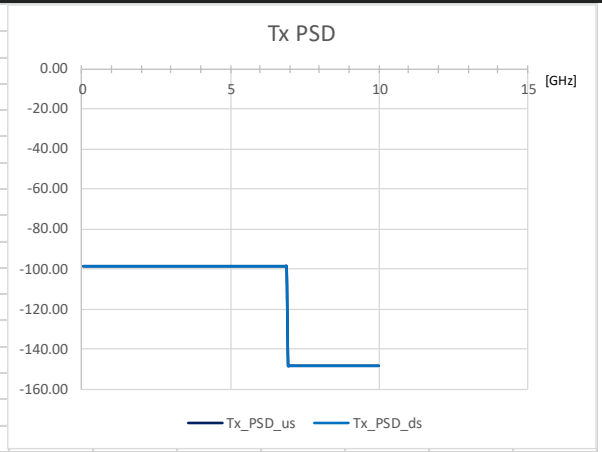


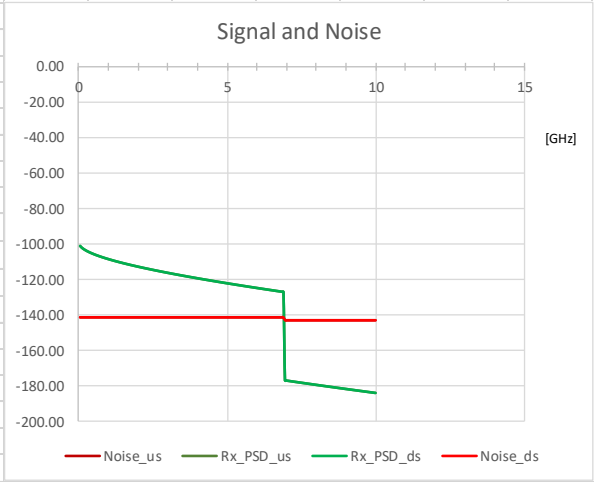
Example Performance for Echo Canceled System (-43dB micro-reflections)

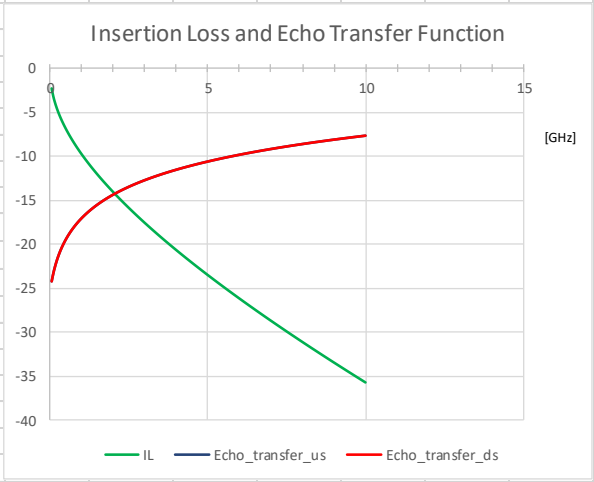
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-43	-43
Number of Connectors:	4	4
Modulation		
PAM Levels:	4	4
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-143	-143
EC cancelation [dB]:	5	5
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	24.77	24.77
Estimated Slicer SNR [dB]:	24.77	24.77
Required Slicer SNR [dB]:	17.78	17.78
SNR Margin [dB]:	6.98	6.98
Nyquist Frequency [GHz]:	6.90	6.90
Insertion Loss @ Nyquist [dB]:	28.39	28.39





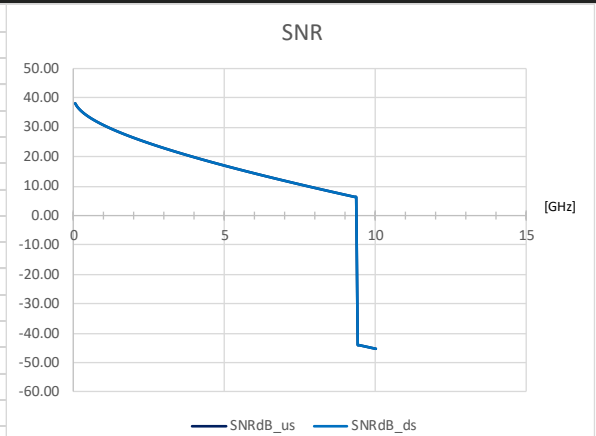


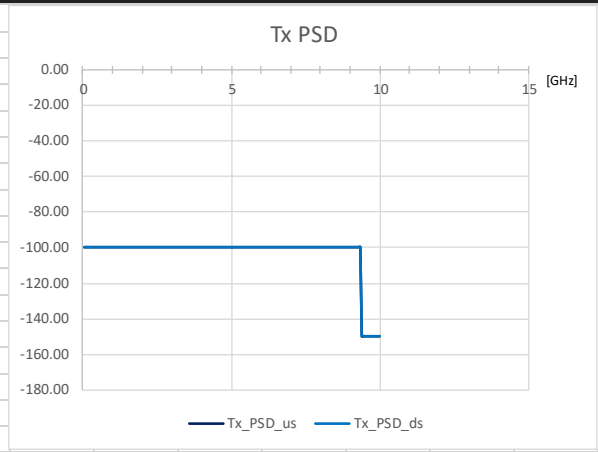


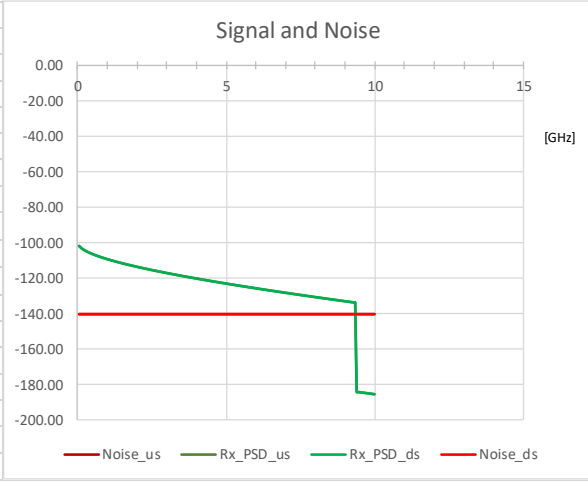
Example Performance for Symmetric TDD System (with PAM-8)

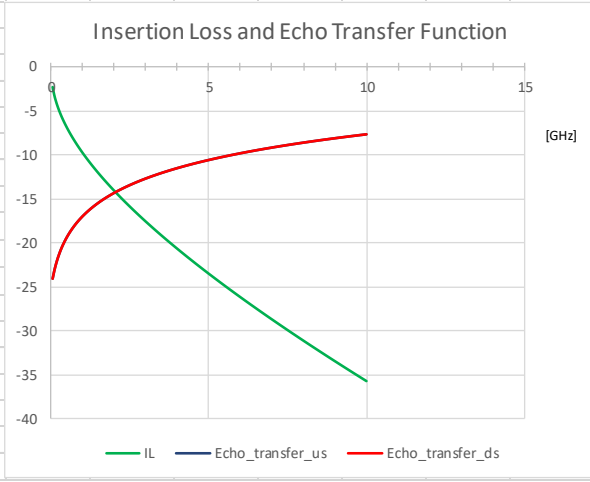
	Upstream	Downstream
Requrements		
Data Rate [Gbps]:	25	25
Target RS-FEC output BER:	1.00E-12	1E-12
Cable Length [m]:	8.5	8.5
Wire u-reflections [dB]:	-40	-40
Number of Connectors:	4	4
Modulation		
PAM Levels:	8	8
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	49%	49%
Transmit Signal		
PSD-mask:	PSD_brick	PSD_brick
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	0.0001
AFE-noise [dB/Hz]:	-140	-140
EC cancelation [dB]:	100	100
EC Connector cancelation [%]:	100%	100%
Implementation Loss [dB]:	0	0
Simulation Parameters		
Cable Model:	eq149-18	
Connector Echo Model:	hard	
Max Simulation Frequency:	1.00E+10	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	18.54	18.54
Estimated Slicer SNR [dB]:	18.54	18.54
Required Slicer SNR [dB]:	24.12	24.12
SNR Margin [dB]:	-5.58	-5.58
Nyquist Frequency [GHz]:	9.39	9.39
Insertion Loss @ Nyquist [dB]:	34.19	34.19







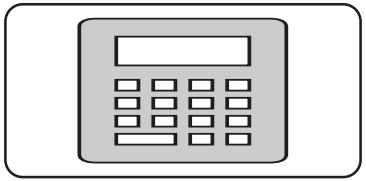


Observations About the Example Calculations

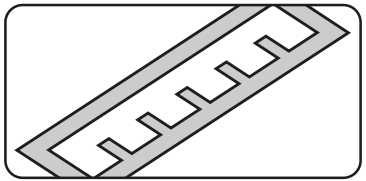
- Echo Canceled system with 25G upstream and 25G downstream has similar SNR margin as asymmetric Time Division Duplexing system with 25G upstream and 2.5G downstream
- Symmetric 25G TDD system has considerably lower performance (SNR margin) than Echo Canceled symmetric system

- Symmetric 25G Echo Canceled system can operate over approximately 7m cable when accounting for PCB Insertion Loss and realistic noise numbers
- Echo Canceled systems have higher total capacity than Time Division Duplexing systems

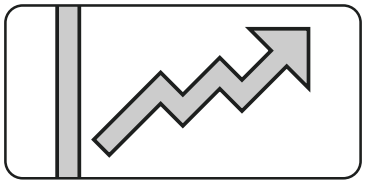
Summary



We described good parameter values to use in the jonsson_3cy_01_10_28_20 channel capacity calculator, including realistic AFE-noise floor and how to account for PCB Insertion Loss



The channel capacity calculations indicate that 25G systems can operate over approximately 7m cables



Echo Canceled systems have higher total throughput than Time Division Duplexing systems

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