FEC Interleaving

Contribution to IEEE 802.3cy

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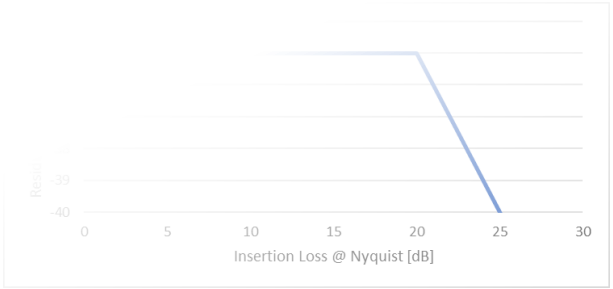
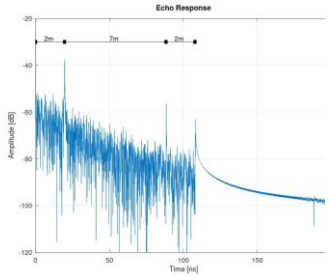
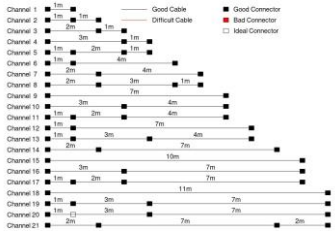
Introduction

- In the Telephonic Interim Meeting on September 9, 2021, the text proposal in [jonsson_etal_3cy_01a_09_21_21] was adopted
- Among the things that were identified for further study are FEC and Interleaving
- This contribution discusses some of the open questions that need to be addressed to select the FEC and the Interleaving depth



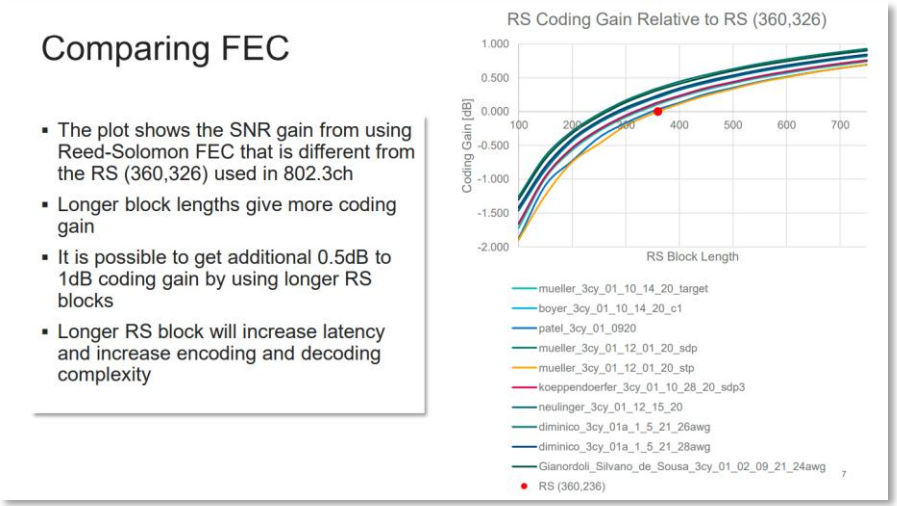




Comparison of RS Block Length

- Initial evaluation of different FEC RS was presented in [jonsson_3cy_01_08_03_21]
- The analysis showed calculated slicer SNR improvement of about 0.75 dB when going from RS(360,326) to RS(750,680)
- The table to the right shows a two times increase in relative HW Decoding Latency, Silicon Area, and Power when going from RS(360,326) to RS(750,680)

NOTE: The RS encoding and decoding are not expected to be the dominant sources of power consumption in an 802.3cy PHY



Source: [https://www.ieee802.org/3/cy/public/adhoc/jonsson_3cy_01_08_03_21.pdf]

	RS(360,326)	RS(750,680)
Relative HW Decoding Latency	**1**	**2**
Relative Silicon Area	**1**	**2**
Relative Power	**1**	**2**

Interleaving Needed Depends on RS Block Size

	Interleaving							
	1x	2x	4x	8x	10x	16x	20x	24x
25G RS(750,680)	12	25	50	100	125	199	249	299
25G RS(360,326)	6	12	24	48	60	97	121	145

Protection (ns)

- The RS(750,680) RS block is slightly more that twice the size of the RS(360,326) block
- To get approximately the same protection from interleaving the RS(750,680) code needs half the number of interleaved blocks of what is needed for RS(360,326)

For example, 2x interleaving for RS(750,680) can provide about the same duration protection as 4x interleaving for RS(360,326)

Open Questions Related to Interleaving

Before we can decide on interleaving

- we need to know the latency requirements for 802.3cy
- we need to know the duration of interfering pulses that need to be protected against
- we need to understand the statistics for the time between pulses
- we need to know what FEC code will be used

More specific questions

- Have the latency requirements changed from 802.3ch?
- Is 50ns the right target for pulse duration?
- What is the probability of having two pulses on top of one another?

Conclusion

Different FEC RS block lengths were compared

Relationship between RS block length and interleaving depth was discussed

We need to decide on FEC before we can decide the interleaving depth

We need to understand better if there have been any changes to the interleaving requirements from 802.3ch

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