Thoughts on the FEC for 802.3cy

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Summary of the TF consented baseline and the pending FEC decision

Jan 2021 Motion #3: Draft timeline
- Draft 1.0 (November 2021)
- Draft 2.0 (March 2022)
- Draft 3.0 (November 2022)

(1) March 2021 Motion #2: Support PHY OAM (multi-lane)
- OAM similar to the MultiGBASE-T1 OAM (Multi-lane)
- Multi-lane De-skew for 50GBASE-T2 and 100GBASE-T4

(2) July 2021 Motion #3/4: Link segment
- Link segment insertion loss limit.
- Link segment return loss limit.

(3) Sept 2021 Motion #3: Modulation text for PCS+PMA
- XGMII changes to 25GMII
- 2.5G/5G/10G changes to 25G
- S=2.5
- The L values for 25G are 1 and TBD, up to four choices.

Oct 2021 Motion #2/3/4/5:
- Test Point

Oct 2021 Motion #6:
- e2e Channel limit

Reviewing 802.3ch MultiGBASE-T1 FEC discussion and conclusion

- STP cable – Transient noise amplitude will be lower than measured on UTP cables (1000BASE-T1);
- Optional pre-coder (1+D/1-D/1-D^2) for controlling DFE error propagations;
- Support burst error protection up to 60ns (tu_3ch_01a_0918.pdf);
  - Transient noise + random errors + some margin
- RS(360,326) with different levels of interleaving is adopted for MultiGBASE-T1, correcting up to 60ns of burst errors, as shown in the following table.

PHY Type	S	Interleave *L=*	Frame (ns)	Burst error protection time (ns)	Latency (ns)	PCS i/p P bits	PCS o/p P+1 bits
2.5GBASE-T1	0.25	1	1280	60.44	1404.44	64	65
5GBASE-T1	0.5	2	2×640	2×30.22	2×702.22	64	65
10GBASE-T1	1	4	4×320	4×15.11	4×351.11	64	65

tu_3ch_01a_0918.pdf

Considerations on the RS FEC for 25GBASE-T1

- **Consideration 1:** The burst error protection when required is larger than 60ns, since the impulse environment for 802.3cy is similar to 802.3ch (see also: zimmerman_3cy_01_08_10_21.pdf).
- **Consideration 2:** Random error performance should be equivalent to or better than RS(360,326) FEC (BER_{in} = ~7.08e-4 @ BER_{out} =1e-12) used in 802.3ch.
- **Consideration 3:** Implementation friendly,
  - Simple RS FEC with line rate no more than 28.125Gb/s (Scaling factor S=2.5 from 10GBASE-T1);
  - Feasible RCM (integer/fractional Reference Clock Multiplier) with CLK_{ref}. For example, CLK_{ref} = 10G/(2x32)=156.25MHz, 10GBASE-T1 with RS(360,326), RCM=72.
  - RS FEC (n, k, t, m) information block: $k \times m$ should be divisible by the encoder length if no dummy bit added, e.g. 65 bit for 64/65B.
- **Consideration 4:** Support PHY Layer OAM (March 2021 Motion #2) :
  - 1 OAM symbol per FEC code word (same as 802.3bp and 802.3ch);
- **Consideration 5:** Preferring the same FEC as 25GGBASE-T1 for 50GBASE-T2 and 100GBASE-T4.

What interleave depth (L) is needed for 25GBASE-T1?

- Reusing RS(360,326) for 25GBASE-T1 requires interleave depth ***L*=10** to correct up to 60ns of burst errors. The overall interleaving for 50GBASE-T2 and 100GBSE-T4 will be 20 and 40.
- For RS FEC (n, k, t, m), the burst error protection time T_c can be roughly evaluated as $(t \times m) \cdot L / R_{\text{line}}$.
- Larger GF(2^{12}) field has to be used for small interleave depth (L≤3).

Interleave L=	**$t \times m$ for $T_c \geq 60\text{ns}$** (Assuming no bandwidth expansion, R_{serdes}=25Gb/s)	**Possible GF field (2^m)**
1	>1500	m=10, $\rightarrow \begin{cases} n \leq 1023 \\ t > 150 \end{cases}, \rightarrow CR = \frac{k}{n} < 0.707$ m=12, $\rightarrow \begin{cases} n \leq 4095 \\ t > 125 \end{cases}, \rightarrow CR = \frac{k}{n} < 0.939$
2	>750	m=10 (CR<0.853) , m=12 (CR<0.969)
4	>375	m=10 (CR<0.926), m=12 (CR<0.984)
8	>187.5	m=10 (CR<0.963), m=12 (CR<0.992)
10	>150	m=10 (CR<0.971), m=12 (CR<0.994)

FEC candidates for 25GBASE-T1 (64/65B, *L*=1)

- For a given ***m*** and ***L***, smaller ***n*** generally indicates less implementation complexity.

Interleave Depth (*L*)	*n*	*k*	*n-k*	*m*	# OAM Symbols	# Data Symbols	# PCS blocks	Frame (ns)	Burst Error Protection (ns)	Line Rate (Gb/s)	Overhead (%)	PCS_ibits	PCS_obits
1	2880	2601	279	12	1	2600	480	1228.8	59.307	28.125	12.5	64	65
1	2952	2666	286	12	1	2665	492	1259.52	61.013	28.125	12.5	64	65
1	3024	2731	293	12	1	2730	504	1290.24	62.293	28.125	12.5	64	65
1	3096	2796	300	12	1	2795	516	1320.96	64.000	28.125	12.5	64	65
1	3168	2861	307	12	1	2860	528	1351.68	65.280	28.125	12.5	64	65
1	3240	2926	314	12	1	2925	540	1382.4	66.987	28.125	12.5	64	65
1	3312	2991	321	12	1	2990	552	1413.12	68.267	28.125	12.5	64	65
1	3384	3056	328	12	1	3055	564	1443.84	69.973	28.125	12.5	64	65
1	3456	3121	335	12	1	3120	576	1474.56	71.253	28.125	12.5	64	65
1	3528	3186	342	12	1	3185	588	1505.28	72.960	28.125	12.5	64	65
1	3540	3251	289	12	1	3250	600	1536	62.481	27.65625	10.625	64	65
1	3560	3251	309	12	1	3250	600	1536	66.445	27.8125	11.25	64	65
1	3600	3251	349	12	1	3250	600	1536	74.240	28.125	12.5	64	65
1	3672	3316	356	12	1	3315	612	1566.72	75.947	28.125	12.5	64	65
1	3744	3381	363	12	1	3380	624	1597.44	77.227	28.125	12.5	64	65
1	3816	3446	370	12	1	3445	636	1628.16	78.933	28.125	12.5	64	65
1	3850	3576	274	12	1	3575	660	1689.6	60.123	27.34375	9.375	64	65
1	3888	3511	377	12	1	3510	648	1658.88	80.213	28.125	12.5	64	65
1	3894	3576	318	12	1	3575	660	1689.6	68.990	27.65625	10.625	64	65
1	3916	3576	340	12	1	3575	660	1689.6	73.348	27.8125	11.25	64	65
1	3920	3641	279	12	1	3640	672	1720.32	61.001	27.34375	9.375	64	65
1	3960	3576	384	12	1	3575	660	1689.6	81.920	28.125	12.5	64	65
1	3990	3706	284	12	1	3705	684	1751.04	62.318	27.34375	9.375	64	65
1	4032	3641	391	12	1	3640	672	1720.32	83.200	28.125	12.5	64	65
1	4060	3771	289	12	1	3770	696	1781.76	63.195	27.34375	9.375	64	65

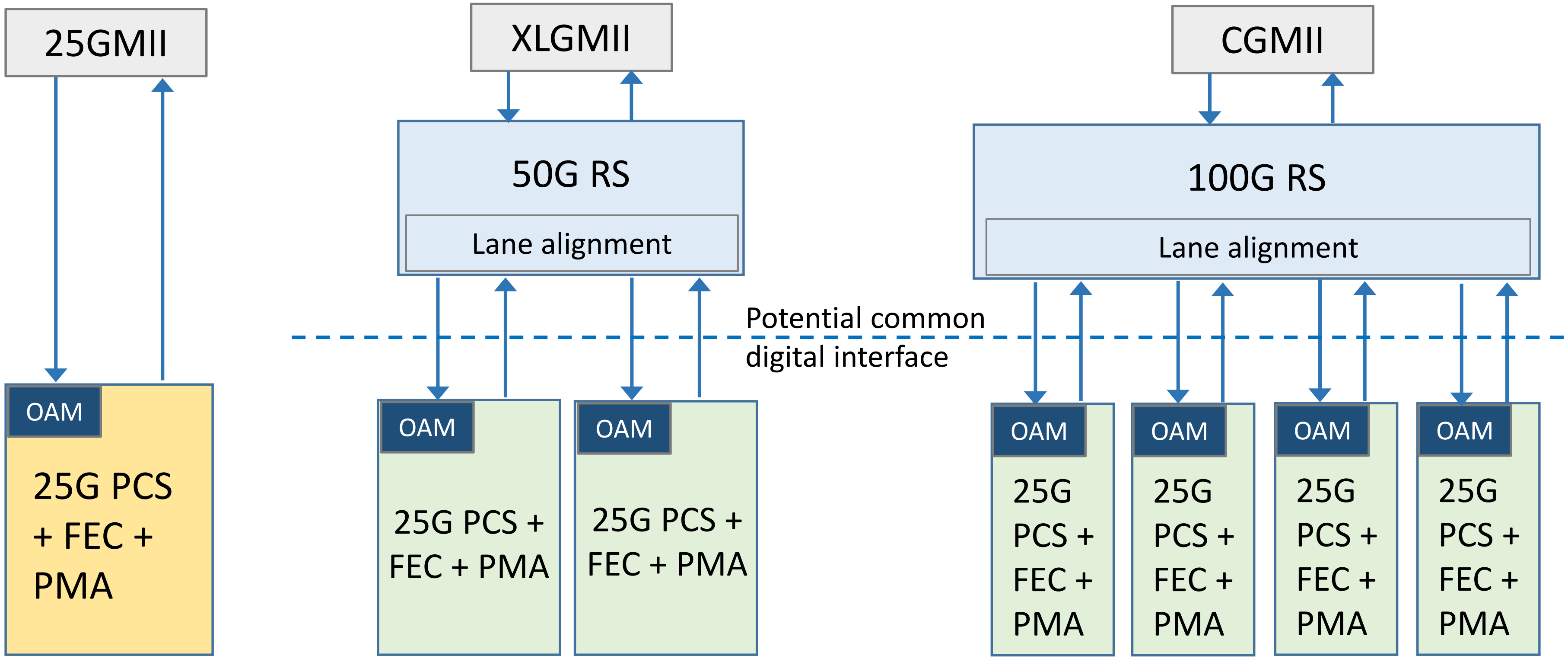
FEC candidates for 25GBASE-T1 (64/65B)

- In the case of 64/65B encode, 10 different RS FEC with varied interleaving can correct up to 60ns burst errors.
- Reusing 802.3ch FEC RS(360,326) requires a interleaving depth ***L*** of 10, which can be reduced by using new FEC with larger block size. For example, doubled block size of RS(720, 651) compared with RS(360,326) reduces interleaving by half, and improves random error performance.

Interleave Depth (*L*)	*n*	*k*	*n-k*	*m*	# OAM Symbols	# Data Symbols	# PCS blocks	Frame (ns)	Burst Error Protection (ns)	Line Rate (Gb/s)	Overhead (%)	PCS_ ibits	PCS_ obits	BER_{in} @ BER_{out}=1e-12
1	2952	2666	286	12	1	2665	492	1259.52	61.013	28.125	12.5	64	65	2.35e-3
2	1512	1366	146	12	1	1365	252	645.12	31.147	28.125	12.5	64	65	1.82e-3
3	1008	911	97	12	1	910	168	430.08	20.480	28.125	12.5	64	65	1.45e-3
4	936	846	90	10	1	845	130	332.8	16.000	28.125	12.5	64	65	1.68e-3
5	720	651	69	10	1	650	100	256	12.089	28.125	12.5	64	65	1.36e-3
6	648	586	62	10	1	585	90	230.4	11.022	28.125	12.5	64	65	1.29e-3
7	576	521	55	10	1	520	80	204.8	9.600	28.125	12.5	64	65	1.12e-3
8	504	456	48	10	1	455	70	179.2	8.533	28.125	12.5	64	65	1.03e-3
9	432	391	41	10	1	390	60	153.6	7.111	28.125	12.5	64	65	8.33e-4
10	360	326	34	10	1	325	50	128	6.044	28.125	12.5	64	65	7.08e-4

FEC for 50GBASE-T2 and 100GBASE-T4

- Lane PMA/FEC/PCS as a unit allows independent PHY units to be bonded (zimmerman_3cy_01_05_18_21.pdf).
- The FEC for 50GBASE-T2 and 100GBASE-T4 can reuse the FEC of 25GBASE-T1.



zimmerman_3cy_01_05_18_21.pdf

Conclusion & Proposal

Conclusion:

- Considering lane PMA/FEC/PCS as a unit, the two-lane 50GBASE-T2 and four-lane 100GBASE-T4 can fully reuse the 25GBASE-T1 PMA/FEC/PCS.
- Reusing RS(360,326) and 64/65B encode for 25GBASE-T1 requires interleave depth ***L***=10 to correct up to 60ns burst errors.
  - ***L***=10 implies certain level of FEC process complexity.
  - Upper layer retransmission could be considered if smaller ***L*** (***L*** <10 or even ***L*** =1) is preferred.
- Less interleave depth ***L*** requires new FEC with increased block size.
  - Some new FEC candidates such as RS(720,651), ***L***=5 meets the 60ns burst error protection time.
  - More FEC options can be achieved for different OAM lengths (≠1).

Proposal:

- If the burst error protection time up to 60ns is a 'must' and 802.3ch FEC is reused, ***L***=10 should be one of 25GBASE-T1 FEC interleaving options.
- More work could be done on the gain/latency/area of the new RS FEC candidates before the final decision.

Different encode of the PCS layer could be also considered

- In previous slides, we have only considered the FEC candidates using 64/65B encode, adopted in both 802.3ch and 802.3cz.
- Shall we consider a different encode for 25GBASE-T1? Changing the encode may give different FEC options, since the number of blocks should be integer RS symbols.
- The more we compress the encode, the larger margin we give for the FEC. For example, to achieve 60ns protection using interleaving ***L*=4**, we have the FEC option **RS(936,846)** in the case of 64/65B, while **RS(768,685)** in the case of 512/513B.
- We have provided more FEC candidates for different encode (128/129B, 256/257B, 512/513B) in the backup slides.

Thank you!

FEC candidates for 25GBASE-T1 (128/129B)

- Using 128/129B encode, 7 different RS FEC coupled with varied interleaving achieves 60ns burst error protection.
- For a given ***L*** **(*L*<10)**, RS FEC code word in the case of 128/129B encode gives smaller ***n*** than 64/65B.

Interleave Depth (*L*)	***n***	***k***	***n-k***	***m***	# OAM Symbols	# Data Symbols	# PCS blocks	Frame (ns)	Burst Error Protection (ns)	Line Rate (Gb/s)	Overhead (%)	PCS_ ibits	PCS_ obits	BER_{in} @ BER_{out}=1e-12
1	2736	2452	284	12	1	2451	228	1167.36	60.587	28.125	12.5	128	129	2.52e-3
2	1392	1248	144	12	1	1247	116	593.92	30.720	28.125	12.5	128	129	1.94e-3
3	912	818	94	12	1	817	76	389.12	20.053	28.125	12.5	128	129	1.55e-3
4	864	775	89	10	1	774	60	307.2	15.644	28.125	12.5	128	129	1.75e-3
5	720	646	74	10	1	645	50	256	13.156	28.125	12.5	128	129	1.57e-3
6	576	517	59	10	1	516	40	204.8	10.311	28.125	12.5	128	129	1.28e-3
7	576	517	59	10	1	516	40	204.8	10.311	28.125	12.5	128	129	1.28e-3
8	432	388	44	10	1	387	30	153.6	7.822	28.125	12.5	128	129	1.01e-3
9	432	388	44	10	1	387	30	153.6	7.822	28.125	12.5	128	129	1.01e-3
10	432	388	44	10	1	387	30	153.6	7.822	28.125	12.5	128	129	1.01e-3

FEC candidates for 25GBASE-T1 (256B/257B)

- Using 256/257B encode, we have 7 different RS FEC options, which can correct up to 60ns burst error by resorting to interleaving.
- RS (560,515) for *L*≥8 has slightly better random error performance than RS (360,326) with *L*=10.

Interleave Depth (*L*)	*n*	*k*	*n-k*	*m*	# OAM Symbols	# Data Symbols	# PCS blocks	Frame (ns)	Burst Error Protection (ns)	Line Rate (Gb/s)	Overhead (%)	PCS_ ibits	PCS_ obits	BER_{in} @ BER_{out}=1e-12
1	2880	2571	309	12	1	2570	120	1228.8	65.707	28.125	9.09	256	257	2.66e-3
2	1440	1286	154	12	1	1285	60	614.4	32.853	28.125	9.09	256	257	2.07e-3
3	1152	1029	123	12	1	1028	48	491.52	26.027	28.125	9.09	256	257	1.83e-3
4	864	772	92	10	1	771	30	307.2	16.356	28.125	9.09	256	257	1.88e-3
5	840	772	68	10	1	771	30	307.2	12.434	27.34375	6.06	256	257	1.17e-3
6	576	515	61	10	1	514	20	204.8	10.667	28.125	9.09	256	257	1.36e-3
7	576	515	61	10	1	514	20	204.8	10.667	28.125	9.09	256	257	1.36e-3
8	560	515	45	10	1	514	20	204.8	8.046	27.34375	6.06	256	257	7.84e-4
9	560	515	45	10	1	514	20	204.8	8.046	27.34375	6.06	256	257	7.84e-4
10	560	515	45	10	1	514	20	204.8	8.046	27.34375	6.06	256	257	7.84e-4

FEC candidates for 25GBASE-T1 (512B/513B)

- Using 512/513B encode, we again have 7 different RS FEC options, which can correct up to 60ns burst error by resorting to interleaving.
- The last two FEC options RS(576,514) and RS(560,514) are close to that using 256/257B encode.

Interleave Depth (*L*)	*n*	*k*	*n-k*	*m*	# OAM Symbols	# Data Symbols	# PCS blocks	Frame (ns)	Burst Error Protection (ns)	Line Rate (Gb/s)	Overhead (%)	PCS_ ibits	PCS_ obits	BER_{in} @ BER_{out}=1e-12
1	2688	2395	293	12	1	2394	56	1146.88	62.293	28.125	12.5	512	513	2.66e-3
2	1344	1198	146	12	1	1197	28	573.44	31.147	28.125	12.5	512	513	2.05e-3
3	960	856	104	12	1	855	20	409.6	22.187	28.125	12.5	512	513	1.72e-3
4	768	685	83	12	1	684	16	327.68	17.493	28.125	12.5	512	513	1.47e-3
5	576	514	62	12	1	513	12	245.76	13.227	28.125	12.5	512	513	1.21e-3
6	576	514	62	10	1	513	10	204.8	11.022	28.125	12.5	512	513	1.44e-3
7	576	514	62	10	1	513	10	204.8	11.022	28.125	12.5	512	513	1.44e-3
8	560	514	46	10	1	513	10	204.8	8.411	27.34375	9.375	512	513	8.54e-4
9	560	514	46	10	1	513	10	204.8	8.411	27.34375	9.375	512	513	8.54e-4
10	560	514	46	10	1	513	10	204.8	8.411	27.34375	9.375	512	513	8.54e-4