802.3cy TX Droop Spec Revisited

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Introduction

- D2.1 Test mode 6 waveform
  - When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 320 {+1} symbols followed by 320 {–1} symbols with the transmitted symbols timed from its local clock source.
- 165.5.3.1 Maximum output droop
  - With the transmitter in test mode 6 and using the transmitter test configuration 1 shown in Figure 165–25, the magnitude of both the positive and negative droop shall be less than 15%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).
- Question: do we need to change the spec ?
- We present simulation results based on board trace and PHY MDI termination impedance, with both non-PoDL and PoDL cases
- Conclusion: existing D2.1 Tx droop spec is reasonable

D2.1 Droop Test Configuration

165.5.1.1 Test configurations

The following configurations, or their equivalents, as shown in Figure 165–25, Figure 165–26, and Figure 165–27, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

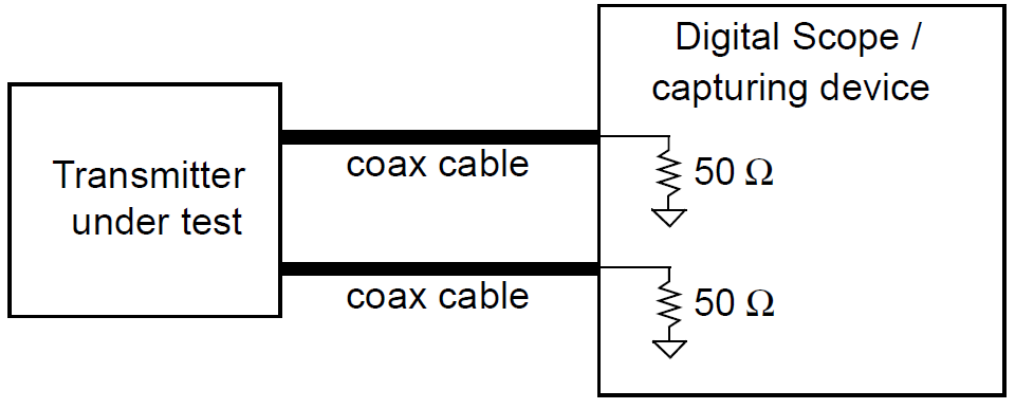
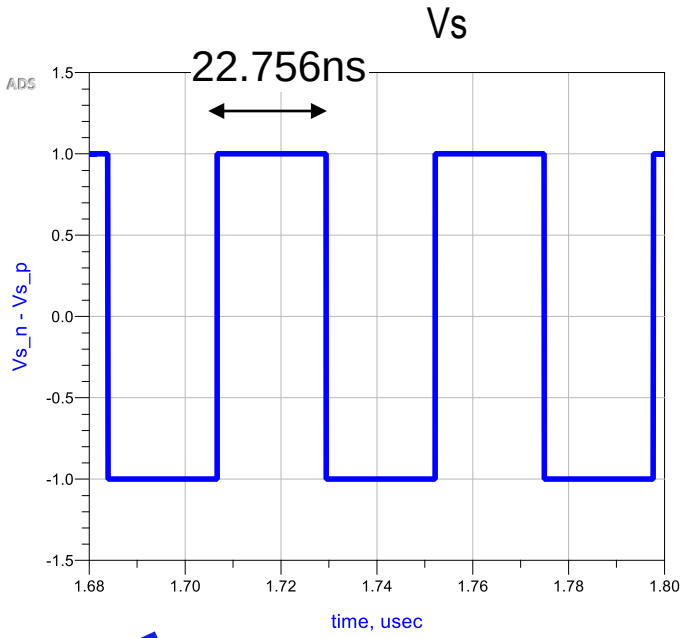


Figure 165–25—Transmitter test configuration 1 for transmitter droop, transmitter linearity, and jitter measurement

Simulation Setup

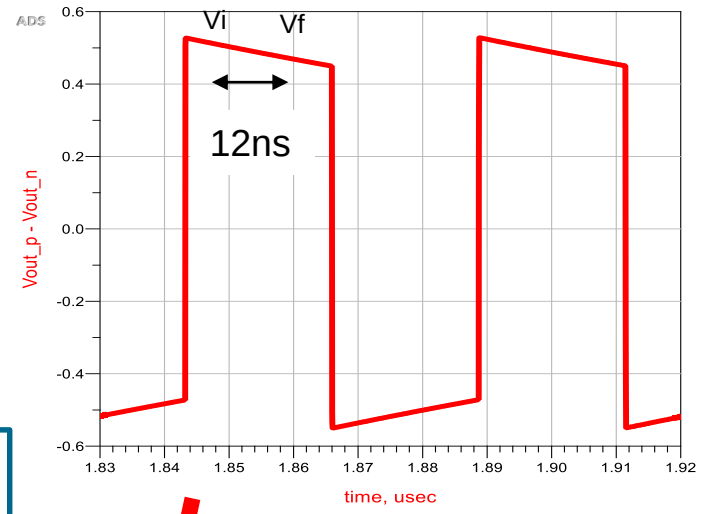
- Board trace models
  - Board trace length: 0.75 in
  - Impedance variation: -10% considered
  - Board material: FR408
- PHY termination impedance
  - +5% case is considered
- PoDL inductance and capacitance also considered
- D2.1 Test Mode 6 is used to generate source square pulse waveform

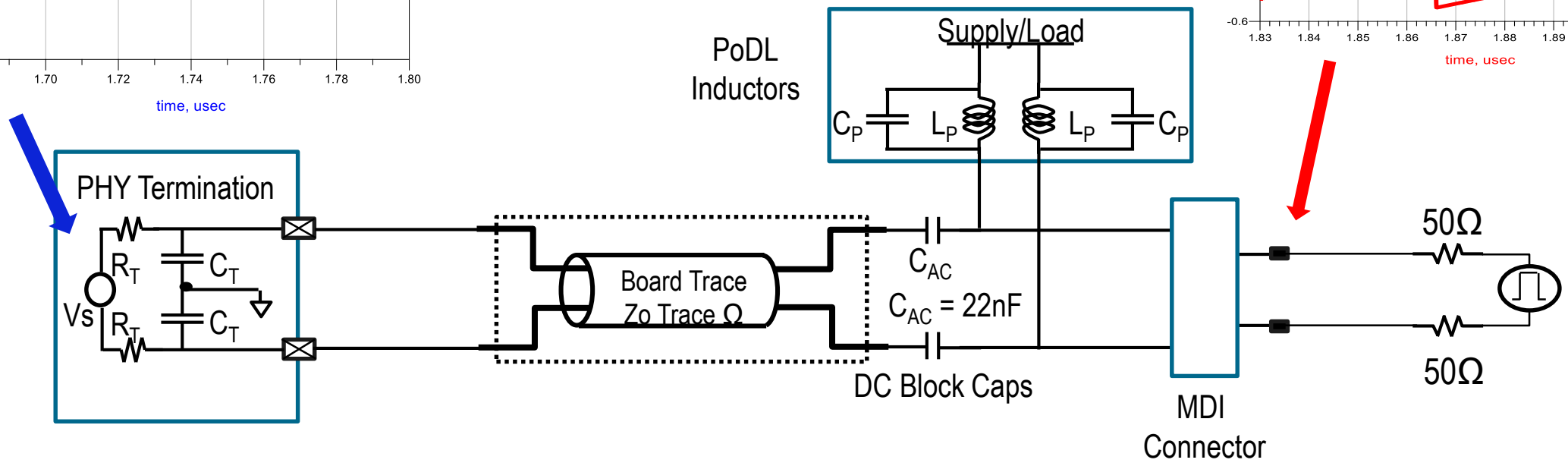
Tx Droop Simulation Model



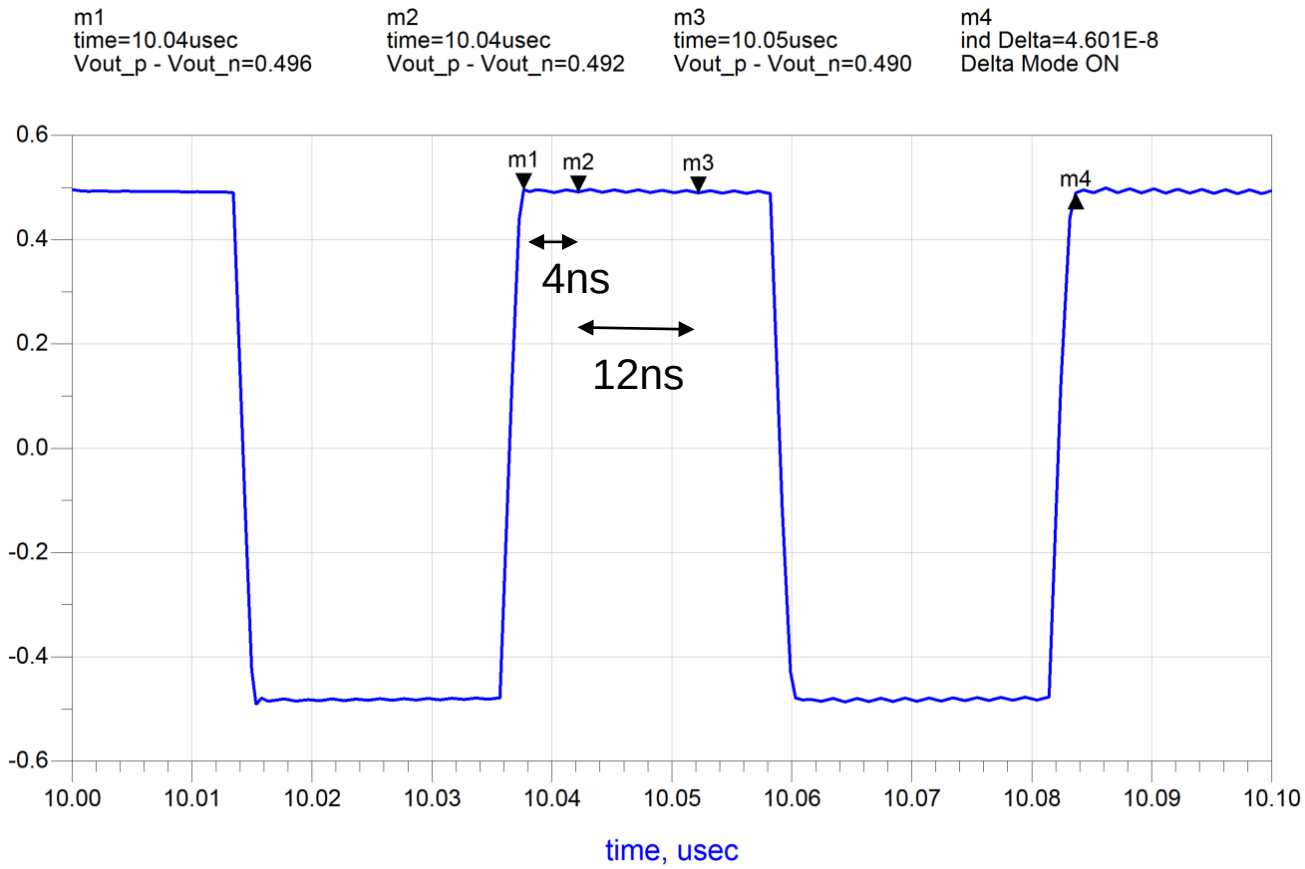
Element	unit	min	nom	max
R_T	Ω	45	50	55
Zo	Ω	45	50	55
C_T	pF		0.10	
L_P	µH	2	4.7	
C_P	pF		0.15	
Z_o	Ω	90	100	110

Droop = (Vi - Vf)/Vi





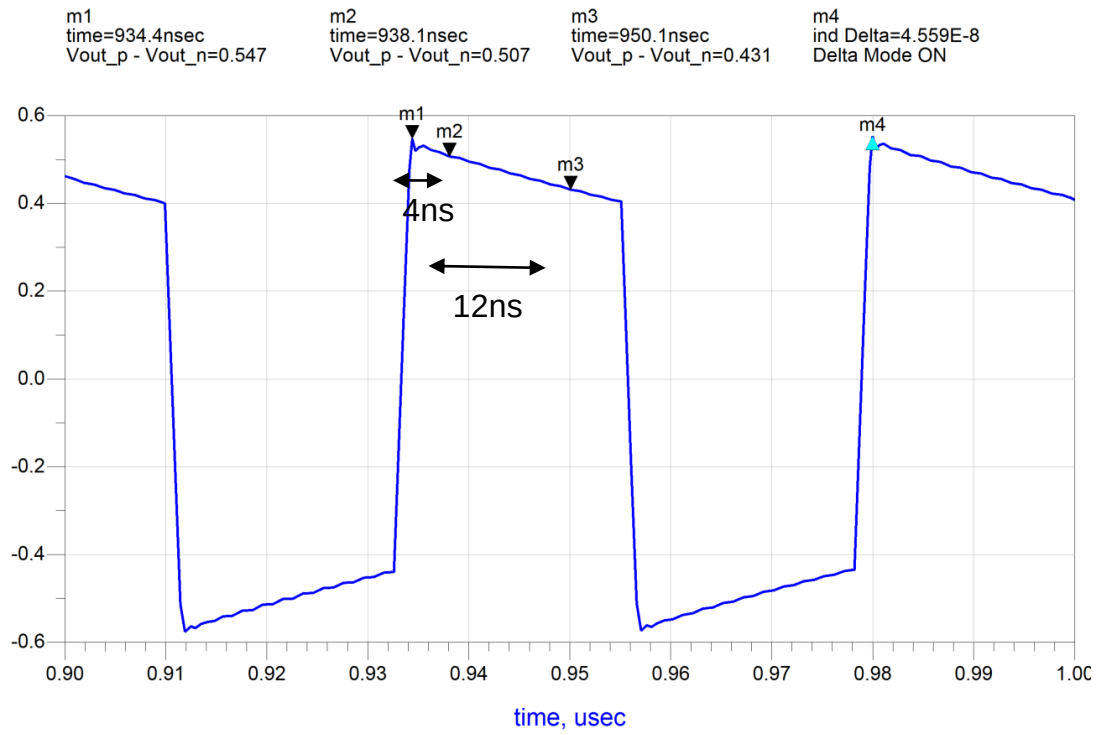
Tx Droop: Non PoDL Case



PHY = 105 Ohm
Trace = 90 Ohm

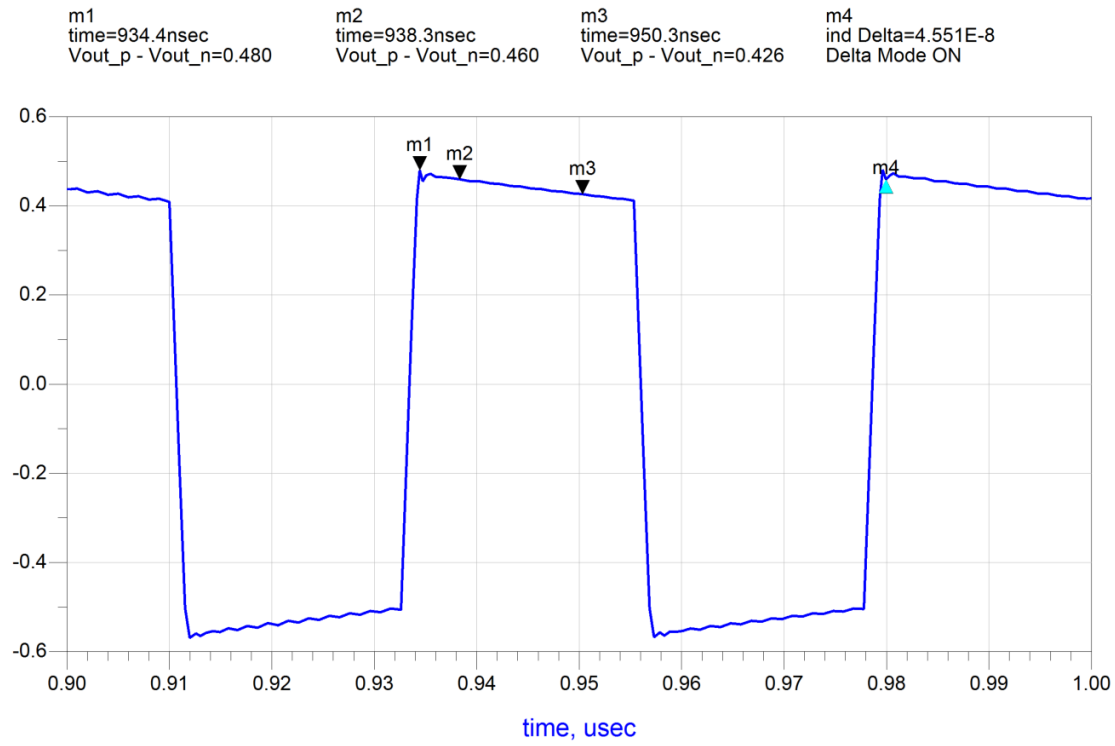
$$\text{Droop} = \frac{Vm_2 - Vm_3}{V_{m2}} * 100\ \% = 0.4\%$$

Tx Droop: PoDL with L=2uH vs. L=4.7uH



L=2uH

$$\text{Droop} = \frac{Vm_2 - Vm_3}{V_{m2}} * 100\ \% = 15\%$$

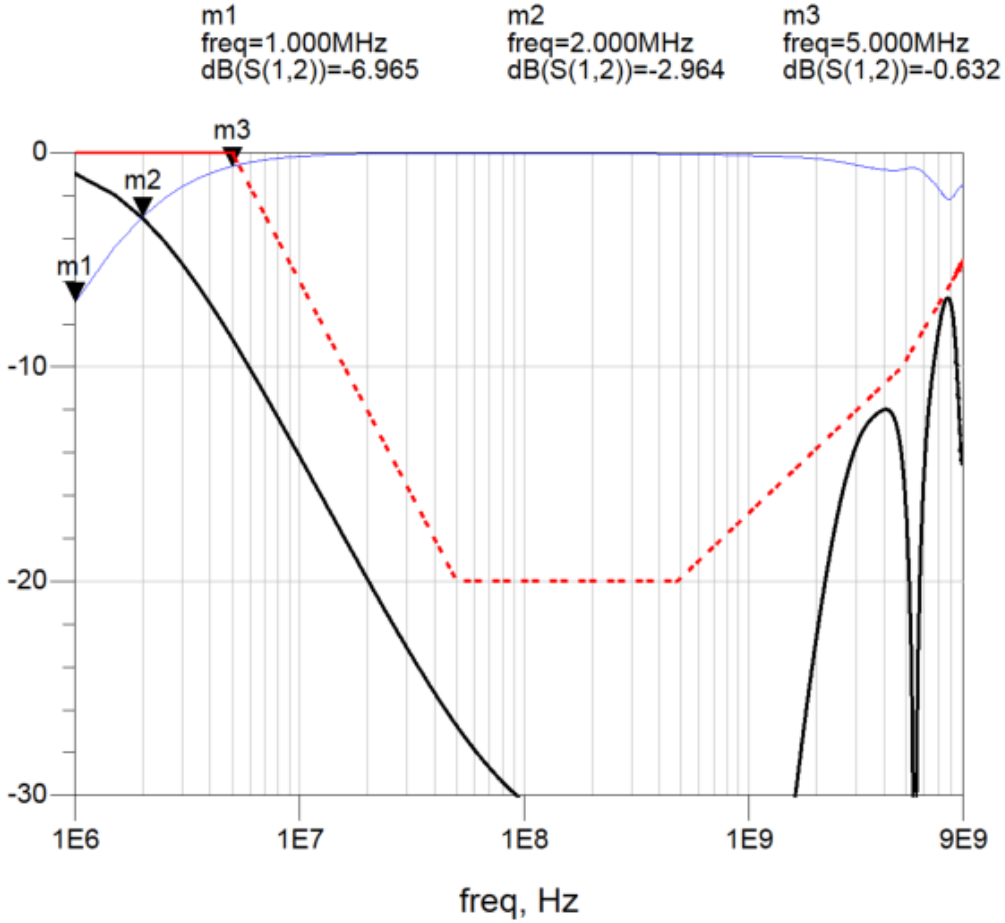


L=4.7uH

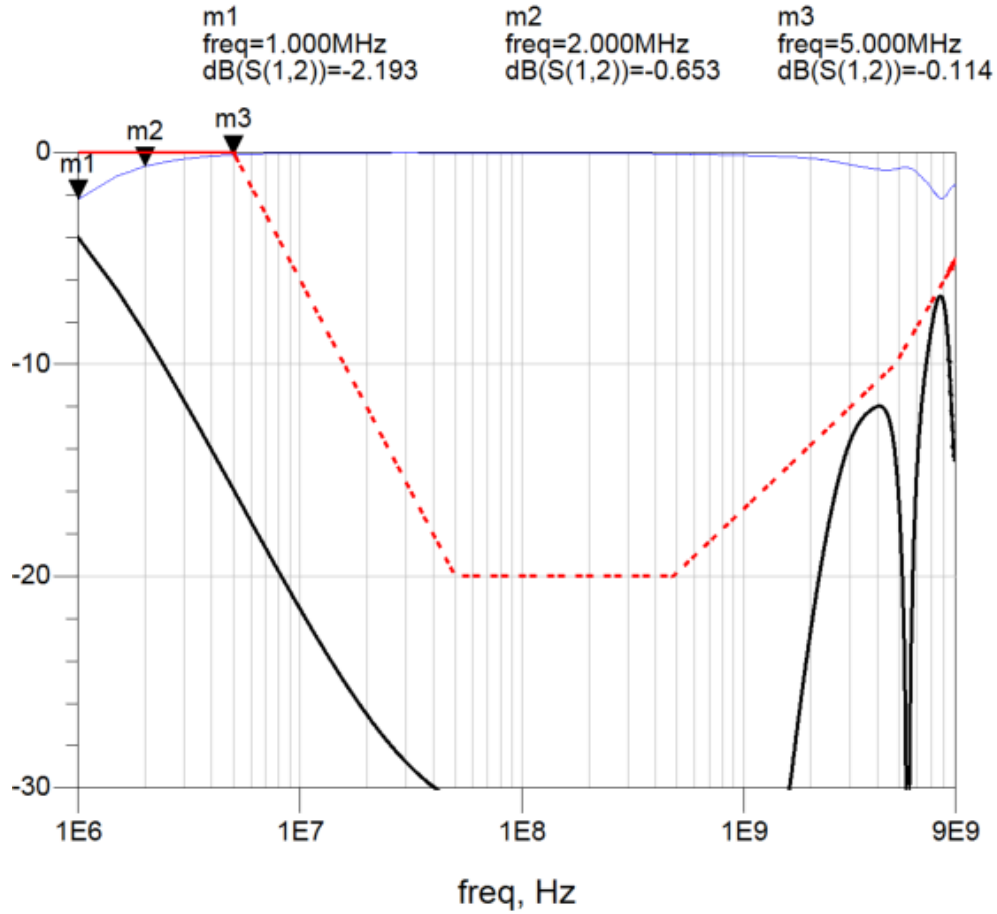
$$\text{Droop} = \frac{Vm_2 - Vm_3}{V_{m2}} * 100\ \% = 7.4\%$$

PHY = 105 Ohm
Trace = 90 Ohm

MDI RL and IL: PoDL with L=2uH vs. L=4.7uH



L=2uH



L=4.7uH

PHY = 105 Ohm
Trace = 90 Ohm

Impact of PoDL Inductance on Droop

Droop duration	DC cap	PoDL, L	Vi @4ns	Vf @16ns	TX IL 1 MHz	TX IL 2 MHz	TX IL 5 MHz	Droop Calculated	Droop sim
12ns	22nF	No PODL	0.492V	0.49V	-0.03 dB	-0.01 dB	0 dB		0.4%
12ns	22nF	4.7uH	0.46V	0.426V	-2.2 dB	-0.6 dB	-0.1 dB	6.2%	7.4%
12ns	22nF	2uH	0.507 V	0.431V	-6.9 dB	-2.9 dB	-0.6 dB	14%	15%

- Droop Calculated = $1 - e^{-td / (2*L/R)}$, where td =12ns and R=50 Ohm

Conclusion

- 802.3cy D2.1 Test Mode 6 output waveform provides sufficient time to measure both positive and negative droops.
- For the non-PoDL case, the Tx droop is less than 1%
- For the PoDL cases, the 15% droop over 12ns spec can be met with a minimum PoDL inductor of 2uH.
  - With 2uH PoDL inductors, the Tx droop over 12 ns is 15% and the board IL is 6.9dB at 1MHz.
  - With 4.7uH PoDL inductors, the Tx droop over 12 ns is 7.4% and the board IL is 2.2dB at 1MHz.
- If the board IL at 1MHz needs to be further limited, then one can tighten the droop percentage correspondingly.
- For now, we believe the D2.1 droop test is adequate and does not require further changes.